Analysis and Comparative Evaluation of a Three-Phase Three-Level Unity Power Factor Y-Rectifier

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Abstract. **The basic principle of operation of a three-phase PWM rectifier system formed by star-connection of three single-phase three-level PWM rectifier modules (three-level Y-Rectifier) is discussed based on space vector calculus. The mains current ripple resulting for synchronized operation of the phase modules is calculated and comparatively evaluated against a direct three-phase PWM (Vienna) Rectifier realization. The current stresses on the power semiconductors and on the passive power components are calculated analytically in order to provide a basis for the system dimensioning. A novel concept for controlling the Y-Rectifier is proposed which guarantees a symmetric loading of the phase modules and allows to continue the system operation also in case of heavily unbalanced mains voltage and/or for a failure of a mains phase. Finally, the advantages and drawbacks of the Y-Rectifier concept are summarized and topics of further research are identified.**

1. Introduction

The input stage of high-power telecommunications power supply modules basically can be realized in modular form, i.e. by star-connection (*Y-Rectifier* [1,2], cf. **Fig.1**(a)) or delta-connection (*Δ-Rectifier*, [3]) of single-phase PWM rectifier modules with individual DC output voltages or in direct three-phase form, i.e. with a DC output voltage being common to all phases (*Vienna Rectifier* [4], cf. Fig.1(b)).

The three-level structure of the Vienna Rectifier results in a low blocking voltage stress on the power semiconductors and a low volume of the input inductors and therefore allows the realization of three-phase rectifier systems with high efficiency and high power density. Similar properties are given for the Δ-Rectifier in case the line-to-line modules are realized in three-level technique [5]. However, for a wide line-to-line input voltage range of 320…530V_{rms} the output voltage has to be set for both systems to 800 V_{DC} and/or the output stage has to be realized using a series connection of two DC/DC converters and/or a three-level converter topology in order to allow the application of 600V power semiconductors and/or to utilize the advantages resulting from a low on-resistance of the power MOSFETs and low reverse recovery time of the power diodes.

In contrast, the Y-Rectifier shows the advantage of a low DC output voltage of the phase modules of only 400V. Therefore, the DC/DC converters connected in series can be realized using 600V power semiconductor technology as known from single-phase off-line power supplies. For employing three-level PWM rectifier modules, the power semiconductors have to show a blocking capability of only 300V and/or a reduction of the switching losses which are largely determined by the reverse recovery behaviour of the free-wheeling diodes can be achieved as compared to a conventional two-level realization. Furthermore, an interleaved operation of the power transistors of each phase module allows a reduction of the input inductor values for given RMS value of the mains current ripple and/or allows to increase the system power density. There, one also could expect a potential reduction of common-mode noise due to the reduction of the switched voltage level by a factor of 2 resulting in a lower filtering effort for ensuring compliance to EMI standards.

The aforementioned advantages motivate a more detailed analysis of the *Y*-Rectifier which is the subject of this paper. In **Section 2** the basic principle of operation of the system is described and the space vectors of the rectifier input voltage being available for the sinusoidal control of the mains current are analyzed. In **Section 3** the current stresses on the power semiconductors and on the passive power components are calculated analytically in order to provide a basis for the dimensioning of the system. In **Section 4** a concept for controlling the Y-Rectifier is proposed which does allow to continue the system operation also in case of heavily unbalanced mains voltage and/or for a failure of a mains phase. Finally, in **Section 5** the advantages and drawbacks of the Y-Rectifier are summarized and topics of further research are identified.

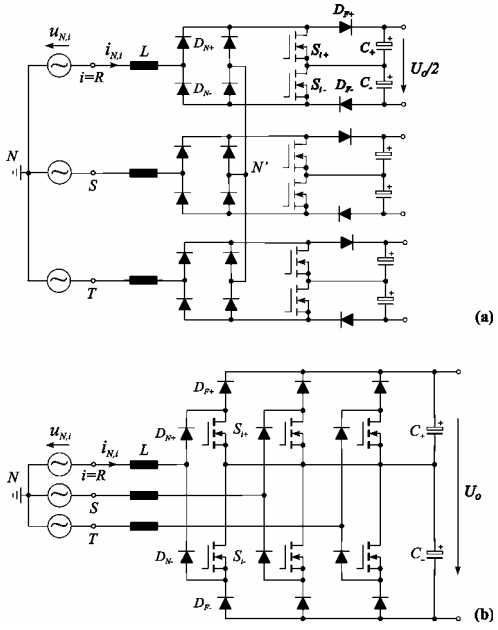


Fig.1: Modular and direct three-phase realization of three-phase PWM rectifier systems; **(a)**: Three-level *Y-Rectifier* formed by star-connection of three single-phase three-level PWM rectifier systems [2], **(b)**: *Vienna Rectifier* (basically, only a single power transistors is required for the realization of the system [4]; the topology shown has been selected in order allow a direct comparison to the Y-Rectifier which also employs 6 power transistors).

2. Basic Principle of Operation

The AC side equivalent circuit of a Y-Rectifier is shown in **Fig.2**(a). There, we have for the current formation in each phase i=R,S,T,

$$u_{N,i} = L\frac{di_{N,i}}{dt} + u_{U,i} + u_{N'N} \,. \tag{1}$$

where the sign of the rectifier input phase voltage $u_{U,i}$ is determined by the direction of the corresponding phase current $i_{N,i}$. Considering

$$i_{N,R} + i_{N,S} + i_{N,T} = 0 \tag{2}$$

there results for a purely sinusoidal symmetric mains voltage system, i.e. for $\Sigma u_{N,i}$=0,

$$u_{N'N} = -\frac{1}{3}(u_{U,R} + u_{U,S} + u_{U,T}) = -u_{U,0} \,. \tag{3}$$

Due to zero sequence component $u_{U,0}$ = $^1/_3$($u_{U,R}$+$u_{U,S}$ +$u_{U,T}$) contained in the phase voltages $u_{U,i}$, a voltage $u_{N'N}$ does appear between the star point N' of the phase modules and the mains star point N. Accordingly, in each phase only the voltage

$$u_{U,i}' = u_{U,i} - u_{U,0} = u_{U,i} - \frac{1}{3}(u_{U,R} + u_{U,S} + u_{U,T}) \,, \tag{4}$$

which contains no zero-sequence component is effective for the current formation. Therefore, we have as shown in **Fig.2**(b)

$$u_{N,i} = L\frac{di_{N,i}}{dt} + u_{U,i}' \,. \tag{5}$$

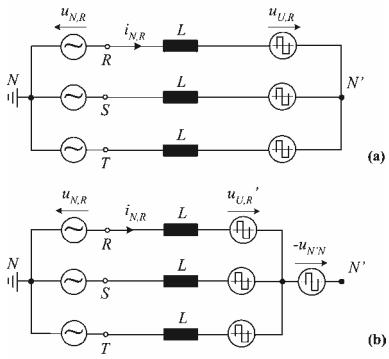


Fig.2: AC-side equivalent circuit of the Y-Rectifier **(a)**; the mains current is defined by the component $u_{U,i}'$ of a phase voltage $u_{U,i}$ (remaining after subtraction of the zero sequence component) in combination with the corresponding mains phase voltage $u_{N,i}$ (cf. **(b)**).

For combining the phase quantities $u_{U,i}'$ in a complex space vector

$$\underline{u}_U' = \frac{2}{3}(u_{U,R}' + \underline{a}u_{U,S}' + \underline{a}^2 u_{U,T}') \,, \tag{6}$$

$$\underline{a} = e^{j\frac{2\pi}{3}} \,, \tag{7}$$

and for introducing equally defined space vectors for the mains phase voltages $u_{N,i}$ and the mains phase currents $i_{N,i}$, (5) results in

$$\underline{u}_N = L\frac{d\underline{i}_N}{dt} + \underline{u}_U' \,. \tag{8}$$

The phase quantities $u_{U,i}'$ and $i_{N,i}$ and/or the space vectors $\underline{u}_{U,i}'$ and $\underline{i}_N$ now can be decomposed into a mains frequency fundamental (index *(1)*) and a switching frequency ripple (distortion) component (Index n),

$$\begin{matrix} \underline{u}_U' = \underline{u}_{U,(1)} + \underline{u}_{U,n} \\ \underline{i}_N = \underline{i}_{N,(1)} + \underline{i}_{N,n} \end{matrix} \;; \tag{9}$$

considering (8) we then have

$$\underline{u}_N = \hat{U}_N e^{j\omega_N t} = L\frac{d\underline{i}_{N,(1)}}{dt} + \underline{u}_{U,(1)} = j\omega_N L\underline{i}_{N,(1)} + \underline{u}_{U,(1)} = j\omega_N L\hat{I}_N e^{j\omega_N t} + \hat{U}_U e^{j\omega_N t} \tag{10}$$

$$L\frac{d\underline{i}_{N,n}}{dt} = \underline{u}_{U,(1)} - \underline{u}_U' \,. \tag{11}$$

For achieving a sinusoidal shape $\underline{i}_{N,(1)}$ of the mains current, a rectifier input voltage $\underline{u}_U' = \underline{u}_{U,(1)} = \hat{U}_U e^{j\omega_N t}$ has to be formed in the average over a pulse period. The distortion, i.e. the ripple $\underline{i}_{N,n}$ of the input current $\underline{i}_N$ is caused by the difference of the actually applied voltage $\underline{u}_U'$ and the ideal voltage $\underline{u}_{U,(1)}$. Therefore, in order to ensure a minimum mains current distortion, the voltage vector $\underline{u}_{U,(1)}$ (showing constant magnitude and constant angular speed) has to be formed using switching states which are corresponding to voltage space vectors in the immediate vicinity of $\underline{u}_{U,(1)}$. Due to employing 6 power transistors, the Y-Rectifier basically shows 2^6=64 possible switching states which are denoted in the following by the combination of the power transistor switching functions

$$\underline{s}_{RST,i} = \begin{pmatrix} s_{R+} s_{S+} s_{T+} \\ s_{R-} s_{S-} s_{T-} \end{pmatrix} \,, \tag{12}$$

(s_{i+}=1 denominates the turn-on state of S_{i+}, i=R,S,T, s_{i+}=0 the turn-off state).

The voltage space vectors $\underline{u}_U'$ corresponding to the different switching states for $i_{N,R}$>0, and $i_{N,S}$, $i_{N,T}$ <0 are depicted in **Fig.3**. Accordingly, for each combination of signs of the phase currents 19 different space vectors are available for the formation of $\underline{u}_{U,(1)}$ and/or for the voltage-proportional control of the mains phase currents ($i_{N,i} \sim u_{N,i}$).

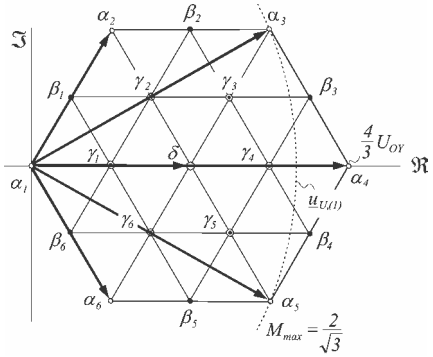
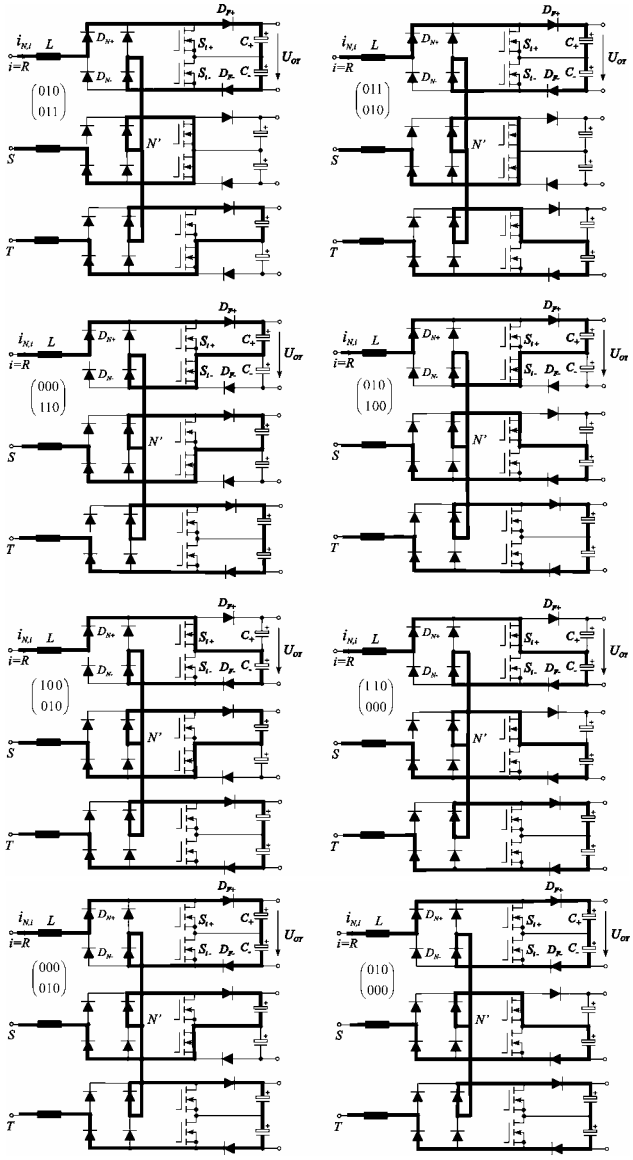


Fig.3: Space vectors $\underline{u}_U'$ of the rectifier input phase voltages $u_{U,i}'$ of the Y-Rectifier available for the mains current control under assumption of $i_{N,R}$>0, $i_{N,S}$, $i_{N,T}$<0. Each of the space vectors β_i, γ_i, and δ can be formed by different switching states (redundancy r_α=1, r_β=2, r_γ=6, r_δ=10). For the Vienna Rectifier only the voltage space vectors α_i, and δ are available (shown by explicit vectors) with a redundancy of r_α=1, and r_δ=2. Furthermore shown: Section of the trajectory $\underline{u}_{U,(1)}$ of the space vector of the phase voltage fundamentals $u_{U,(1),i}$ for maximum modulation M_{max} (cf. (16)). The phase voltages $u_{U,R}'$ can be derived by projection of $\underline{u}_U'$ onto the real axis; accordingly, in total (for $i_{N,R}$>0 and $i_{N,S}$, $i_{N,T}$ <0) 19 voltage space vectors are available for the formation of a voltage shape resulting in $u_{U,(1),R}$ after averaging over a pulse period.

The redundancy of switching states concerning voltage formation allows an active balancing of the partial output voltages and/or a control of the output voltage center point potential of each phase module. According to **Fig.4** we, e.g., have for the switching states resulting in $\underline{u}_U' = \gamma_3$ for the output voltage center point current of phase module R

$$i_{M,R} = \begin{cases} +i_{N,R} & \text{for} \quad \begin{pmatrix}100\\010\end{pmatrix}, \begin{pmatrix}110\\000\end{pmatrix} \\ 0 & \text{for} \quad \begin{pmatrix}010\\011\end{pmatrix}, \begin{pmatrix}011\\010\end{pmatrix} \\ -i_{N,R} & \text{for} \quad \begin{pmatrix}000\\110\end{pmatrix}, \begin{pmatrix}010\\100\end{pmatrix} \end{cases} . \qquad (13)$$

Therefore, for defining a switching state sequence comprising switching states corresponding to $i_{M,R}>0$ and $i_{M,R}<0$, by proper distribution of the total on-time of γ_3 to the switching states an increase and/or a reduction of $u_{C+,R}$ can be performed without direct influence on the mains current control. The same is true for the modules of phases *S* and *T* (cf. Fig.4). For the sake of brevity we would like to omit a further discussion here and would like to only refer to Fig.5 where the balancing of the partial input voltages is integrated into the average input phase current control by an offset $I_{0,i}$ of the carrier signals i_{D+} and i_{D-}.



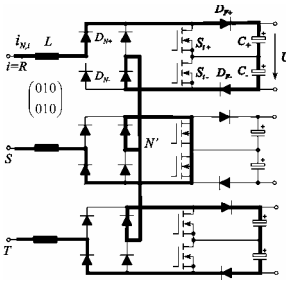


Fig.4: Conduction states of the Y-Rectifier corresponding to the space vectors γ_3 (cf. **(a)**), β_3 (cf. **(b)**) and α_3 (cf. (c)); see Fig.3. For achieving a minimum ripple of the mains current, α_3, β_3 and γ_3 have to be employed for the voltage formation when $\underline{u}_{U,(1)} \approx \underline{u}_N$ (cf. (14)) is pointing into the triangle defined by γ_3, β_3, and α_3; according to ohmic fundamental mains behavior ($u_{N,i} \sim i_{N,i}$) we there have $i_{N,R}>0$, $i_{N,S}<0$, $i_{N,T}<0$.

For the control of three-phase multi-level converters usually space vector oriented modulation concepts are employed [7]. However, in order to minimize the realization effort in the case at hand an average current mode controller with mains voltage feed-forward is be employed in each phase for performing the pulse width modulation (cf. **Fig.5**). There, the synchronization of the phase modules is by carrier signals i_{D+} and i_{D-} being equal for all phases. Furthermore, by phase shifting of i_{D+} and i_{D-} by 180° an interleaved operation of the power transistors S_{+i} and S_{-i} of each module is achieved what results in a formation of the phase voltages $u_{U,i}$ and/or of the mains current ripple with twice the switching frequency f_P. As already mentioned, the partitioning of the output voltage of a module *i* is controlled by an offset signal $I_{0,i}$ where the controller unity gain bandwidth is significantly lower than the mains frequency [8].

The reference values of the mains phase currents are essentially derived by multiplication of the zero sequence free mains phase voltage $u_{N,i}'$ with a reference conductance G_R^* defined by a combination of voltage control loops (cf. Fig.12). The sinusoidal control of each phase current is done by a current controller *R(s)* which slightly changes the pulse pattern resulting from the mains voltage feed-forward in order to ensure the formation of a voltage $\underline{u}_{L,(1)} = j\omega_N L \hat{I}_N \, e^{j\omega_N t}$ (cf. (10)) across the inductors in the average over a pulse period. As the star point *N′* of the phase modules is not connected to the mains neutral *N*, the sum of the phase currents is forced to zero, $\Sigma i_{N,i}=0$, i.e. only two phase currents can be controlled independently. Considering the non-idealities of a practical realization, therefore, no integral component of *R(s)* is admissible in order to avoid a wind-up of the current control. However, due to the mains voltage feed-forward and due to the low absolute value of $\underline{u}_{L,(1)}$ for high switching frequency and/or low inductance *L* also a purely P-type control ensures a low current control error.

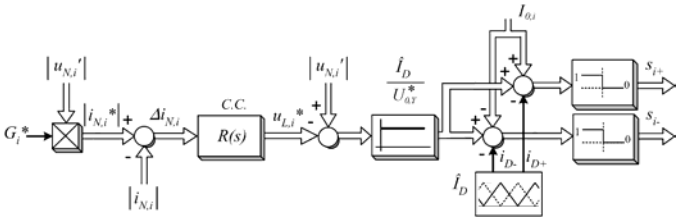


Fig.5: Control of the local average of the rectifier mains phase currents (average current mode control, signal paths being equal for a phases are combined in double lines); for balancing the partial output voltages $u_{C+,i}$ and $u_{C-,i}$ of a phase module, an offset $I_{0,i}$ is added to the carrier signal i_{D+} and/or subtracted from i_{D-}.

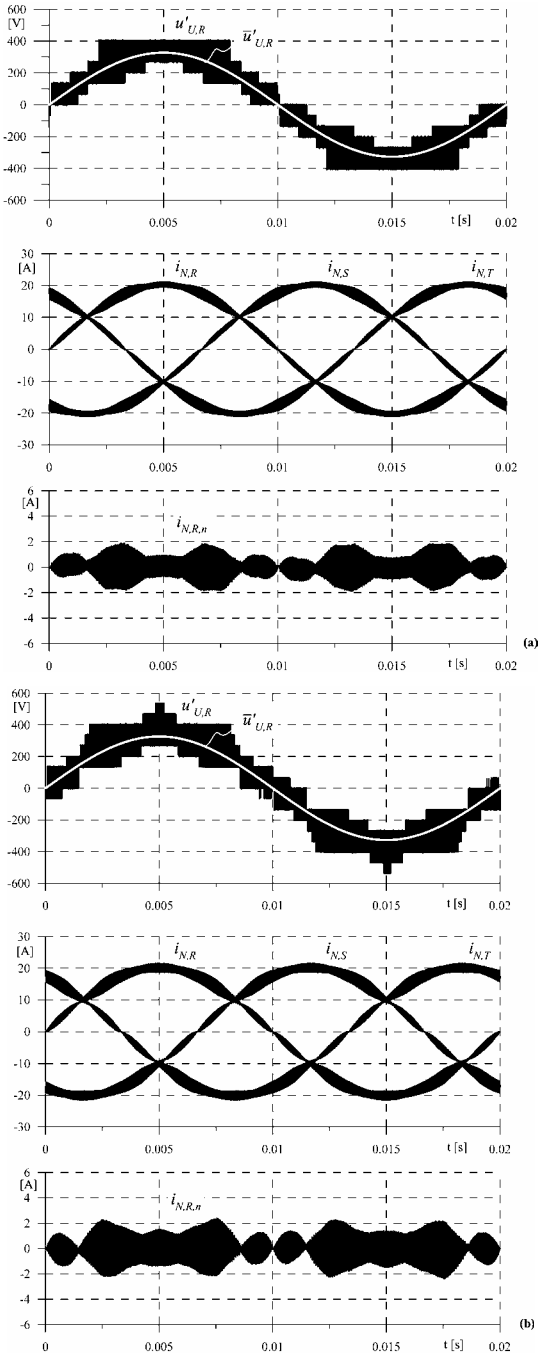


Fig.6: Digital simulation of the stationary operating behavior of a Y-Rectifier employing average current mode control according to Fig.5 for **(a)** mains voltage feed-forward and **(b)** extension of the mains voltage feed-forward by a third harmonic showing $^1/_6$ of the mains voltage amplitude in order to fully utilize the modulation range $M = 0\ldots2/\sqrt{3}$. Shown are: time behavior of the current forming rectifier input phase voltage $u_{U,R}'$, and of the local average value $\bar{u}_{U,R}'$ of $u_{U,R}'$ which is approximately equal to the mains voltage feed-forward signal, and mains phase currents $i_{N,i}$ and ripple component $i_{N,R,n}$ of $i_{N,R}$ **($i_{N,R} = i_{N,(1),R} + i_{N,R,n}$)**; the third harmonic contained in the mains voltage feed-forward signal for (b) is not affecting the shape of $\bar{u}_{U,R}'$ but only the selection of the switching states employed for the formation of $u_{U,R}'$; Simulation parameters: $U_{N,rms}$=230V ($\hat{U}_N$ =327V), U_{OY}=400V, L= 540µH, f_P= 12.5kHz , P_0= 10kW, symmetric mains (see Section 3); in order to reduce the simulation time a low switching frequency has been selected where the inductance L has been increased accordingly.

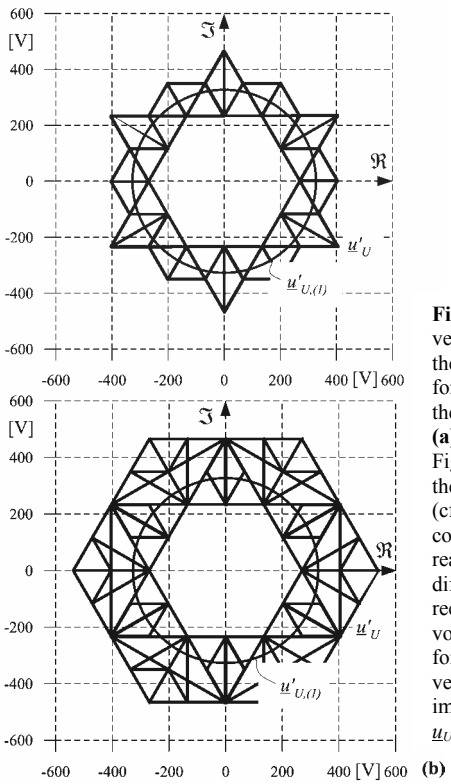


Fig.7: Voltage space vectors $\underline{u}_U'$ employed for the formation of $\underline{u}_{U,(1)}$ and/or for the sinusoidal control of the mains phase currents for **(a)** and **(b)** according to Fig.6. The lines connecting the voltage space vectors (cf. Fig. 3) are due to the continuous transitions of the real system between the different levels of the rectifier input phase voltages $u_{U,i}$. The voltage formation is partly by space vectors which are not immediately neighbouring $\underline{u}_{U,(1)}$ (cf. Fig.6).

According to **Fig.6**(a), a low ripple of the mains phase currents results for direct mains voltage feed-forward, and/or for purely sinusoidal shape of the feed-forward signal, where the high frequency harmonics are located at multiples of $2f_P$ due the interleaved operation of S_{i+} and S_{i-}. The pulse width modulation is not far from optimum, as for the current control largely voltage space vectors $\underline{u}_U'$ in the immediate vicinity of $\underline{u}_{U,(1)}$ are employed (cf. **Fig.7**(a)).

However, for given output voltage U_{OY} and for neglection of the fundamental voltage drop $\underline{u}_{L,(1)}$ across the input inductors L, i.e. for

$$\underline{u}_{U,(1)} \approx \underline{u}_N \tag{14}$$

and/or for $\hat{U}_U \approx \hat{U}_N$ a purely sinusoidal feed-forward signal does allow a system operation only for $\hat{U}_N < U_{OY}$ and/or for a modulation index M<1,

$$M = \frac{\hat{U}_U}{U_{0Y}}. \tag{15}$$

In order to increase the modulation range to the theoretically maximum value

$$M_{\max} = \frac{2}{\sqrt{3}}, \tag{16}$$

(cf. Fig.3), which is equal to a rectifier input voltage fundamental of amplitude $\hat{U}_{U,max} = 2/\sqrt{3}\ U_{OY}$, the mains voltage feed-forward has to be extended (in the simplest case) by a third harmonic of amplitude $^1/_6\hat{U}_N$. As a simulation of the system behavior shows (cf. Fig.6(b)), the phase currents are then again shaped sinusoidally. However a larger difference of

the employed voltage space vectors and the trajectory of $\underline{u}_{U,(1)}$ occurs what results in a higher ripple of the mains current.

With reference to Fig.3 also for fully utilizing the modulation range a voltage formation by space vectors immediately neighbouring $\underline{u}_{U,(1)}$ should be possible. The calculation of an according feed-forward signal minimizing the switching frequency harmonics of the mains voltage is currently the topic of further research.

In contrast to the Y-Rectifier, for the Vienna Rectifier only 7 voltage space vectors $\underline{u}_{U}'$ are available for each combination of signs of the phase currents (cf. Fig.3, [4]). Accordingly, for equal pulse frequency and equal input inductance a higher average difference of applied voltage vectors $\underline{u}_{U}'$ and the ideal trajectory $\underline{u}_{U,(1)}$ occurs what results in a higher current ripple.

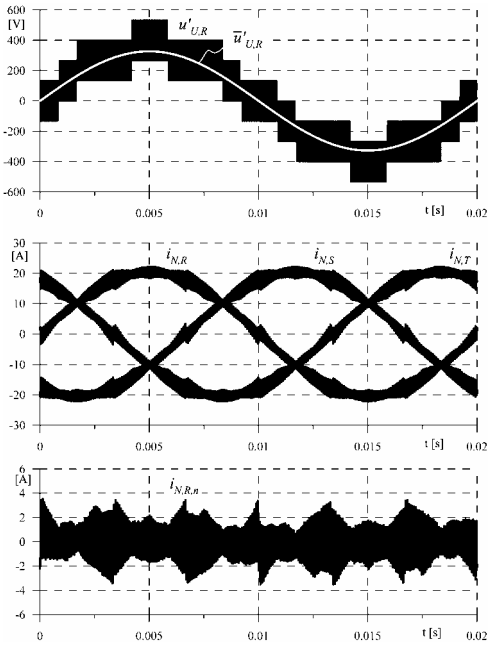


Fig.8: Simulation of the stationary behavior of a Vienna Rectifier; representation of the results as for the Y-Rectifier (cf. Fig.6(b)). For the realization of a phase current control only a single carrier signal i_D is required, as both transistors S_{i+} and S_{i-} of a bridge leg are controlled simultaneously. Simulation parameters as for Fig.6, but U_O=800V; for utilizing the full modulation range the mains voltage feed-forward is again extended by a third harmonic; in contrary to the Y-Rectifier this however does result in a reduction of the mains current ripple as compared to direct (purely sinusoidal) mains voltage feed-forward [9].

For ensuring an equal rectifier input voltage range, the partial output voltage of the Vienna Rectifier has to be set to the Y-Rectifier phase module output voltage level,

$$U_{0Y} = \tfrac{1}{2} U_0 \,. \tag{17}$$

For defining the Vienna Rectifier modulation index as

$$M = \frac{\hat{U}_U}{\tfrac{1}{2} U_0} \,, \tag{18}$$

both systems are operating at the same modulation index for given rectifier voltage fundamental amplitude $\hat{U}_U$. This allows a direct comparison of the resulting RMS values of the mains current ripple components as shown in **Fig.9**.

According to Fig.9, for operation at high modulation index the input inductance of the Y-Rectifier can be reduced by ≈30% as compared to the Vienna Rectifies for equal RMS value of the mains current ripple. This results in a lower weight and/or higher power density of the system. In this connection one also has to note that in contrast to the Y-Rectifier the spectrum of the Vienna Rectifier mains phase current ripple contains harmonics also at single switching frequency (cf. [10]) and that the voltage being switched is twice the partial Y-Rectifier output voltage (cf. (17)) what causes a higher EMI filtering effort.

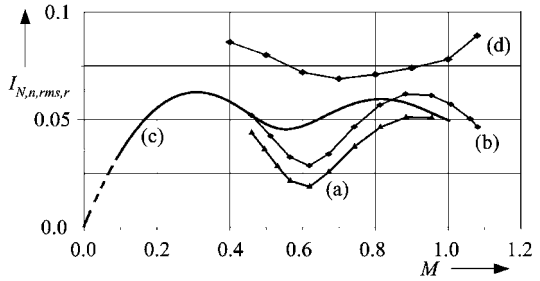


Fig.9: Normalized RMS value $I_{N,n,rms,r}$ of the ripple component $i_{N,n}$ of a mains phase current i_N of the Y-Rectifier in dependency on the modulation index M for average current mode control according to Fig.5; **(a)** direct (sinusoidal) mains voltage feed-forward (cf. Fig.6(a)); **(b)** extension of the mains voltage feed-forward by a third harmonic (cf. Fig.6(b)); furthermore shown: **(c)** $I_{N,n,rms,r}$ resulting for a connection of the star point N' (cf. Fig.1) of the phase modules with the mains star point N and **(d)** characteristic of the Vienna Rectifier for mains voltage feed-forward extended by a third harmonic (cf. Fig.8, $U_O/2 = U_{OY}$). Normalization basis: $U_O T_P/(\delta L)$, T_P denotes the pulse period.

3. Stresses on the Components

As shown in [11] the current stresses on the power components of a PWM rectifier system can be derived by analytical calculations based on local and global averaging, i.e. averaging over a pulse period and a mains period, of the discontinuous switching frequency currents.

For limiting to the essentials a purely sinusoidal mains current lying in phase with the corresponding mains phase voltage is assumed and the ripple of the output voltage with amplitude $\hat{U}_{OY,(2)}$ and twice the mains frequency is neglected. Furthermore, only purely sinusoidal modulation (direct mains voltage feed-forward) is considered, as the injection of a third harmonic takes only a minor influence on the component current stresses [5].

The results of the calculations (which are omitted here for the sake of brevity) are compiled in **Fig.10** and provide a basis for the dimensioning of the main system components. There, one has to set the mains current amplitude as

$$\hat{I}_N = \frac{\sqrt{2}}{\sqrt{3}} \frac{P_O}{\eta \, U_{N,l-l,rms}} \tag{19}$$

in order to consider the system losses which have been neglected for the analytical calculation ($\eta = \eta_{AC/DC} \, \eta_{DC/DC} \approx$

0.92…0.93 denotes the overall efficiency of the power supply modules, $U_{N,l\text{-}l,rms}$ is the RMS value of the mains line-to-line voltage).

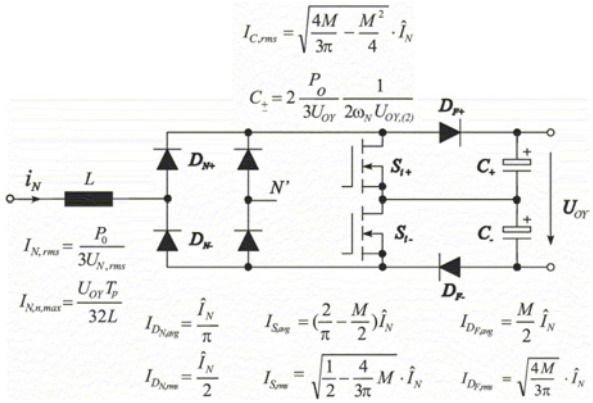


Fig.10: Results of the analytical calculation of the current stresses on the power components of the Y-Rectifier. For a comparison to the characteristic values of the Vienna Rectifier the output voltage U_{OY} of a phase module has to be considered equal to a partial output voltage ½U_O of the Vienna Rectifier (cf. (17)).

For realizing a wide input voltage range telecom power supply module, the Y-Rectifier output voltage has to be selected as

$$U_{0Y} > \frac{\sqrt{3}}{2}\hat{U}_{N,\max} = \frac{1}{\sqrt{2}}U_{N,l-l,rms,\max} \qquad (20)$$

under consideration of the modulation limit (cf. (16)). For $U_{N,l\text{-}l,rms}$ = 320…530V this results in U_{0Y} > 375V and/or U_{0Y} = 400V under consideration of a control margin. For an output power of the power supply module of P_O = 10kW and an assumed efficiency of η = 0.92 we then have for rated mains voltage $U_{N,l\text{-}l,rms}$= 400V for the current stresses

$\hat{I}_N$ = 22.2A,
$I_{DN,avg}$ = 7.1A,
$I_{DF,avg}$ = 9.0A,
$I_{Si+,rms} = I_{Si-,rms}$= 8.7A,
$I_{C+,rms} = I_{C-,rms}$= 9.3A,
$I_{N,n,max}$ = 0.93A

($I_{N,n,max}$ denotes the maximum value of the mains current ripple occurring within a mains period).

Assuming a maximum admissible phase module output voltage ripple of $\hat{U}_{OY,(2)}/U_{OY}$= 2%,

C_+=C_-=3.6mF

has to be selected for the output capacitors. According to a detailed dimensioning which is omitted here for the sake of brevity, for employing power transistors STU26NM50 (ST, 26A/500V blocking capability) and power diodes 15ETH03 (IRF, 15A/300V blocking capability) for the realization of $S_{i\pm}$ and $D_{F\pm}$ and assuming a switching frequency of f_P=50kHz (L=270µH) the efficiency of the Y-Rectifier at rated voltage and rated power is

$\eta_{AC/DC} \approx$ 96.5%

what is also resulting for a Vienna Rectifier of equal rated power and about equal realization effort of the power circuit.

4. System Control

The control of a three-level Y-Rectifier has to define the input phase current reference values according to a symmetric ohmic loading of the mains and has to maintain the output voltages of the rectifier phase modules, i.e. the DC link voltages $U_{OY,i}$ at a given level U_{OY}*. Furthermore, a symmetric distribution of each DC link voltage $U_{OY,i}$ to the corresponding output capacitors $C_{+,i}$ und $C_{-,i}$ has to be ensured. There, the system should continue in operation also for heavily unbalanced mains and/or for a failure of a mains phase.

A control concept meeting the aforementioned requirements is shown in **Fig.11**, where the input reference conductance G* is set by the power supply output voltage control in dependency on the mains voltage condition. The reference value of an input phase current $i_{N,i}$ is then calculated by multiplication of G* with the zero-sequence-free component $u_{N,i}'$ of the corresponding mains phase voltage derived from a star connection of equal resistors [12] and set by an underlying average current mode controller. There, a limitation of G* ensures that the phase current amplitude does not exceed an admissible maximum value $\hat{I}_{N,max}$ according to the dimensioning of the system.

The output power of a DC/DC converter stage connected to a rectifier phase module output $U_{OY,i}$ is defined to be equal to the module input power resulting for G* and $u_{N,i}'$ by properly defining the DC/DC stage output current $i_{out,i}$*. Therefore, the DC link voltage $U_{OY,i}$ ideally should remain at a constant level. However, due to the losses of the real system a control of $U_{OY,i}$ has to be provided which adapts the reference conductance G* for all phases by ΔG* (cf. Fig.11) in dependency on the control error of the mean value $^1/_3(U_{OY,R}+U_{OY,S}+U_{OY,T})$ of the DC link voltages. A remaining control error U_{OY}*−$U_{OY,i}$ of an individual DC link voltage $U_{OY,i}$ is then controlled by a final individual correction ΔG_i* of G*+ ΔG* (cf. Fig.11, [13]) .

Due to the missing connection of the star point N' of the rectifier modules and the mains neutral N the individual DC link voltage control circuits are mutually coupled. Therefore, e.g. an increase of the conductance in phase R by ΔG_R* does not result in an increase but in a reduction of the output power of the rectifier module and/or of $U_{OY,R}$ and furthermore tends to increase $U_{OY,S}$ and $U_{OY,T}$. This can be explained by the fact that the realization of ΔG_R* would require a current $i_{N,R}$* which is not in correspondence with $i_{N,R}$*+$i_{N,S}$*+$i_{N,T}$* =0. For controlling $i_{N,R}$ to $i_{N,R}$* the current controller in phase R increases the power transistor relative turn-on time, while the current control in phases S and T increases the turn-off time of the corresponding power transistors resulting in an increase of $u_{U,S}'$ and $u_{U,T}'$ in order to prevent an increase of $i_{N,S}$ and $i_{N,T}$ by the reduced voltage $u_{U,R}'$ in phase R. For a P-type control of the DC link voltages $U_{OY,i}$ this finally results in a symmetric distribution of the mains voltage to the inputs of the phase modules according to a symmetric three-phase ohmic load.

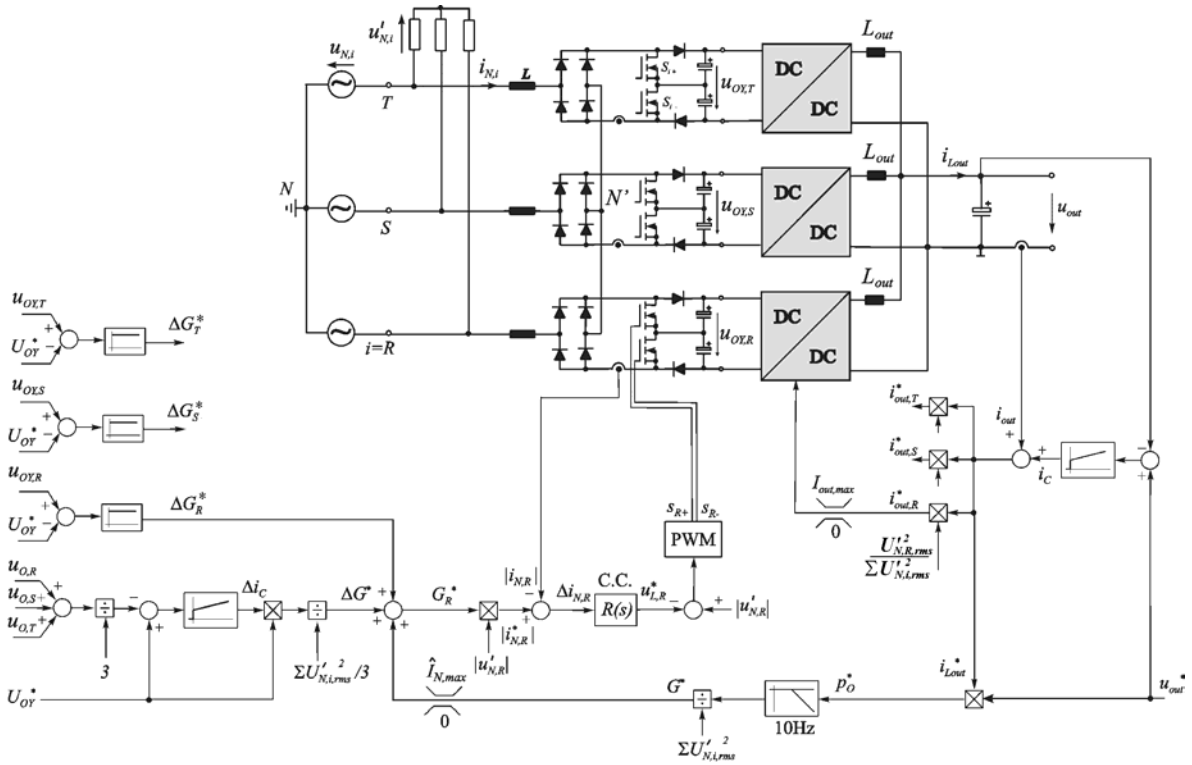


Fig.11: Control of a three-phase telecom power supply module for realization of the input stage by a Y-Rectifier [13]. The input conductance reference value G^* of the rectifier stage is defined by the control of the power supply module DC/DC converter output stage which is formed by a parallel connection of three individual DC/DC converters supplied by the Y-Rectifier phase modules. The power drawn from an Y-Rectifier phase module output $u_{OY,i}$ is set equal to the module input power $P_{0,i} = G^* . U_{N,i,rms}{}'^2$ resulting for G^* (the mains phase voltage information $u_{N,i}'$ is derived with reference to an artificial mains neutral point formed by a star connection of equal resistors). In order to ensure the DC link voltage level required for input current control despite system losses, furthermore a control of the average value of the output voltages $u_{OY,i}$ is provided, resulting in a correction ΔG^* of G* by being equal for all phases; a minor correction of the input conductance with respect to a remaining control error is then provided by individual P-type controllers for each phase (shown only for phase R, cf. ΔG_R^*); the resulting conductance G_R^* defines the mains phase current reference value which is set by an underlying average current mode controller (cf. Fig.5). For the sake of clarity the balancing of the partial output voltages of the phase modules is not shown.

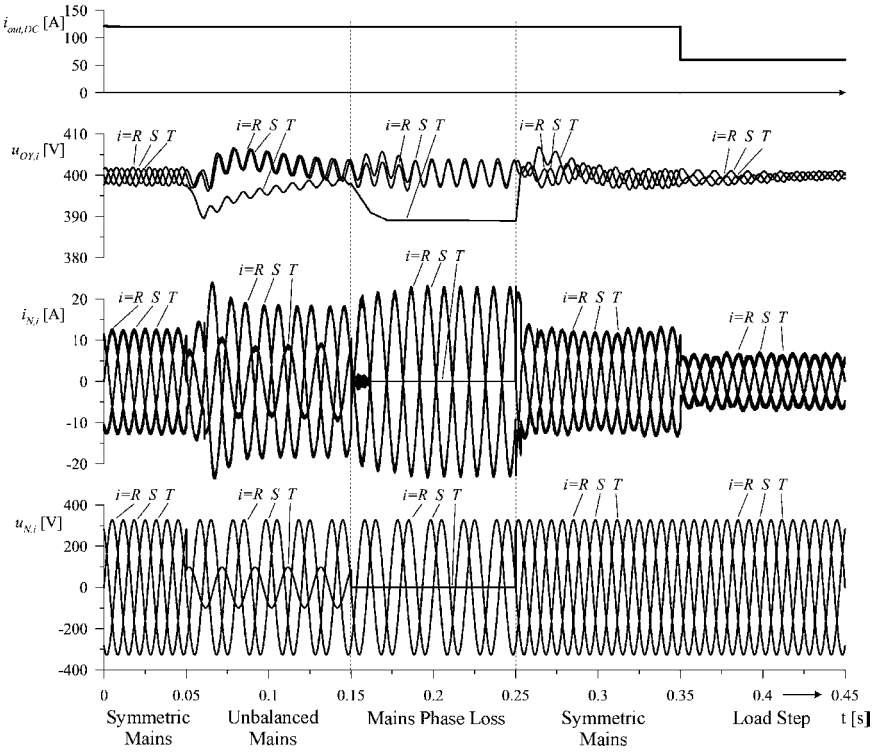


Fig:12: Digital simulation of the behavior of the Y-Rectifier controlled according to Fig.11 for symmetric mains, mains voltage unbalance, mains phase loss and load step. Shown are: mains phase voltage $u_{N,i}$ (with reference to the mains neutral point N), mains phase currents $i_{N,i}$, output voltages $u_{OY,i}$ of the phase modules, load current i_{out} of the parallel connection of DC/DC converters supplied by the Y-Rectifier. Simulation parameters: $U_{N,rms}$=230V ($\hat{U}_N$ =327V), U_{OY}*=400V, L= 1.35mH, f_P= 10kHz , P_0= 6.2 kW; in order to reduce the simulation time a low switching frequency has been selected.

A more detailed analysis of the control-oriented system behavior will be given in a future paper, therefore, a further discussion should be omitted here for the sake of brevity.

The stationary and dynamic control behavior is shown in **Fig.12**. For stationary operation and symmetric mains the DC link voltages $u_{OY,i}$ are controlled to U_{OY}*=400V with the exception of the variation with two times the mains frequency occurring in principle for single phase PWM rectifier systems. In case of a step-like reduction of the amplitude of a mains phase voltage ($u_{N,T}$ at t=50ms) due to the mains voltage feed-forward employed in the phase current control (cf. Fig.5) only a minor disturbance of the module output voltages occurs. This also holds for a failure of a mains phase, e.g. $u_{N,T}$ at t=150ms, where the module connected to phase T and the DC/DC converter connected in series are turned off in case the DC output voltage reaches a given lower limit; when $u_{N,T}$ returns, the module (and the DC/DC converter) are turned on again after the pre-charging of the output capacitors has been completed. There, the mains phase currents $i_{N,i}$ show a sinusoidal shape proportional to the corresponding zero sequence free mains phase voltage $u_{N,i}'$; accordingly, unity power factor operation is guaranteed independent of the mains condition. Also a load step at the output of the DC/DC converter stages (at t=350ms) takes only little influence on the DC link voltage as G* provides a feed-forward of the output power.

5. Conclusions

As this paper shows, a star-connection of three-level single-phase PWM rectifier systems (Y-Rectifier) can be advantageously utilized for realizing the input stage of a three-phase telecommunications power supply module with comparable power density and efficiency as for employing a direct three-phase PWM (Vienna) rectifier approach.

The main advantages of the concept are the low DC output voltage level of the phase modules, low EMI emissions due to the relatively low value of the switched voltage and high modularity (manufacturability, testability). The relatively high control complexity can be seen as disadvantage which, however, is of low importance as the control of future power supply systems will be realized in fully digital form.

In the course of further research the theoretical results will be experimentally verified and a final comparative evaluation of the Y-Rectifier and the Vienna Rectifier concept will be performed based on measurements and the filtering effort required for guaranteeing compliance to EMI standards. Furthermore, the pulse width modulation will be optimized concerning the RMS value of the mains current ripple and a control concept proposed in [1] for the symmetric distribution of the total output power to the phase modules of a two-level Y-Rectifier will be analyzed concerning stability and control dynamics.

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