Experimental Analysis of a 10kW Wide Input Voltage Range Modular Three-Phase Unity Power Factor PWM Δ-Rectifier

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Abstract.

The three-phase three-level Δ-*Rectifier* is formed by a delta-connection of single-phase three-level PWM rectifier modules and does provide the full rated output power also in case of a mains phase loss. Furthermore, the system shows a low harmonic content of the mains phase currents if the modulation is with respect to the formation of a maximum zero-sequence component of the module input current ripples which circulates inside the delta connection and does not take influence on the phase current formation. This concept has been proposed based on theoretical considerations and digital simulations and is verified in this paper experimentally at the example of a 10kW laboratory prototype of the Δ-*Rectifier*. The influence of non-idealities of the practical realization on the current ripple formation is analyzed and a high input current quality of the system is demonstrated. Finally, a star-connection of the three-level PWM rectifier modules, i.e. the *Y-Rectifier* is proposed and discussed briefly. As compared to the Δ-*Rectifier*, the *Y-Rectifier* is expected to allow a further increase of the power density and the efficiency and therefore will be treated in the course of the continuation of the research.

1 INTRODUCTION

For the realization of a three-phase boost-type PWM rectifier system a direct three-phase concept, i.e. the *VIENNA Rectifier* (cf. Fig.1(b) in [1]) or a delta-connection of three single-phase PWM rectifier modules, i.e. a Δ-*Rectifier* (cf. **Fig.1** and/or Fig.12 in [1]) could be employed. There, in case of a mains phase loss the full rated power is available without overdimensioning only for the Δ-*Rectifier* if the single-phase bridge rectifier input stages are replaced by three-phase thyristor bridge circuits which allow to switch over all line-to-line modules to the two remaining phases (cf. Fig.1). Furthermore, the Δ-*Rectifier* does allow to achieve a lower RMS value of the mains current ripple as compared to a *VIENNA Rectifier* employing input inductors of equal volume (cf. Fig.3 in [2]). This is due to the formation of a zero-sequence component of the line-to-line module input current ripples which does circulate inside the delta-connection and does not take influence on the formation of the ripple of the mains phase currents. The low harmonic content of the mains current is immediately obvious also from the large number of space vectors of the equivalent rectifier input phase voltages of a Δ-*Rectifier* which are determining the formation of the input current in combination with the mains phase voltages (cf. **Fig.2** and/or Fig.2 in [1]).

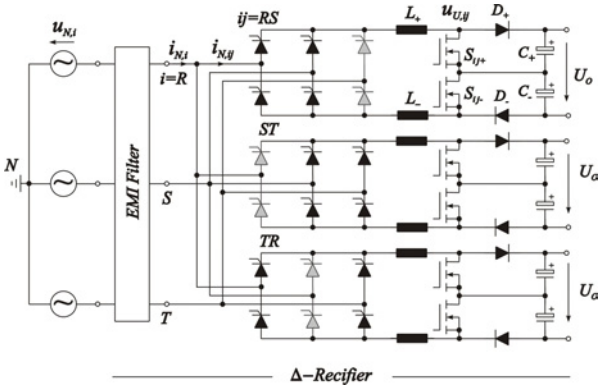


Fig.1: Basic structure of the power circuit of the three-level Δ-*Rectifier* according to Fig.1(a) in [1].

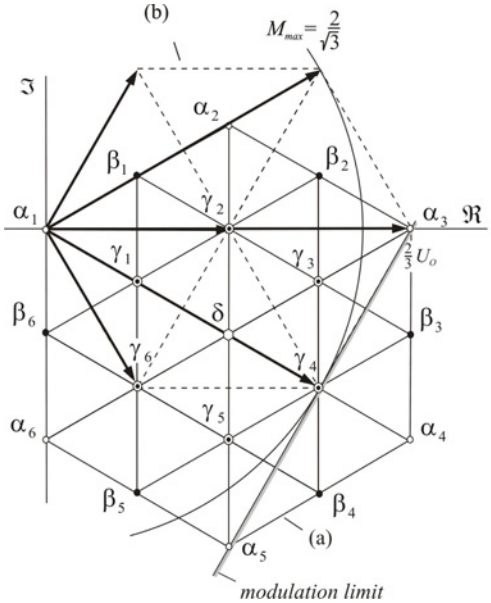


Fig.2: Space vectors of the rectifier input phase voltages $u_{U,i}'$ of an equivalent star-connection of the Δ-*Rectifier* (cf. **(a)** and Fig.2 in [1]); the voltages $u_{U,i}'$ are determining the input phase currents $i_{N,i}$ in combination with the mains phase voltages $u_{N,i}$. Furthermore shown: Input voltage space vectors **(b)** of the *VIENNA Rectifier*. Both rectifier systems show 9 different levels of the rectifier input phase voltages, however for the Δ-*Rectifier*

a reference space vector can be formed with lower deviation what does result in a lower switching frequency ripple of the input phase currents. Concerning the correspondence of the space vectors α_i, β_i, γ_i, δ to the rectifier switching states and the switching state redundances see Fig.2 in [1].

However, the transfer of part of the ripple current of a line-to-line module into a zero sequence component and/or the low ripple of the input phase currents up to now has only been considered theoretically and/or demonstrated by digital simulations.

Therefore, in this paper the concept shall be verified experimentally at the example of a 10kW laboratory prototype of the Δ-*Rectifier* being designed for $400V_{rms}$ line-to-line input and $800V_{DC}$ output. There, the influence of non-idealities introduced by the practical realization like, e.g., offsets and/or asymmetries of the PWM carrier signals, turn-on and turn-off delay times of the power transistor gate drive circuits and the non-linearity of the iron powder core input inductors is of special interest. For controlling the module input currents a concept is employed which does not require a multiplication of the reference input conductance value and of the rectifier mains line-to-line voltages and does not rely on a mains voltage pre-control (cf. **Section 2** and/or Fig.I.1 in [3]). In **Section 3** results of the experimental analysis are compared with digital simulations of the time behavior of the ripple components of the line-to-line module input currents $i_{N,ij}$, *ij=RS, ST, TR,* and input phase currents $i_{N,i}$, $i = R, S, T$ (cf. Fig.1) and the origin of minor deviations will be discussed. Finally, in **Section 4** topics to be treated in the continuation of the research will be outlined briefly.

2 MODULE INPUT CURRENT CONTROL

For ensuring a low realization effort a current control concept which (in contrast to conventional average current mode control) does not rely on a multiplication of a reference conductance with the absolute value of the respective mains line-to-line voltage is employed for the module input current control [3]. As shown in **Fig.3**, there the boost inductor current $|i_{N,ij}|$ is directly compared with switching frequency triangular carrier signals which are interleaved in order to utilize the three-level module characteristic, accordingly, harmonics of $i_{N,ij}$ do ideally occur only in the vicinity of multiples of twice the switching frequency.

There, the turn-off time of the power transistors and, therefore, the local average value $\bar{u}_{ij}$ of the voltage across the power transistors S_+ and S_- shows a proportional relationship to $|i_{N,ij}|$ for operation in the continuous conduction mode. Therefore, with rising current $\bar{u}_{ij}$ does increase until it balances the local mains voltage $|u_{N,ij}|$,

$$\left|u_{N,ij}\right| = \bar{u}_{ij} = d' u_0 = \frac{\left|i_{N,ij}\right|}{\hat{I}_D} u_0 \,. \tag{1}$$

Accordingly, the system shows an ohmic input characteristic

$$\left|i_{N,ij}\right| = \frac{\hat{I}_D}{u_0}\left|u_{N,ij}\right| \tag{2}$$

where the reference value of the conductance can be defined (for constant output voltage U_O) by the amplitude of the carrier signals,

$$G^* = \frac{\hat{I}_D}{u_0}\,, \tag{3}$$

which can be varied with low circuit realization effort. The line-to-line module input current, the input current ripple and characteristic voltages resulting from a digital simulation of the current control concept are depicted in **Fig.4**.

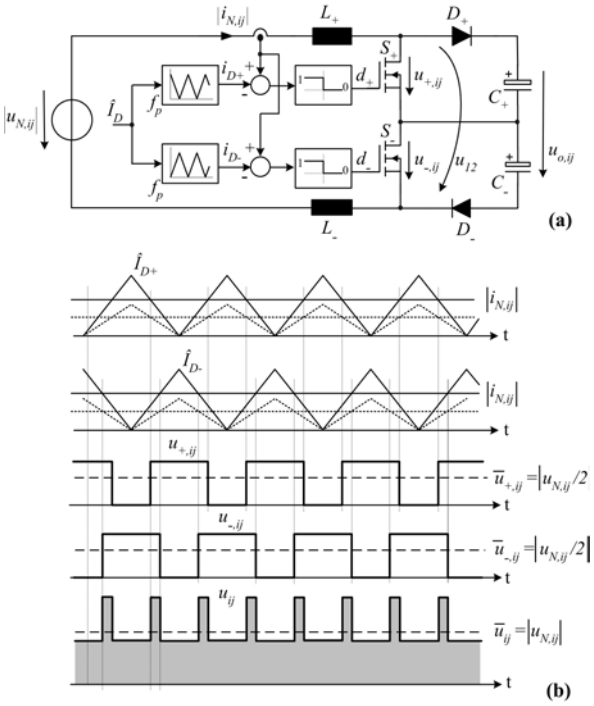


Fig.3: Basic structure of the power circuit of a three-level line-to-line module of the Δ-*Rectifier* **(a)** and derivation of the control signals of the power transistors S_+ and S_- **(b).** Furthermore shown: Resulting time behavior of the voltages $u_{+,ij}$ and $u_{-,ij}$ across S_+ and S_- and of the total transistor voltage $u_{ij} = u_{+,ij} + u_{-,ij}$. Dependent on the amplitude of the triangular carrier signal a given time behavior of u_{ij} is achieved for different inductor current levels; accordingly, the equivalent input conductance of the circuit is defined (for constant output voltage U_O) directly by the triangular carrier amplitude $\hat{I}_{D+}=\hat{I}_{D-}$.

3 EXPERIMENTAL ANALYSIS

The experimental analysis of the Δ-*Rectifier* is based on a laboratory prototype with the following parameters:

Rated power	$P_O = 10.5$ kW
Input voltage range	$U_{N,l\text{-}l} = 320V\ldots530V_{rms}$
Module output voltage	$U_O = 800V_{DC}$
Switching frequency	$f_P = 50$kHz (for S_+ and S_-)
Module input inductors	$L_+ = L_- = 420\mu$H (iron powder cores).

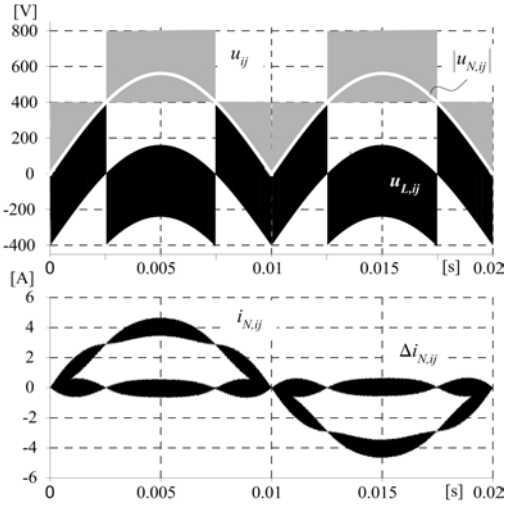


Fig.4: Digital simulation of the time behavior of u_{ij}, of the rectified line-to-line mains voltage $|u_{N,ij}|$ and of the inductor voltage $u_{L,ij} = u_{L+,ij} + u_{L-,ij}$. Furthermore shown: line-to-line module input current $i_{N,ij}$ and switching frequency ripple $\Delta i_{N,ij}$ of $i_{N,ij}$.

The system is supplied with a symmetric three-phase voltage system generated by a three-phase high power linear amplifier. For each module an output voltage control and an underlying input current control is provided (cf. Fig.3). The system represents a symmetric ohmic load to the mains, where the reference value G^* of the input conductance is defined by a low-cost µC in the form of a PWM signal $PWM\_\hat{I}_D$; furthermore, the µC defines the switching frequency f_P and does balance the module partial output voltages by an opposite shift (offset) of the triangular carrier signals i_{D+} and i_{D-} (cf. **Fig.5**). Due to the high dynamics the current control is realized in analogue technique.

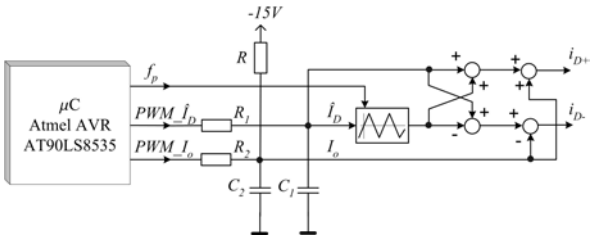


Fig.5: Basic structure of the control of a line-to-line module. Due to the low dynamics the control of the output voltage is performed by a low-cost µC. There the amplitude of the triangular carrier signals i_{D+} and i_{D-} is defined by the duty cycle (average value) of the PWM signal $PWM\_\hat{I}_D$. The opposite shifting of the carrier signals for balancing the partial output voltages is implemented in a similar way. The input current control is realized in analogue technique.

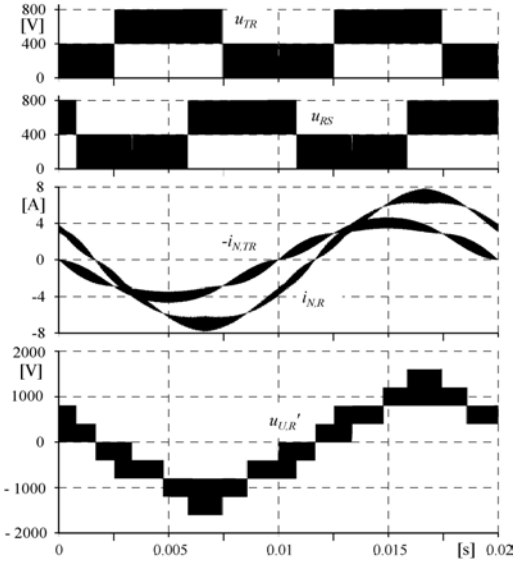
According to **Fig.6** and **Fig.7** the results of a digital simulation of the system behavior are fully verified by the experimental analysis. The phase current forming equivalent rectifier input phase voltage $u_{U,i}'$ (cf. Fig.2 in [2]) resulting for the combination of the line-to-line modules shows an approximately sinusoidal shape (cf. Fig.6). Therefore, the input phase current contains a ripple component of only low amplitude despite the relatively low input inductance value. This can be clearly seen also from Fig.7. The zero-sequence component Δi_0 of the line-to-line input current ripple,

$$\Delta i_0 = \frac{1}{3}(\Delta i_{N,RS} + \Delta i_{N,ST} + \Delta i_{N,TR}) \tag{4}$$

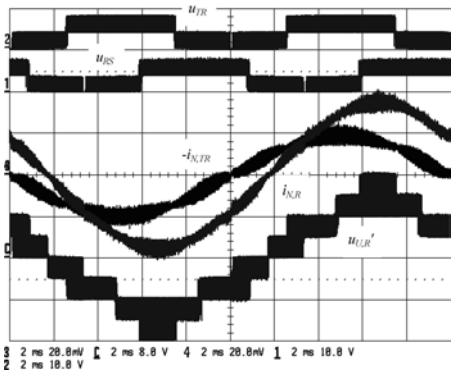
($\Delta i_{N,ij} = \Delta i_{N,ij}' + \Delta i_0$), is circulating inside the delta connection and, therefore, does not take influence on the ripple of the mains phase currents, i.e. the zero-sequence ripple components Δi_0 of two line-to-line module input currents do cancel each other in the formation of a mains phase current

$$\Delta i_{N,R} = \Delta i_{N,RS} - \Delta i_{N,TR} = (\Delta i_{N,RS}' + i_0) - (\Delta i_{N,TR}' + i_0) = \Delta i_{N,RS}' - \Delta i_{N,TR}' \tag{5}$$

(shown at the example of phase R). Accordingly, the mains phase current shows a ripple comparable to the module input current ripple (cf. also **Fig.14**) what does result in a low effort for filtering of differential mode EMI.

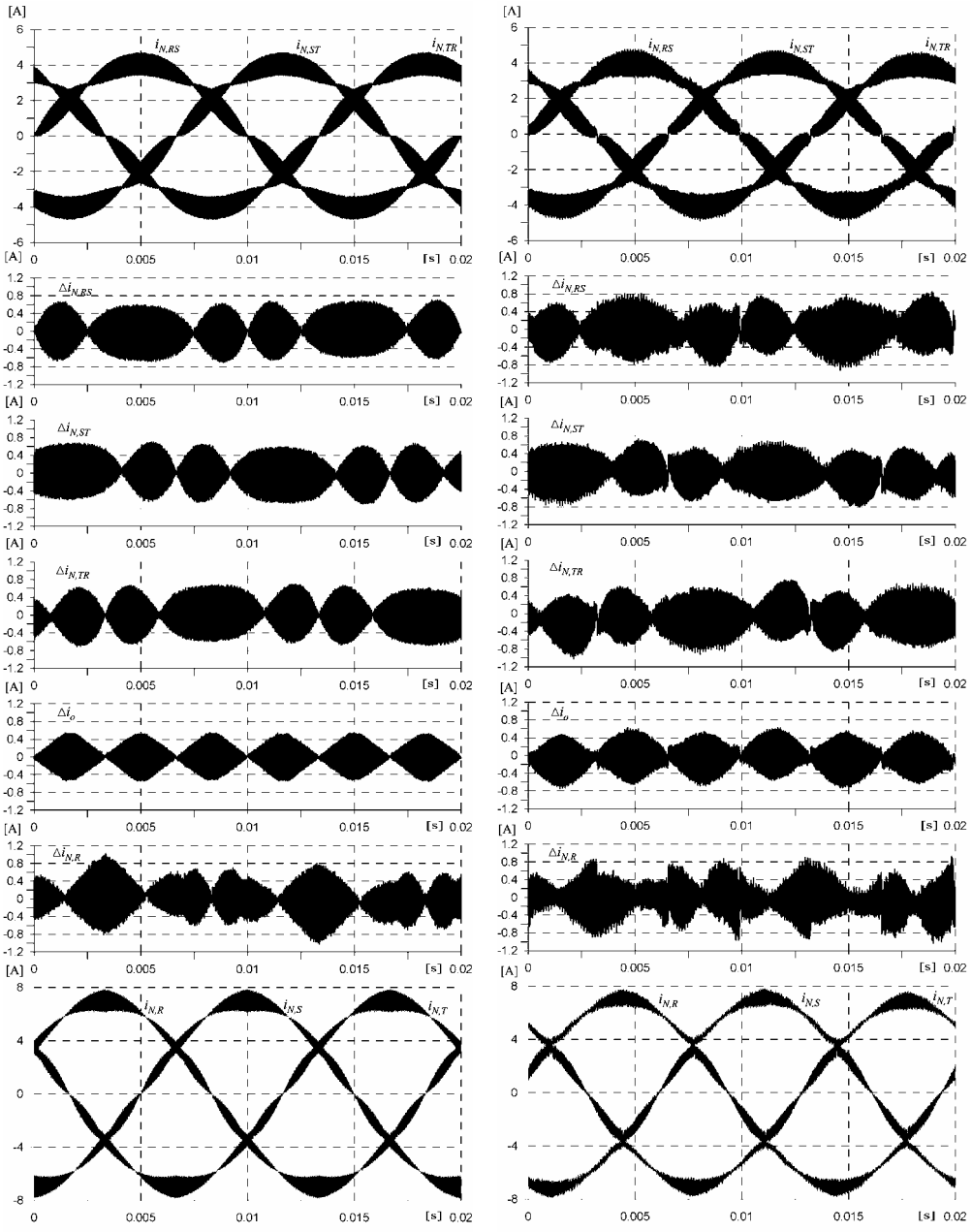


(a)



(b)

Fig.6: Digital simulation **(a)** and experimental determination **(b)** of the time behavior of the voltages across the power transistors of the line-to-line modules *RS* and *TR*, u_{RS} und u_{TR} , of the module input current $-i_{N,TR}$, of the mains phase current $i_{N,R}$ and of the equivalent rectifier input phase voltage $u_{U,R}'$ which does determine the input phase current $i_{N,R}$ in combination with the mains phase voltage $u_{N,R}$ (cf. Fig.2(b) in [2]).



(a) **(b)**

Fig.7: Digital simulation **(a)** and experimental determination **(b)** of the time behavior of the line-to-line module input currents $i_{N,ij}$, of the ripple components $\Delta i_{N,ij}$ of $i_{N,ij}$, of the zero-sequence component Δi_0 of $\Delta i_{N,ij}$ circulating inside the delta-connection, of the ripple $\Delta i_{N,R}$ of the main phase current $i_{N,R}$ and of the main phase currents $i_{N,i}$ within a mains period for P_O=3.4kW.

According to **Fig.8** the ripple components of the line-to-line module input currents and of the mains phase currents, $\Delta i_{N,i}$ und $\Delta i_{N,ij}$, do contain harmonics (of low amplitude) with single switching frequency f_P. For ideal system operation due to the interleaving of the power transistor control signals of each module harmonics only should be present in the vicinity of multiples of $2f_P$ (cf. Fig.8). As a more detailed analysis clarifies, the non-ideal behavior is caused partly by an asymmetry or offset of the PWM carrier signals, by different turn-on and turn-off delay times of the gate drive circuits, by asymmetries of the line-to-line modules, by the non-linearity of the iron powder core input inductors and by the discontinuous inductor current operation occurring in the vicinity of the module input current zero crossings (cf. **Fig.9**).

As the experimental analysis shows (cf. **Fig.10**(a)) a finite ripple of the line-to-line module input current with single switching frequency does occur for $|u_{N,ij}| = u_O/2$ due to slightly different turn-on and turn-off delay times of the gate drive circuits of the power transistors S_+ und S_-. The voltage u_{ij} across the power transistors does not remain at $u_{ij}=u_O/2$ but does also assume $u_{ij} = u_O$ and $u_{ij} = 0$ what does result in a step-like change of $|i_{N,ij}|$.

A further disturbance of the mutual cancellation of the harmonics of $u_{+,ij}$ and $u_{-,ij}$ with single switching frequency does result from a minor difference of the amplitudes of the carrier signals i_{D+} and i_{D-}, e.g., the module input current does show a ripple with single switching frequency in the vicinity of the zero crossing (cf. Fig.10(b)).

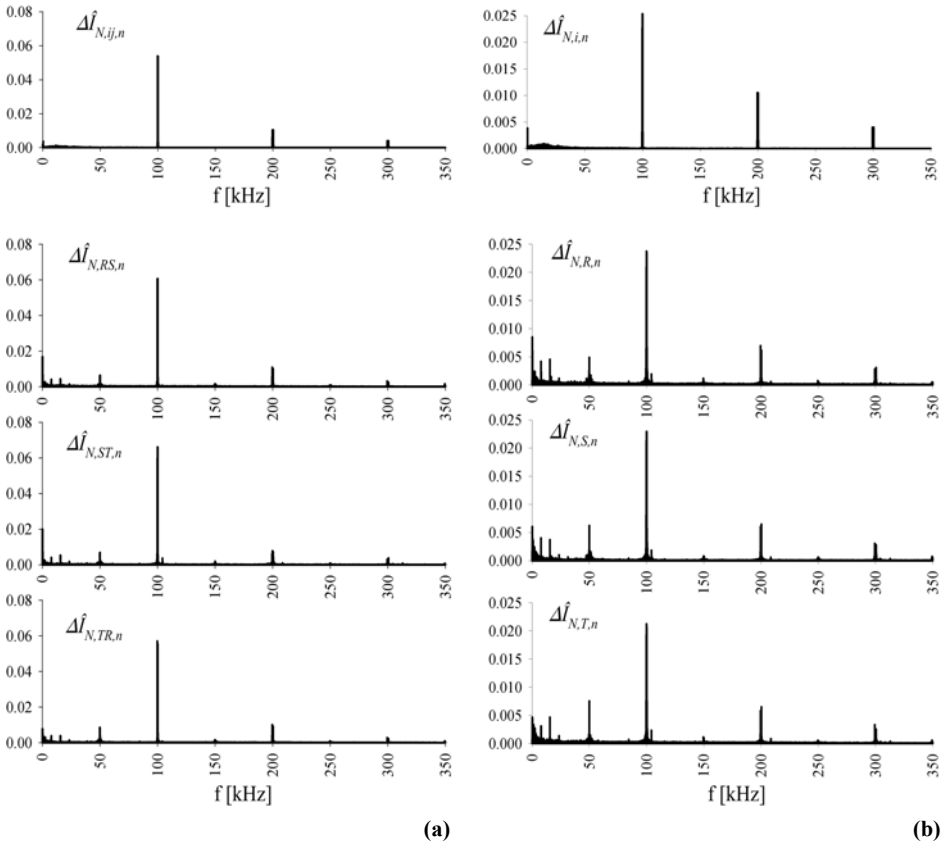


Fig.8: Normalized spectra (normalized with reference to the fundamental) of the measured ripple components of the line-to-line module input currents **(a)** and of the mains phase currents **(b)**. Furthermore shown (top): Spectrum resulting from digital simulation (identical for all line-to-line modules and/or phase currents).

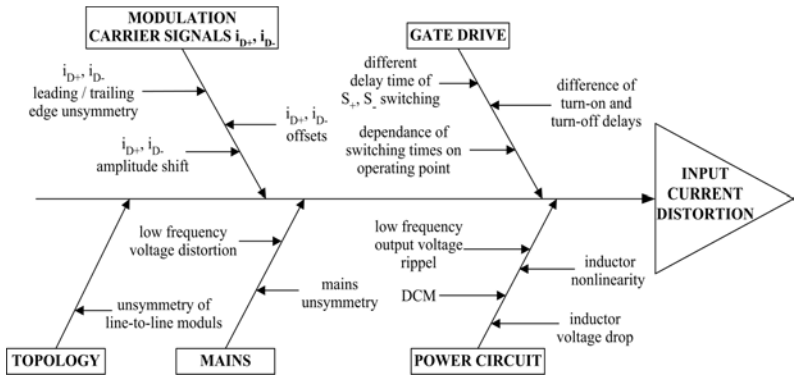


Fig.9: Possible sources (fishbone diagram) of a switching frequency or low frequency distortion of a line-to-line module input current.

It is important to note that for the current control concept employed in the case at hand (cf. **Fig.11**(a)) a non-ideality of the carrier signals, of the gate drive circuits or of the power circuit does take direct influence on the input current quality. Therefore, a high linearity and symmetry and low offset of the PWM carrier signals and equal turn-on and turn-off switching delay times have to be considered for the practical realization. In contrast, e.g. for conventional average current mode control (cf. Fig.11(b)) the non-idealities of the PWM and/or of the gate drive circuits are largely suppressed by the explicit current controller performing a comparison of the actual and the reference current shape.

According to **Fig.12**, the measured RMS value of the ripple current shows only a minor deviation from the results of digital simulations and/or from analytical calculations (cf. Fig.5 in [1]) despite the non-idealities introduced by the practical realization. For equal values of the input inductors, i.e. for $L=1/3L_{\Delta}=1/3(L_{+}+L_{-})$ (cf. Eq.(7) in [2]), the Δ-*Rectifier* is characterized by a considerably lower mains phase current ripple RMS value $\Delta I_{N,rms}$ than the *VIENNA Rectifier*. Furthermore, the Δ-*Rectifier* mains phase currents show a remarkably high quality; after filtering of harmonics with switching frequency the remaining total harmonic current distortion is only $THD_I \approx 2\%$ for $P_0 \geq 2.5$kW (purely sinusoidal supply mains voltage).

Fig.10: Time behavior of the carrier signals i_{D+} and i_{D-} and of a the low-pass filtered line-to-line module input current $i_{N,ij,LP}$ determining the PWM, and of the resulting ripple component $\Delta i_{N,ij}$ of $i_{N,ij}$ (scales: 0.5V/div; 1A/div **(a)**, 0.25V/div, 0.5A/div **(b))**.

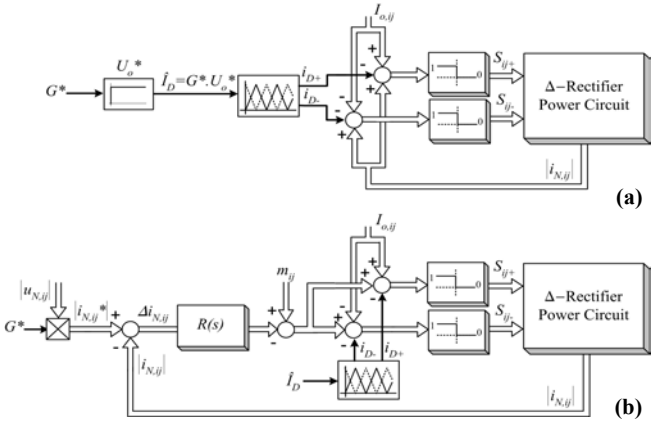


Fig.11: Block diagram of the current control employed in the case at hand (cf. **(a)**) and of a conventional average current mode control **(b)**. The conductance reference value G^* is defined by the superimposed output voltage controller. For (a) no multiplication of G^* with the rectifiers mains input voltage $|u_{N,ij}|$ is required, the conductance information is directly transferred into the amplitude $\hat{I}_{D+}=\hat{I}_{D-}$ of the carrier signals i_{D+} and i_{D-} what can be achieved with low realization effort. According to the phase shift of i_{D+} and i_{D-} the power transistors S_+ and S_- of a line-to-line module are operating in an interleaved manner; for balancing the partial module output voltages U_{O+} and U_{O-} an offset signal $I_{O,ij}$ is employed.

4 CONCLUSIONS

As shown in this paper, the minimization of the input phase current ripple of a Δ-*Rectifier* by interleaved operation of the power transistors of each line-to-line module and by formation of module input current ripples containing a maximum zero-sequence component

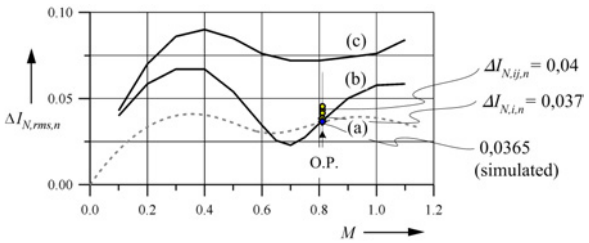


Fig.12: Normalized RMS value $\Delta I_{N,ij,rms,n}$ of the ripple $\Delta i_{N,ij}$ of a Δ-*Rectifier* line-to-line module input current $i_{N,ij}$ (cf. **(a)**) and RMS value $\Delta I_{N,i,rms,n}$ of the input phase current ripple (cf. **(b)**) in dependency on the modulation index $M=2\hat{U}_U'/U_O$ (cf. Eq.(11) in [2]). Furthermore shown: normalized RMS value of the ripple of an input phase current of the *VIENNA Rectifier* (cf. **(c)**); normalization basis: $\Delta i_n = U_O T_P/(8L)$.

which circulates inside the delta-connection can be fully utilized also under consideration of the non-idealities of a practical realization. The RMS value of the resulting mains phase current switching frequency ripple is significantly lower than for the *VIENNA Rectifier* and/or the Δ-*Rectifier* is characterized by a lower effort for the filtering of conducted differential mode EMI. As also the efficiency and the power density of the Δ-*Rectifier* are comparable to a direct three-phase PWM rectifier system (cf. **Fig.13** und **Fig.14**) and the full rated power is available also for two-phase operation, the system is of potential interest for the realization of medium or high power telecommunications rectifier modules.

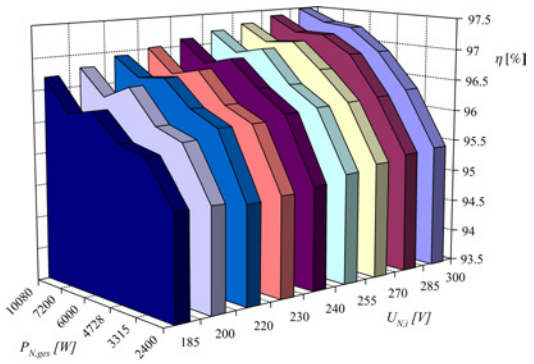


Fig.13: Dependency of the efficiency (including the auxiliary power for supplying the control board and the fans) of the 10kW prototype of the Δ-*Rectifier* on the output power and on the mains phase voltage RMS value.

In the course of the continuation of the research the star-connection of three-level single-phase PWM rectifier modules (cf. **Fig.15**) which has been proposed in [4] and denominated as three-level *Y-Rectifier* will be analyzed in detail. There, for operation in the European low voltage mains ($400V_{rms}$ line-to-line voltage) 300V power semiconductor technology could be employed for the power transistors and the free-wheeling diodes. According to first simulations the *Y-Rectifier* will allow a further halving of the mains current ripple RMS value and of the switching losses as compared to the Δ-*Rectifier*. Therefore, for equal ripple current RMS value the inductance of the input inductors and the switching frequency could be reduced and/or a higher power density and efficiency could be achieved.

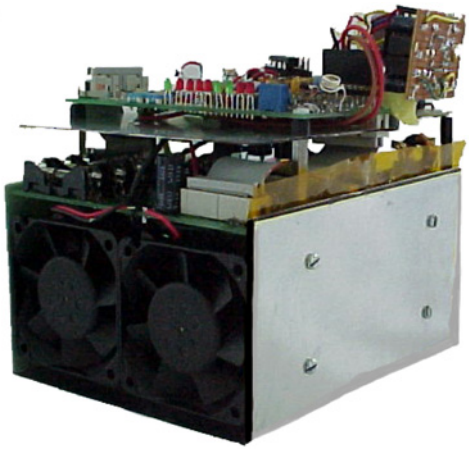


Fig.14: Prototype of a 3.5kW line-to-line module of the three-level Δ-*Rectifier*; overall dimensions: 12.5cm x 11.5cm x 15cm (power density: 1.6kW/dm^3).

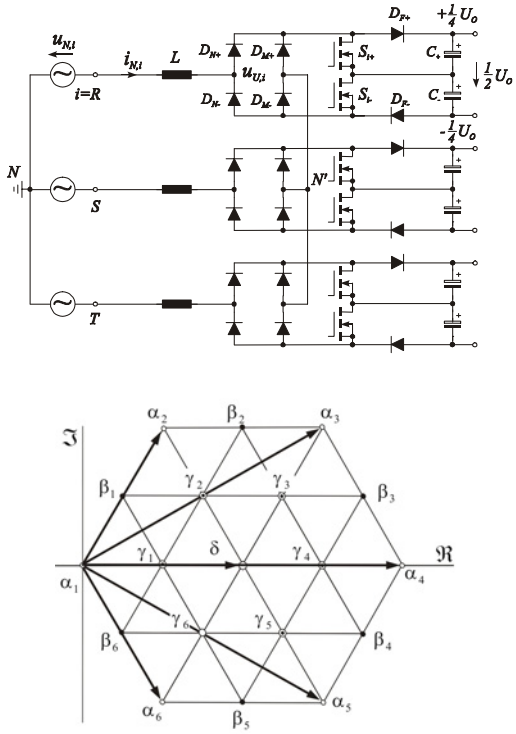


Fig.15: Basic structure of the power circuit of the three-level *Y-Rectifier* and voltage space vectors available for the input current formation in comparison to the *VIENNA Rectifier* (α_i and δ, shown by bold lines). The redundancy r of switching state δ is r_δ=10, for the space vectors β_i and γ_i we have r_β=2 and/or r_γ=6. The input phase voltages of the *Y-Rectifier* do show 17 different levels as compared to 9 levels available for the *VIENNA Rectifier*.

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