Switching Transient Shaping of RF Power MOSFETs for a 2.5 MHz, Three-Phase PFC

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Abstract—To increase the power density of active rectifiers, the switching frequency and switching-speed have to be raised considerably. However, the very fast switching transients induce a strong voltage and current ringing. In this paper, a novel magnetically coupled damping layer is introduced for attenuating these unwanted oscillations. The proposed damping layer can be implemented using standard materials and printed circuit board manufacturing processes. The system behavior is analyzed in detail and design guidelines are given. The effectiveness of the introduced layer is determined by layout parasitics, which are calculated with the Partial Element Equivalent Circuit method and compared to impedance measurements. The performance of the damping layer is demonstrated by simulations and verified via measurements on a laboratory prototype.

I. INTRODUCTION

Traditional requirements on 3-phase active rectifiers such as unity power factor and sinusoidal input currents have been extended over the last few years to include high compactness and high efficiency [1]. Therefore, the power density of active rectifiers, such as the three-level Vienna Rectifier (VR) [2], has to be increased substantially. Whereas the size of the active components (switches and diodes) can be minimized by using a low profile power module including all active components [3], the size of the passive components (EMI-filter, boost inductor etc.) has to be minimized by increasing the switching frequency.

An optimization of the size of the EMI-filter shows that a maximal power density of 24 kW/liter for a system with either CoolMOS or RF MOSFETs, water cooling and a switching frequency of 2.1 MHz could be achieved [4]. For realizing a switching frequency in the MHz range, a very fast switching transition is required in order to limit the switching losses.

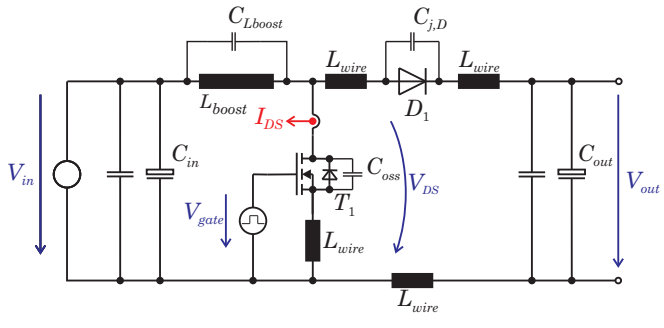

Fig. 1: Schematic of the boost circuit including some parasitic elements.

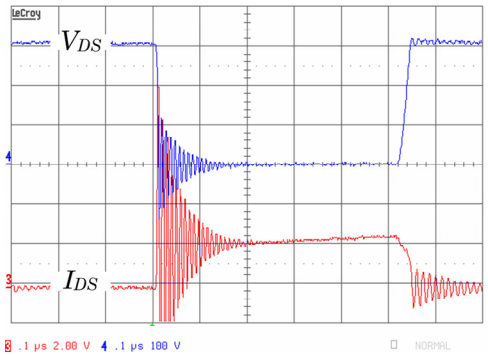

Fig. 2: Current and voltage wave shapes at turn-on of transistor T_1 at 20 A, V_{DS} (100 V/div), I_{DS} (20 A/div), time scale 50 ns/div.

Therefore, voltage slopes of 30 kV/µs and current slopes up to 2 kA/µs have to be realized.

In order to analyze the switching behavior of CoolMOS and RF MOSFET devices in combination with SiC-diodes for the target VR system with regard to switching frequencies in the MHz range in detail, a boost-type test circuit (cf. **Fig. 1**) has been designed. In Fig. 1**,** the parasitic capacitances C_{oss} of the MOSFET and $C_{j,D}$ of the diode are shown as well as the wiring inductances L_{wire} of the commutation path and the parasitic capacitance C_{Lboost} of the boost inductor. These parasitic inductances and capacitances cause current and voltage oscillations excited by the very fast switching transients (cf. **Fig. 2**). The oscillations increase the voltage stress of the devices and generate EMI noise. Basically, the ringing can be reduced by application of an RC snubber, however, the losses of such snubber circuit would be far too high for a switching frequency in the MHz range, and hence another solution has to be found for reducing the unwanted oscillations.

Some interconnection concepts with low-pass characteristics, based on high-ε-materials, have been reported in literature [5, 6]. However, these approaches are applicable only in case of longer interconnection distances to achieve the desired damping behavior.

In this paper, a novel magnetically coupled damping layer is introduced to realize the required damping. As shown in **Fig. 3** the additional layer is inserted between the two wiring layers. If the copper path of the damping layer now is terminated by an appropriately designed RC network, the currents induced in the damping layer will significantly reduce the parasitic oscillations in the wiring layers. An optimized termination network results in a very good damping

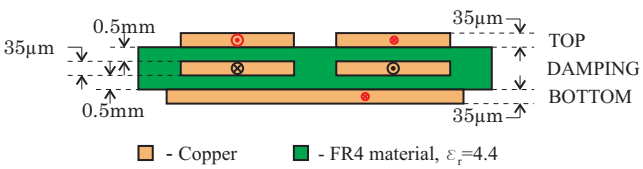

Fig. 3: Layer stack of the system with damping layer.

behavior and much lower losses compared to a classical snubber circuit. Furthermore, the damping network uses standard materials (FR4, copper) and no extra manufacturing processes are needed, which leads to lower realization costs.

In **Section II** the proposed damping concept is analyzed in detail using a simple circuit model. Furthermore, the design and optimization of the termination network is given. Subsequently, a laboratory prototype of the mentioned boost converter employing the proposed damping concept is analyzed in detail in **Section III**. The parasitic wiring elements are calculated using the Partial Element Equivalent Circuit (PEEC) method and compared to measurements of the realized prototype leading finally to a precise model of the system. The resulting voltage and current wave shapes demonstrate the very good performance of the optimized damping.

II. Analysis Of The Proposed Damping Layer

The origin of the undesired switching transient oscillations shall be described briefly in the following. At turn-on of the MOSFET T_1 the converter's input current has to commutate from diode D_1 to MOSFET T_1. Since SiC-Schottky diodes are used, there is no reverse recovery current I_{rr}. However, a displacement current is charging the voltage dependent junction capacitance $C_{j,D}$ of D_1. This capacitance in connection with the wiring inductance L_{wire} forms a series resonant circuit which is damped only by the on-state resistance $R_{DS,on}$ of T_1 and by the high frequency resistance of the wiring.

At turn-off of T_1 the input current has to commutate from MOSFET T_1 to diode D_1 and now the voltage dependent output capacitance C_{oss} of the MOSFET forms a weakly damped series resonant circuit with the wiring inductance L_{wire} of the PCB. In [7], the turn-off behavior of the MOSFET is analyzed and an analytical expression for the turn-off switching transient overvoltage is given. In the following only the behavior of the circuit at turn-on of the MOSFET shall be analyzed for the sake of brevity since the turn off behavior can be treated in a similar way.

The natural frequency f_0 and characteristic impedance Z_0 of the LC-tank at turn-on are given in (1). For SiC-diodes with some 100 pF junction capacitance and some 10 nH stray inductance f_0 lies in the 100 MHz range. To achieve a proper damping, the value of the damping resistor in series to the LC-tank has to be in the range of Z_0

$$f_0 = \frac{1}{2\pi\sqrt{L_{wire}C_{j,D}}}, \quad Z_0 = \sqrt{\frac{L_{wire}}{C_{j,D}}}. \qquad (1)$$

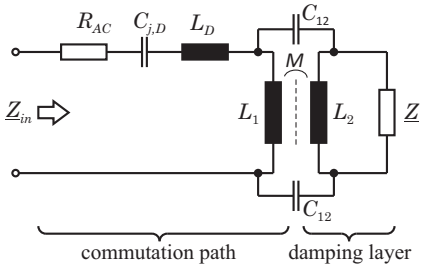

Fig. 4: Model of the circuit at turn-on of the MOSFET with damping layer.

With (1), the stray inductance of the commutation path can easily be determined by measuring the frequency of the voltage or current oscillation and by using the junction capacitance $C_{j,D}$ of the diode, specified in the datasheet.

In **Fig. 4** a simple model for the turn-on behavior of the MOSFET including the damping layer is shown, where the following symbols are used:

R_{AC}	HF-resistance of the wiring in the commutation path;
$C_{j,D}$	Junction capacitance of the SiC-Schottky diode;
L_D	Parasitic inductance of diode and MOSFET;
L_1	Effective inductance of the commutation path;
L_2	Inductance of the damping layer;
M	Mutual inductance between commutation path and damping layer;
C_{12}	Coupling capacitance between wiring layer and damping layer;
$\underline{Z}$	Termination network for damping layer.

Although the inductance of the commutation path can be minimized using a proper layout, a small residual value will remain. An excellent PCB layout offers stray inductances in the range of the parasitic inductances of the diode and the MOSFET. Hence the component parasitics are added to the model. Due to skin effect, the current of the high frequency oscillations flows only in a thin layer at the surface of the copper layer and so the HF-resistance R_{AC} has to be considered. Additionally, the skin effect reduces the effective area of the copper "wires" and so the high frequency coupling capacitance C_{12} is reduced to small values so that it can be neglected for sake of an easier modeling. Furthermore, the input inductors parasitic capacitance C_{Lboost} can be neglected because the analyzed oscillations at turn-on of T_1 are not directly affected by C_{Lboost}.

A. *Equivalent circuits*

For a better understanding of the proposed damping system two equivalent circuit diagrams for the model of Fig. 4 are given in **Fig. 5**. There, the two magnetically coupled layers are modeled by a leakage inductance L_{lki}, a magnetizing inductance L_{mi} and an ideal transformer with the ratio u_i:1. In Fig. 5(a) u_1 is chosen such, that the full leakage inductance is considered on the primary side:

$$L_{lk1} = L_1 - \frac{M^2}{L_2}, \quad u_1 = \frac{M}{L_2}, \quad L_{m1} = \frac{M^2}{L_2}, \qquad (2)$$

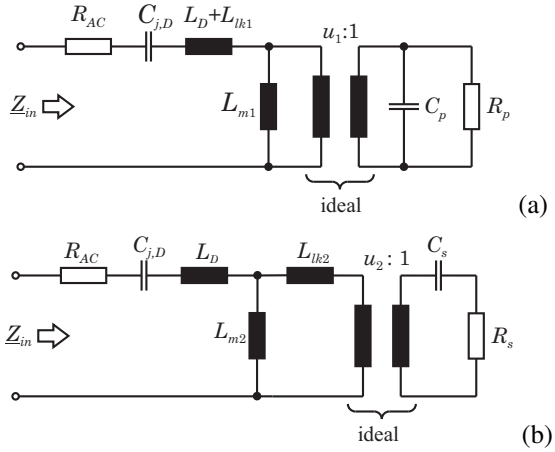

Fig. 5: Equivalent circuits for the model of **Fig. 4** for turn-on of the MOSFET with (a) leakage inductance transferred to the primary side and (b) leakage inductance transferred to the secondary side.

where in Fig. 5(b) the transformer conversion ratio u_2 is chosen such that the full leakage inductance is considered on the secondary side:

$$L_{lk2} = \frac{L_1^2 L_2}{M^2} - L_1\,, \quad u_2 = \frac{L_1}{M}\,, \quad L_{m2} = L_1\,. \tag{3}$$

B. Approaches for the termination network

As is well known from coreless transformer designs [8], the magnetizing inductance L_{mi} is quite small as compared to the leakage inductance L_{lki} because of the limited coupling of the layers. If only the resistor R_s (cf. Fig. 5(b)) is used as termination (e.g., realized by resistive materials in the damping layer itself) the major part of the input current is flowing through the magnetizing inductance because the magnetizing reactance $X_{m2} = j\omega L_{m2}$ is much smaller than the impedance of the series connection formed by R'_s (primary side referenced value) and by $X_{lk2} = j\omega L_{lk2}$. The inductance L_{mi} (and hence the coupling of the two layers) could be increased using a ferrite core or a magnetic layer as done in [9]. However this also raises the inductance of the commutation path and, therefore, is no option in the case at hand.

The unwanted leakage inductance can be cancelled if a well designed capacitor C_s is placed in series to the resistor R_s. This capacitance in connection with the leakage inductance L_{lk2} forms a series resonant circuit, which has to be tuned to a resonant frequency being equal to the oscillations to be damped. However, simulations of the proposed system showed that the coupling capacitance C_{12} can not be neglected in this case and that even a very small coupling capacitance of a few pF overrides the positive effect of canceling the leakage inductance. The best results are achieved by using a parallel connection of R and C as termination network which will be discussed in the following.

C. Damping using a parallel R-C connection

As can be seen in Fig. 5(a) the series resonant circuit, formed by $C_{j,D}$ and the sum of the inductances L_{lk1} and L_D, is connected in series with a well damped parallel resonant circuit, formed by the termination network and the inductance L_{m1}. The two elements C_p and R_p have to be transferred to the primary side considering u_1:

$$C'_p = \frac{C_p}{u_1^2}\,, \qquad R'_p = R_p \cdot u_1^2\,. \tag{4}$$

If the natural frequency f_{par} of the parallel resonant circuit is chosen according to

$$f_{par} = \frac{1}{2\pi\sqrt{L_{m1}\cdot C'_p}} = f_{ser} = \frac{1}{2\pi\sqrt{(L_D + L_{lk1})\cdot C_{j,D}}}\,, \tag{5}$$

leading to

$$C_p = \frac{L_D + L_{lk1}}{L_{m1}} C_{j,D} \cdot u_1^2\,, \tag{6}$$

and the damping resistor is chosen to

$$R_p = \frac{R'_p}{u_1^2} \approx Z_1 = \sqrt{\frac{L_D + L_{lk1}}{C_{j,D}}}\,, \tag{7}$$

the damping of the resulting system can be increased significantly. A Bode plot of the input impedance

$$\underline{Z}_{in} = \underline{Z}_{ser} + \underline{Z}_{par} \quad \text{with} \tag{8}$$

$$\underline{Z}_{ser} = \frac{1 + sR_{AC}C_{j,D} + s^2 C_{j,D}(L_D + L_{lk1})}{sC_{j,D}} \quad \text{and} \tag{9}$$

$$\underline{Z}_{par} = \frac{sL_{m1}}{1 + s\dfrac{L_{m1}}{R_p} + s^2 L_{m1} C_p} \tag{10}$$

is given in **Fig. 6**. The damping of the system is increased when the magnitude of the input impedance is increased at the resonant frequency. Since (7) is only an approximation, the optimal values for a maximal damping can be found by application of the following optimization function:

$$Z_{opt} = \left|\underline{Z}_{in}\left(f, C_p, R_p\right)\right|\Big|_{\arg(\underline{Z}_{in}(f))=0°} \rightarrow \max\,. \tag{11}$$

The result of the optimization for an assumed system with

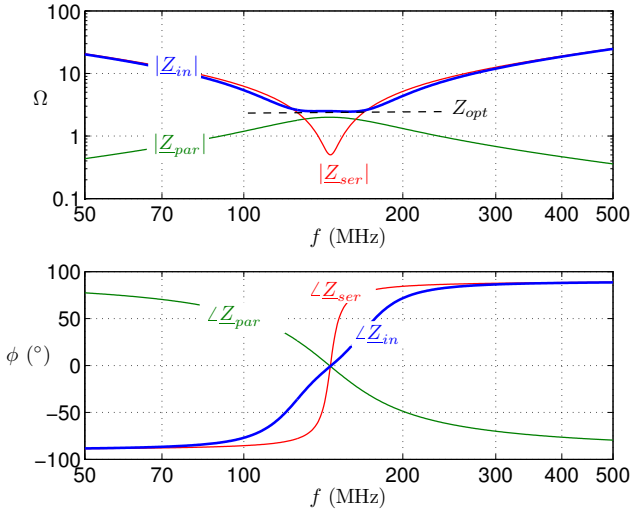

Fig. 6: Calculated Bode diagram of impedances $\underline{Z}_{ser}$, $\underline{Z}_{par}$ and $\underline{Z}_{in}$ for the system: L_1=10 nH, L_2 = 10 nH, M = 5 nH, L_D = 6 nH and $C_{j,D}$ = 136 pF.

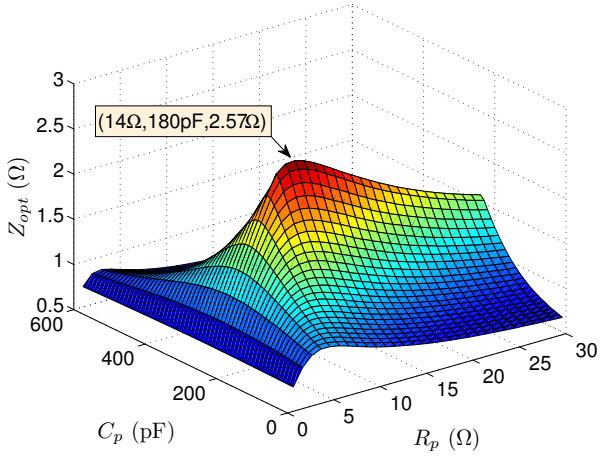

Fig. 7: Calculated magnitude of impedance Z_{opt} as a function of the termination network parameters R_p and C_p.

the parameters L_1 = 10 nH, L_2 = 10 nH, M = 5 nH, L_D = 6 nH and $C_{j,D}$ = 136 pF is depicted in **Fig. 7** and the results are summarized in **TABLE 1**.

TABLE 1
CALCULATED VALUES FOR THE TERMINATION NETWORK ACCORDING TO (6) AND (7), AND RESULTS OF THE OPTIMIZATION ACCORDING TO (11).

	R_p	C_p
Calculated values	9 Ω	186 pF
Result of optimization	14 Ω	180 pF

III. DESIGN OF A DAMPING LAYER

A. *Design of the realized prototype*

The design of the damping layer is performed using a boost converter as an example (cf. Fig. 1). This circuit is also used to study the switching behavior of different MOSFET devices. To achieve very fast switching transients, a low impedance gate driver DEIC420 featuring a peak current capability of over 20 A is used. For the boost diode D_1 a 600 V SiC-Schottky diode CSD20060D is used; output capacitance C_{out} and also input capacitance C_{in} are partly realized by several 220 nF / 630 V ceramic type SMD capacitors, providing high current capability and low inductance.

In [10] it is shown that the switching losses are dominated by the intrinsic capacitance $C_{oss}(V_{DS})$ of the MOSFET when very fast switching is realized. Because of the low $R_{DS,on}$ of the CoolMOS SPW47N60C3 and its low output capacitance C_{oss} at V_{DS} = 300 V, a superjunction power MOSFET seems to be an ideal choice for high speed switching. Unfortunately, as shown in [11], C_{oss} rises from a few 100 pF to over 10 nF for very low blocking voltage levels. This results in long delay times at turn-off of the device, finally leading to significant current distortions for lower current values in single phase and three phase active rectifier applications [4]. To overcome this drawback the RF switch-mode power MOSFET DE475-501N44 from IXYS-RF is used. This device shows a much less pronounced $C_{oss}(V_{DS})$-characteristic than

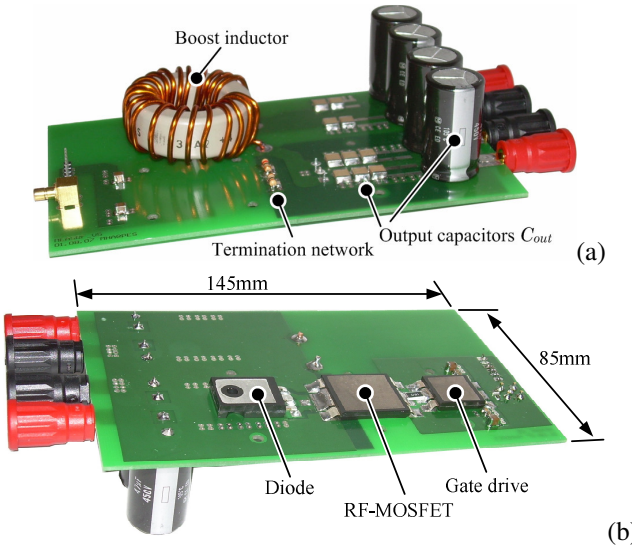

Fig. 8: Realized prototype of the boost circuit with PCB board wiring including a damping layer with optimized termination network. (a) TOP view and (b) BOTTOM view of the prototype which can directly be mounted on a heatsink.

superjunction MOSFETs. Additionally, the RF MOSFET utilizes a DE475 package which is optimized for high speed, high frequency, high power applications (**Fig. 8**). Due to the symmetrical package design, where the two source terminals lie on either side of the drain terminal, the parasitic inductance of the device can be reduced to less than 5 nH [12]. Due to the two source terminals two commutation paths have to be also considered. The layout of the boost circuit is optimized for very low wiring inductances in the commutation path. To form the proposed damping structure a copper loop (terminated by the proposed RC-network) is routed in a layer that is between the two wiring layers (cf. Fig. 3).

B. *Current measurement*

The MOSFET current I_{DS} is measured using a self-made AC-current probe (**Fig. 9**). The sensor has been designed for a sensitivity of 100 mV/A using a minimum number of turns to achieve a high bandwidth. The performance of this sensor has been compared to a 2 GHz shunt of T&M research [13] and shows very good results for frequencies beyond 100 MHz. Due to its small size the current transformer can be plugged directly on the connection leads of a TO220- or TO247-package. Unfortunately the DE475- package has wide connection leads and, therefore a short wire has to be used to insert the current sensor into the circuit, resulting in an additional inductance of approximately 8 nH for the commutation path which has to be considered in the model of the damping circuit

Fig. 9: Self-made AC-current transformer with a sensitivity of 100 mV/A to measure the Drain-Source current I_{DS} of the MOSFET.

C. *Design of the damping layer using PEEC method*

For designing an optimal termination network of the damping layer, the parasitic elements of the system have to be considered. These elements could be determined by impedance measurements on the realized hardware using an adequate impedance analyzer. However, due to the fact that such measurements in the pF / nH-range are rather difficult, an alternative method to determine the parameters in an early state of system design based on simulation without building a dedicated prototype shall be used.

For a simulation including layout parasitics, the PEEC method emerged as a computational effective and accurate technique [14, 15]. Here, the PCB layout is discretized into a large number of individual elements as shown in the 3D-model of the prototype layout (cf. **Fig. 10**). The PEEC method creates matrices of partial elements representing the magnetic and electric field couplings and the resulting equations subsequently are solved in a Spice-like circuit simulator. Recent development makes PEEC an integrated full wave method, which can handle non-orthogonal elements [16] as well as dielectrics [17]. In **TABLE 2** both simulation results of the PEEC method and measurement results, using the impedance analyzer HP4294A, are summarized. The difference between the measured and calculated layout inductances L_{1i}, L_{2i} and M_i has its origin in the measurement technique, which poses a challenge due to the compact geometry of an optimized layout.

Since all parameters of the prototype are identified, a simplified model of the boost circuit can be drawn (cf. **Fig. 11**). Using the optimization of (11) results in $R_{p,opt}$= 22 Ω and $C_{p,opt}$= 184 pF for the termination network. The optimized components of the termination network are added to the PEEC model.

The capacitive coupling C_{12} between the proposed damping layer and the circuit layout, which is neglected for the sake of easy modeling in **Section II**, lowers the damping performance. Due to the distributed nature of the parasitic capacitance and inductance, it is not possible to distinguish clearly between the opposing effects of magnetic and capacitive coupling between the layers. Likewise, the assumption of a frequency independent lumped inductance and capacitance is not an accurate representation. However, the solver [18] takes all these effects into account.

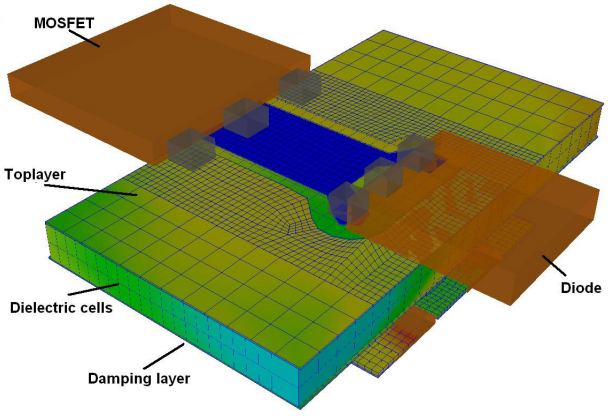

Fig. 10: PEEC model of the realized prototype with damping layer.

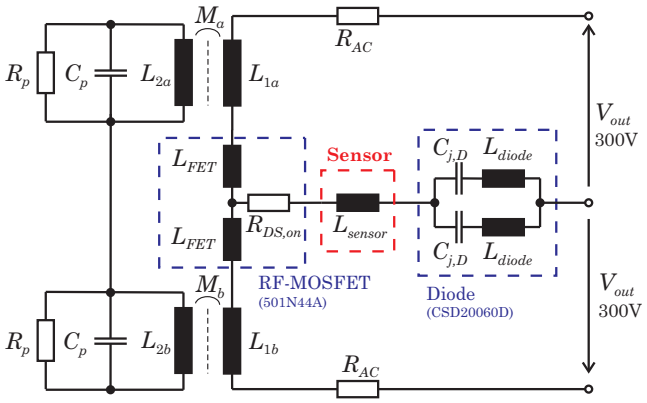

Fig. 11: Simplified model of the realized prototype with damping layer including parasitic elements of the RF-MOSFET, current sensor and the SiC-diode.

The simulated total impedance of the commutation path with optimized damping network, including the dielectric of the FR4 material (ε_r=4.4), is depicted in **Fig. 12**. There is also an impedance measurement included, taken from the realized prototype, as well as the calculated impedance of the simplified model of Fig. 11. The measurements could only be performed up to 110MHz due to the bandwidth limitation of the used impedance analyzer HP4294A. The damping of the resonance at 100 MHz is apparent. The similarity of simulation and measurement is very good but also the simplified model with lumped elements shows very good results.

TABLE 2
MEASURED AND SIMULATED PARASITICS OF THE REALIZED PROTOTYPE.

	Measurements (HP4294A)	Simulation (PEEC method)
L_{diode}	10.9 nH (per diode)	-
$C_{j,D}$	55 pF	-
L_{FET}	4 nH (per lead)	-
L_{sensor}	8 nH	-
R_{AC}	500mΩ	-
L_{1a} / L_{1b}	8.2 nH / 7.7 nH	11.3 nH / 10.5 nH
L_{2a} / L_{2b}	9.9 nH / 8.1 nH	11.5 nH / 10.6 nH
M_a / M_b	5 nH / 5.25 nH	6.4 nH

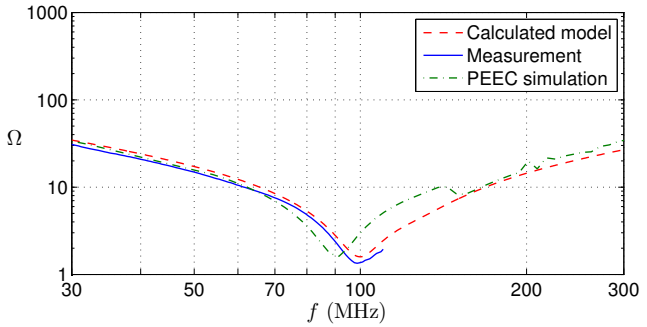

Fig. 12: Impedance measurement, calculated impedance using (8) – (10) and corresponding PEEC simulation of the commutation path, including the effect of the damping layer.

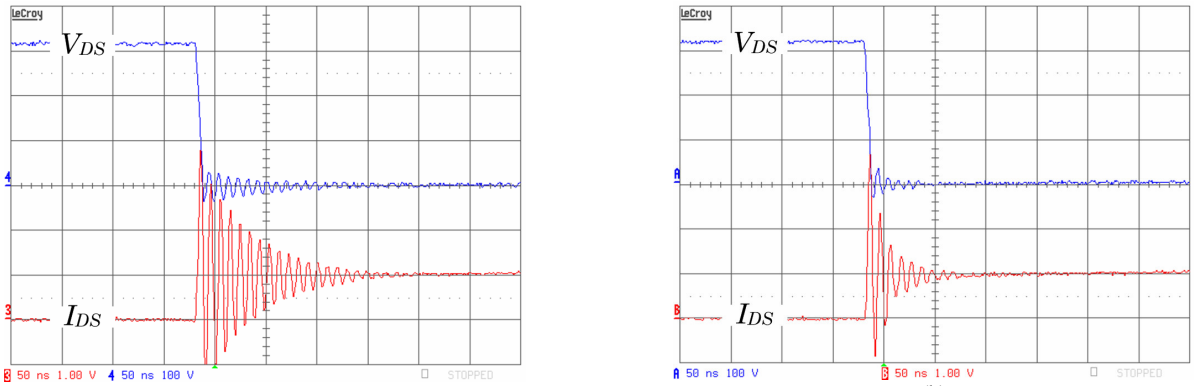

Fig. 13: Measurement results taken from the realized prototype (a) without damping layer and (b) with damping layer terminated with an optimized RC-network. U_{DS} (300 V/div), I_{DS} (10A/div), time scale 50 ns/div.

D. Experimental Results

The realized prototype with optimized damping network has been tested for a boost converter output voltage of 300 V and for current levels up to 20 A. The results for a current of 10 A are given in **Fig. 13** (for Fig. 13(a) the damping layer of the PCB has been left open). It can be seen that the switching transient oscillations are reduced significantly using the damping layer. Although the first voltage/current peak is still present, the decay of the ringing is enhanced noticeably.

The time domain response of the commutation path exited by a step function is calculated based on the simulated impedance curve. In **Fig. 14** the numerical result of this transformation is compared to a current measurement taken from the realized prototype for a current of 10 A (the amplitude of the input step of the numerical system is scaled to obtain an equal final value). The oscillation frequency of the simulated system is slightly smaller compared to the measured. This can also be seen at the lower resonance point in Fig. 12. However, the simulated maximum peak current and especially the damping effect are in good agreement with the measurement results. Therefore a PEEC simulation can be used to directly analyze the performance of the designed damping system in an early development state.

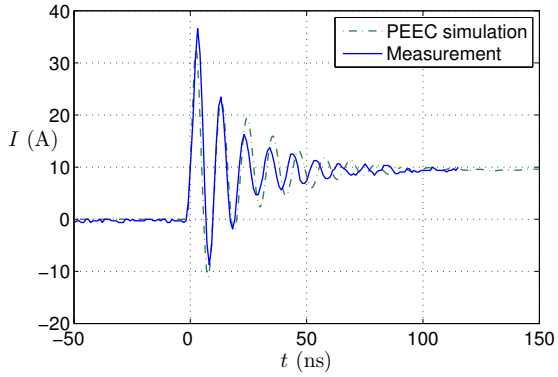

Fig. 14: Measured and calculated current shape obtained from a numeric Laplace transform of the impedance curve of **Fig. 12**.

IV. CONCLUSIONS

In this paper a new passive damping layer is introduced for damping the undesired voltage/current ringing appearing at the switching instants of hard-switched power electronic converters. An additional copper layer, terminated by an optimally designed RC-network, is inserted between the PCB wiring layers of the converter. A very simple model describing the overall system behavior, as well as design guidelines for the damping layer and the RC-termination network are given. The design and performance of the proposed damping layer is shown for a realized boost-converter circuit. For the arrangement and the optimization of the termination network, impedance measurements of the realized PCB would be necessary. It is shown that by application of the PEEC simulation method the system can be designed and analyzed in an early development state without an existing hardware prototype. Measurements, taken from the realized prototype show, that the switching transient oscillations can be reduced significantly but it is also shown that the damping capability of this purely passive approach is limited.

An active control of the switching transient would be an enhanced method for reducing the oscillations. This active control (to be implemented into the gate drive stage of the MOSFET), however, would have to have a control bandwidth in the frequency region of the oscillations to be damped (e.g., typ. 100 MHz for state-of-the-art power MOSFETs). Such active damping seems to be impossible using discrete components, but could be realizable if the gate drive, the active control of the switch and the switch itself are closely integrated.

The switching-transient oscillations at turn-on of the MOSFET are mainly determined by the relatively high junction capacitance of the SiC-diode. The performance of the proposed passive damping layer could be increased considerably if this capacitance is reduced. This can be achieved in future by application of other semiconductor technologies.

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