Design and Realization of a Multi-Cell-Switch-Mode Power Amplifier Employing a Digital Poly-Phase-Pulse-Width-Modulator

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Abstract

This paper presents a multi-cell switch-mode power amplifier formed by a series connection of six H-bridge switching cells. The phase-shifted gating signals of the switching cells are generated using a digital poly-phase-PWM implemented by application of a low-cost CPLD. The generation of the isolated DC link voltages of the switching cells is performed by six series-resonant half-bridge DC/DC converters. The advantages and drawbacks of the circuit topology and the proposed PWM scheme are discussed based on measurements gained from a realized 400V/5A prototype system. There, especially the impact of the delay of the digital modulator on the amplifiers dynamic behavior is analyzed.

1 Introduction

Switch-mode power electronic systems are more and more used to realize power amplifiers. These "class-D" amplifiers are used, e.g., for simulating the mains voltage while testing the EMI compliance of a system. For such tests (e.g. according to IEC-1000-3-2/3) voltages up to ±400V and currents up to ±10A are required. Switch-mode amplifiers generate their output voltage by pulse width modulation (PWM) and a subsequent low pass LC filter. The cut-off frequency of the LC output filter and the limited switching frequency of the bridge legs define the limited bandwidth of such an amplifier. Several methods have been discussed in the past to overcome this drawback, like using a linear correction stage [1] or a hybrid output filter [2]. In this paper a multi-cell topology, formed by a series connection of six H-bridge switching stages (cf. **Fig.1**), is used to increase the bandwidth. Using an interleaved PWM of the N individual cells, results in an effective switching frequency being N-times the switching frequency of a single cell. This significantly increases the bandwidth of the multi-cell amplifier and reduces the effort to realize the output filter because the cutoff frequency can be increased as well and the voltage- and current-ripple at the output is reduced. A detailed analysis of this structure can be found in [3]. Due to the series connection of the cells the blocking voltage of the semiconductors is also reduced by a factor of $1/N$. So semiconductors with a low blocking voltage capability can be considered. This allows the application of majority-carrier devices such as low-voltage MOSFETs and Schottky-diodes. Also the EMI behavior of the system is improved by the multi-cell concept, because only voltage transitions of U/N (instead of U) occur.

Based on the proposed multi-cell concept a laboratory prototype system with following specifications has been realized:

output voltage:	$u_{OUT} = \pm 400\mathrm{V_{pk}}$
output current:	$i_{OUT} = \pm 5\mathrm{A}$
output power:	$P_{OUT} = 2\mathrm{kW}$

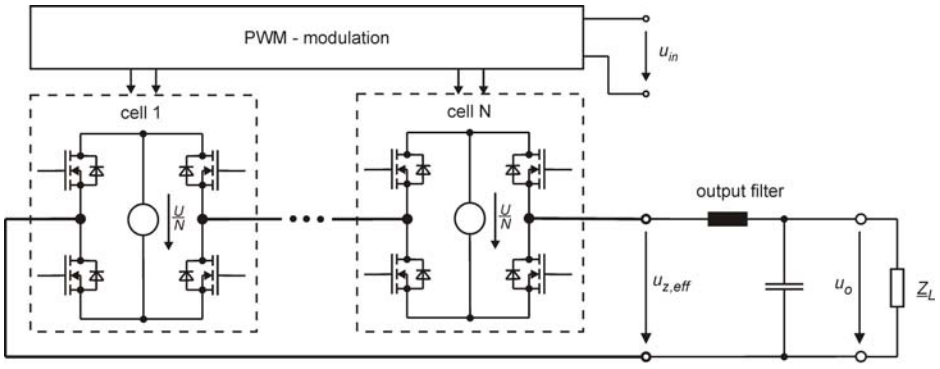


Fig.1: Basic circuit topology of the realized multi-cell switch-mode power amplifier based on a series connection of H-bridge switching-cells ($N = 6$ cells); the autonomous cells are controlled based on interleaved poly-phase pulse width modulation.

switching frequency: f_S = 25kHz (per cell)
number of cells: f_N = 6 H-cells

2 DC-Link Supply

To realize the proposed multicell structure an independent DC-link isolation stage for each individual cell is necessary. As in total N isolation stages are required, an efficient but as simple as possible circuit for feeding the DC-links shall be used. For the proposed system a series-resonant topology has been selected (**Fig.2**). Caused by the resonant operating mode almost zero-voltage and zero-current turn-on of the power transistors can be achieved. The transformer leakage is utilized as inductance to form the resonant circuit together with the two capacitors $C_r/2$. For the realization at hand a switching frequency of f_s=75kHz has been chosen. With this, an explicit resonance inductor can be avoided. Hence a drawback of the transformer is used advantageously. Increasing the transformer leakage usually also reduces coupling capacitance between primary and secondary winding. This helps to reduce the resulting common mode current originated by the common mode stress between the individual cells.

On the secondary side a full bridge rectifier is used. Using the corresponding equivalent circuit of the series resonant converter (Fig.2 (b)), the converter can be calculated analytically. This calculation, including some design proposals which are used in the following section, can be found in [4].

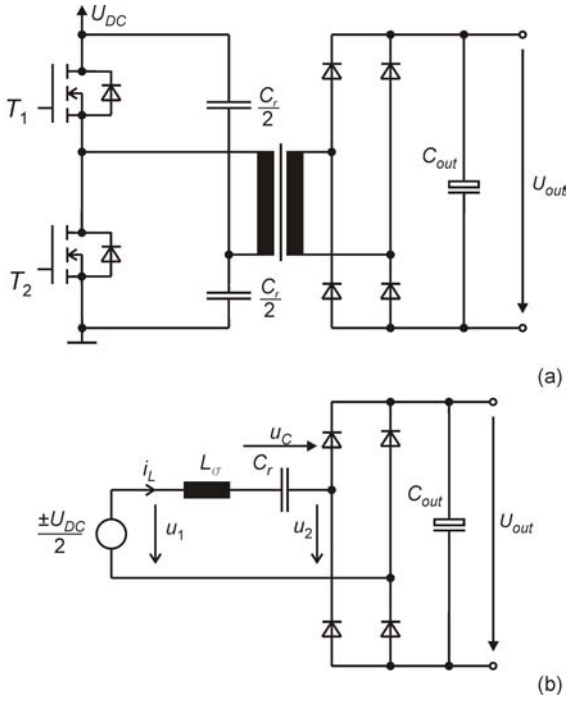


Fig.2: Series resonant converter. (a) Basic schematic and (b) corresponding equivalent circuit.

2.1 Practical Realization

To meet the requirements of an amplifier output voltage of $400V_{pk}$ a DC voltage level of 75V for each cell has to be chosen (N=6 cells). On the primary side all DC-links are connected in parallel to a DC link voltage of 300V…400V, (e.g., generated by a single-phase PFC), leading to a transformer ratio of n = 2:1.

The converter is operated in fixed frequency mode using the self-oscillating gate driver IR21531D dimensioned for a switching frequency of f_S = 75kHz. The two power MOSFETs IRFB9N60 (0.72Ω, 500V, TO220) are featured with an additional turn-off speed up circuit using two PNP transistors (BC807). For the transformer an ETD34 ferrite core (material: N67) is selected with a primary winding of 30 turns. To get a adequate leakage an isolation of 1.5mm depth is applied between primary and secondary, leading to L_s = 31µH. The natural frequency of the resonant circuit is set to f_0 = 50kHz (f_S/f_0 = 1.5, see also [4]) using two 150nF foil-type capacitors (B632653, EPCOS) to form the resonance capacitance C_r.

As described in the next section, the rectifier diodes on the secondary side have to be of fast-switching type to achieve zero-voltage switching behavior. Therefore, 100V Schottky diodes 31DQ10 (0.85V, 3.3A, DO41) are used.

2.2 Measurements and Discussion

The measured voltage/current wave shapes of the prototype converter are given in **Fig.3**. Despite the fact that the MOSFET bridge-leg generates a square-wave output voltage, resonant currents appear which are characterized by sinusoidal sections of natural frequency f_0. The converter operates with a switching frequency being 1.5-times higher than f_0. Hence, the according MOSFET turns off prior the zero crossing of the resonant current leading to turn-off losses. According to Fig.3 (b) a single switching process will be discussed now. At instant t_1 the low-side MOSFET switches off. Due to the interlock delay (600ns) of the gate driver both transistors are in off-state for a short time period. As mentioned before, there is still a current flowing through the resonant circuit. This current now rapidly charges the drain-source capacitance of the low-side MOSFET and discharges the capacitance of the high-side MOSFET. The resonance current is reduced mainly afterwards whereas the voltage at the drain of the low-side MOSFET reaches the primary side DC voltage level of 300V. If the high-side FET would turn on at instant t_2 (zero crossing of i_L) the converter would achieve true zero-voltage and zero-current switching and no turn-on losses would occur. For the case at hand the (too long) interlock delay of the gate driver delays the turn-on of the high-side MOSFET until t_3. At the zero crossing of the resonance current the corresponding rectifier diodes begin to block. But their existing reverse current recharges the low-side MOSFET. As a con-

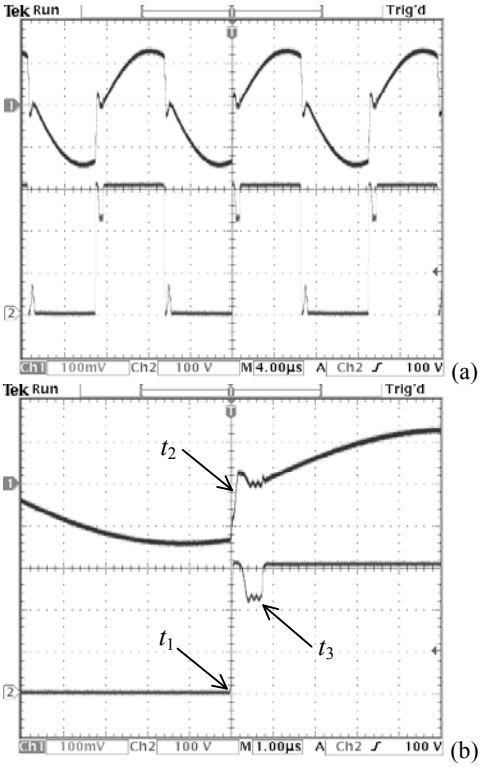


Fig.3: Current and voltage wave shapes of the series resonant converter, load: R_L=40Ω, Ch1 ... resonant current i_L (1A/div), Ch2 ... drain-to-source voltage of low-side MOSFET (100V/div). (a): 4µs/div; (b) detail showing turn-off of low-side MOSFET, 1µs/div.

sequence, the high-side MOSFET has no true zero voltage switching condition for turning on at instant t_3 and so also turn-on switching losses occur. To avoid this problem a current dependent control of the interlock delay would be preferable, which could be implemented, e.g., by application of a control based on a fast FPGA. A second advantage of using a FPGA to generate the gating signals of the six converters is the possibility to realize a phase-shift of the individual cells which lowers the DC link capacitor stress and improves the EMI behavior of the circuit. As measurement results taken from a single-cell laboratory prototype demonstrate (cf. **Fig.4**) true zero-voltage switching can be guaranteed by proper delay time control. On the other hand zero-voltage switching can only be guaranteed achieved in case the load current shows a specific magnitude such that the MOSFET drain-source voltage swing obtains full DC link voltage. For the presented prototype converter a load current of at least ≈1A is required to achieve true zero-voltage switching.

3 Poly-Phase-DPWM

Each cell is designed to work with a switching frequency of f_S = 25kHz. If the gate signals of the six individual H-bridges show a specific phase shift an "effective" switching frequency of f_{eff} = 2·6·25kHz = 300kHz can be achieved (the two half-bridges of the H-bridge are also phase shifted by a factor of 180°). As described in [4] the poly-phase pulse width modulation leads to a largely reduced output voltage/ current ripple of the amplifier. However, a huge degree of complexity to realize a PWM-modulator which generates the 12 phase-shifted channels in analog technique exists. Consequently, a digital PWM-modulator (DPWM) has been developed based on a programmable logic device. An additional advantage of using a DPWM is the independence of temperature, moisture, aging and component tolerances as well as its frequency and phase precision. Remark: It has to be considered that the fundamental advantage of phase-shifted poly-phase systems (i.e., the cancellation of all switching frequency components below $N{\cdot}f_S$ for a system based on N channels) is valid only for a precise 360°/N phase-shift.

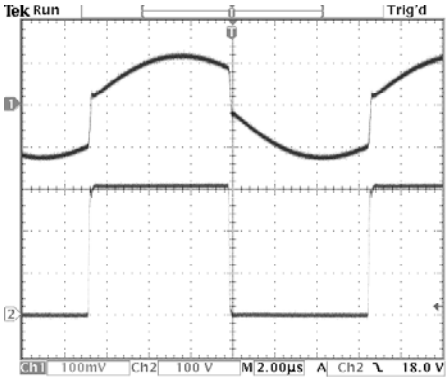


Fig.4: Current and voltage wave shapes of a series resonant converter with current dependent control of the interlock delay; parameters as Fig.3, 2µs/div.

Since a digital PWM-modulation procedure is used, a purely digital control of the amplifier (output voltage) would be self-evident at a first glance. However, a closer investigation of a fully digital control loop reveals stability problems mainly caused by the dead time delay of the A/D converters. Furthermore, the increased realization effort for a digital controller (usually requiring a high-speed DSP) has to be mentioned.

Therefore, for the presented amplifier system an analog control structure shall be used in conjunction with a digital PWM-modulator (see **Fig.5 (a)**). The analog control structure is discussed in the next section. The 12-bit successive approximation ADC AD7495BR realizes the interface between the analog control and the digital modulator. Since the amplifier shall be dimensioned for an effective switching frequency of 300kHz, the sampling frequency of the A/D converter has also be fixed to 300kHz. Because of the low pass characteristic of the control loop no anti-aliasing filter is used at the ADC's input. For implementation of the DPWM, 12 independent and phase shifted digital PWM modulators are required. It is almost impossible to realize this task using a micro-

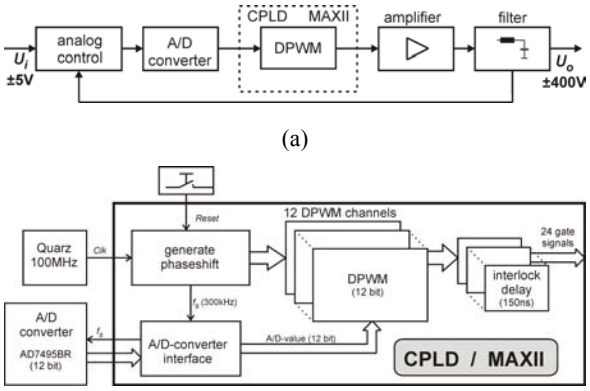


Fig.5: (a) General control-oriented signal diagram of the realized amplifier. (b) Block diagram of the implemented DPWM based on a CPLD by Altera Corp.

controller or DSP system being commonly available. In contrast, programmable logic is nearly ideal dedicated to do this job. For the realized prototype system a single low-cost CPDL EPM1270-C3 of Altera's MAXII-series is used to implement the complete DPWM. A structure diagram of the implementation using the main blocks (i) A/D converter interface, (ii) phase shift generation, (iii) 12 DPWM channels and (iv) interlock delay generation is given in Fig.5 (b). The entire chip is driven with an external generated 100MHz-clock and the ADC's sampling frequency is derived from this signal in the phase shift generation block. All the 12 DPWM pulse width registers are updated with the 12-bit A/D converter result at every sampling instant. Basically, only a discrete set of output voltages can be generated employing a digital PWM modulator. As mentioned in [5] the resolution of the DPWM has to be sufficiently fine such that the change in the output voltage caused by 1 LSB of the DPWM is smaller than 1 LSB of the A/D converter. Otherwise limit cycle oscillations would be existent. Consequently, a resolution of 12-bit is used for the realized DPWM.

Because a gate driver without any interlock delay is used for the H-bridges, the required interlock delay to prevent cross conduction of the bridge-legs is realized also digitally within the CPLD. The ideally matched interlock delay of the proposed design has been found to be $t_d = 150$ns.

3.1 DPWM Generation

Several methods have been reported to realize a digital PWM-modulator. They have to be compared under consideration of their timing and die area requirements and that the realization should be possible using a CPLD. Additionally, the modulator concept should be well suited for implementing poly-phase-PWM. The "classical" digital modulator consists of a counter and a digital comparator (cf. **Fig.6 (a)**). According to Fig.6 (b) the output is set when the counter starts (Q=0) and a reset signal appears if the counter meets a specific value $Q=U_e$ defining the pulse-width. The implementation of such a modulator in a CPLD is very easy, but requires a very high clock frequency. A clock-frequency of

$$f_{clk} = 2^{12} f_s = 102.4MHz \qquad (1)$$

is required for a switching frequency of f_s=25kHz and if a 12-bit DPWM should be realized with this approach. However, because an implementation based on such a high clock frequency is possible with the selected CPLD, the described counter/comparator concept is used even if it is basically not ideally suitable for poly-phase implementation.

As an alternative, a ring-oscillator-MUX scheme has been proposed in [6] for realizing a poly-phase DPWM. There, the fast counter is replaced by a ring oscillator consisting of differential inverters combined with a multiplexer (MUX). Higher operating frequencies would be possible with this approach, however, it is not suited for an implementation to common CPLDs. Very high resolutions for DPWM are possible using a hybrid delay-line/counter scheme as described in [7], but this solution is not very well suited for poly-phase-modulation.

In the proposed poly-phase DPWM based on counters, 12 independent DPWM-modulators are used. Therefore, in total 12 counters and 24 comparators are necessary. An alternative solution using just a single counter and modified compare values in contrast would require 12 adders with a length of 12-bit. With this, no die area would be saved and the systems complexity would be increased. Instead, the phase-shift of the 12 counters is achieved and monitored by the "generate phase-shift"-block (cf. Fig.5 (a)).

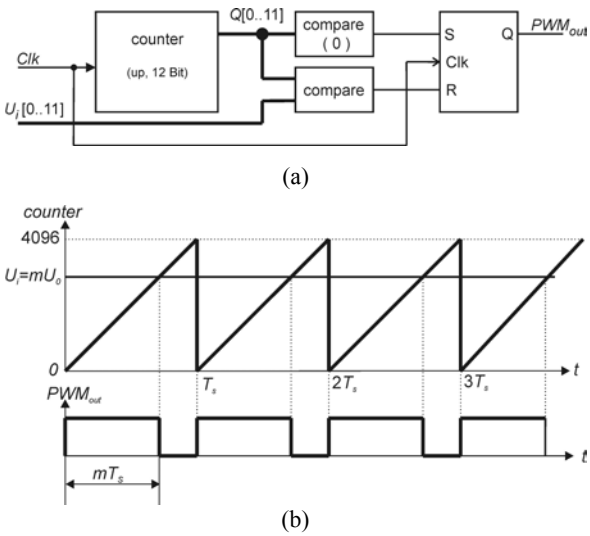


Fig.6: Classical counter/comparator DPWM. (a) Simplified diagram and (b) corresponding waveforms.

3.2 Update Scheme of the DPWM

The update scheme of the counter/comparator unit is very important because it is directly linked to the total delay of the modulator being finally effective for the dynamic behavior of the control loop. The update-rate of the PWM (300kHz) is 12 times higher than the output (switching) frequency of the PWM channels (25kHz). The following update-scheme is used:

i) Modulator output signal PWM_{OUT} is set to 1 exclusively at instant Q=0 (i.e., counter value equals zero, 25kHz repetitive).
ii) PWM-register is updated every ADC sampling instant (300kHz).
iii) PWM_{OUT} immediately is set to 0 if the new pulse-width U_e is less than the actual counter value Q.

So the PWM channel does not turn-on twice a period even in case the PWM has already been switched off and the new pulse-width is higher than the actual counter value, which prevents the MOSFETs from uncoordinated high frequency switching. However, according to this update-scheme slightly different pulse-widths of the individual PWM-channels may occur. This pulse-width differences result in lower switching frequency harmonics which are present in the output signal. However the input frequencies of the amplifier-system are much smaller than the update-frequency and so these effects can be tolerated.

3.3 Model of the Poly-Phase-PWM

For the design of a proper controller for the amplifier's output voltage a linearized dynamic model of the modulator shall be developed based on an identification procedure (the modulator's transfer function is identified by analyzing its step-response). For this purpose, at first according to **Fig.7 (a)** a passive summation of the modulator's output signal is performed. In connection with a 20nF smoothing capacitor a first-order low-pass filter showing a delay time of $T_{Filter}= R{\cdot}C =$ 3.67µs is formed. According to the measured step response (cf. Fig.7 (b)) the actual system can be identified as:

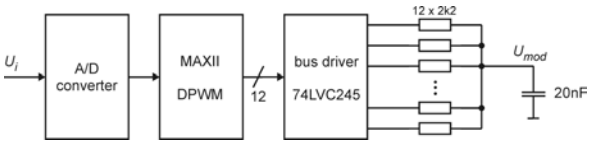
$$G_{res} = \frac{1}{1+sT_{res}} e^{-s\cdot T_t} = \frac{1}{1+s\cdot 6\mu s} e^{-s\cdot 5\mu s} \qquad (2)$$

I.e., the modulator shows a low-pass characteristic with a serious amount of dead time, which can be divided into the dead time of the A/D-converter and the dead time of the PWM-modulator itself. The influence of the measuring filter T_{Filter}

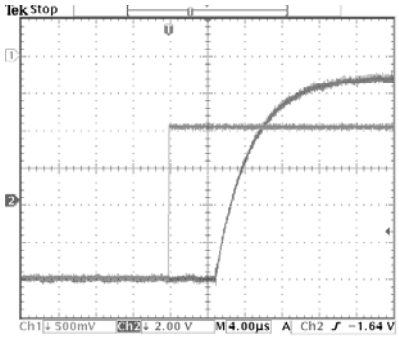
$$G_{res} = \frac{1}{(1+sT_{filter})} \cdot \frac{1}{(1+sT_{DPWM})} \qquad (3)$$

now can be removed analytically. Neglecting the second order terms ($T_{Filter} \cdot T_{DPWM}$) leads to

$$G_{res} \approx \frac{1}{1+s(T_{filter}+T_{DPWM})} \ . \qquad (4)$$



(a)



(b)

Fig.7: Identification of the modulator's transfer function. (a) Schematic measurement circuit and (b) measured transient response of the modulator.

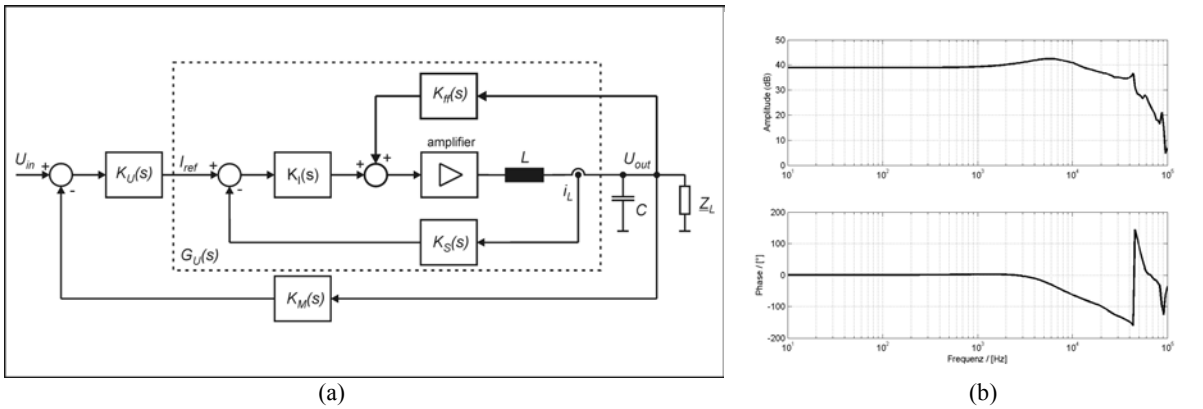
This results in the transfer function of the modulator

$$G_{\mathrm{mod}} = \frac{1}{1+s\cdot T_{DPWM}} e^{-sT_t} = \frac{1}{1+s\cdot 2.4\mu s} e^{-5\cdot \mu s} . \qquad (5)$$

As compared to the 300kHz sampling time (T_s=3.3µs) the total dead time of the modulator is quite high so that stability problems of the controller have to been expected.

4 Controller Design

A two-loop control arrangement with a dedicated current controller and a superimposed voltage control as shown in **Fig.8 (a)** is used for the control of the amplifier's output voltage. For the design and the dimensioning of an appropriate controller the non-phase minimum transfer function of the modulator has to be conditioned applying a 2nd-order Padè-approximation. For the (inner) current loop a P-type controller with voltage-feed-forward is used, whereas the output voltage control is performed using a PI-type controller. As a consequence of the modulator's dead time the dynamic behavior of the current control loop shows a resonance at a frequency of 45kHz. This resonance is still present in the resulting transfer function of the entire amplifier. The bode diagram of the amplifier running at no-load Fig.8 (b) has been recorded using the vector network analyzer Bode 100 of Omicron electronics [8]. Due to the additional damping impact of the load (assumed to be purely resistive) a trade-off has to be accepted between stability at no-load operation and bandwidth at nominal load. As a consequence, the realized amplifier (cf.



(a) (b)

Fig.8: Closed loop operation of the amplifier. (a) Block diagram of the two-loop control arrangement and (b) bode diagram of the amplifier running at no-load condition (recorded with Bode 100 analyzer).

Fig.9) finally shows an open-loop –3dB bandwidth of 10kHz (at a switching frequency of 25kHz), whereas a reduced bandwidth of 5kHz can be specified for closed-loop control.

5 Conclusions

A multi-cell switch-mode power amplifier has been realized successfully. The applied series resonant converters are ideally suited for providing the required isolated DC-links. However, using a fixed interlock-delay true zero-voltage switching can only be achieved for sufficiently high load current.

An analog controller in conjunction with a digital poly-phase PWM serves for the output voltage control of the amplifier and a CPLD is used to implement the poly-phase-PWM in a truly digital manner. The classical counter/comparator PWM approach can be implemented easily in the CPLD. However, this realization is characterized by a substantial amount of delay-time, caused by the update scheme of the poly-phase PWM and the A/D converter. This delay-time leads to stability problems of the control loop and is responsible for the reduced bandwidth of the amplifier in closed loop operation. Nevertheless a bandwidth of 5kHz at nominal load could be achieved using a switching frequency of only 25kHz.

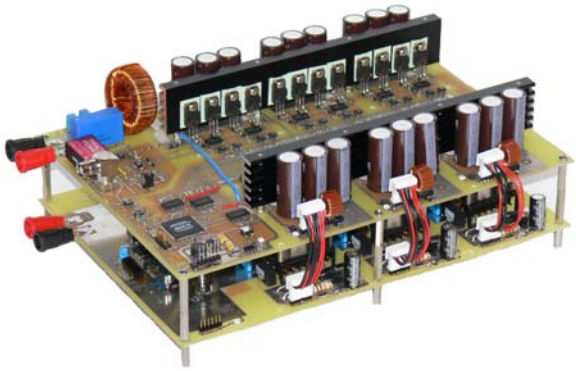


Fig.9: Realized laboratory prototype system.

6 References

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