A Novel SiC J-FET Gate Drive Circuit for Sparse Matrix Converter Applications

Marcelo L. Heldwein and Johann W. Kolar
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
ETH Zentrum / ETL H23, Physikstrasse 3
CH-8092 Zurich / SWITZERLAND / Europe
heldwein@lem.ee.ethz.ch kolar@lem.ee.ethz.ch

***Abstract*—Three-phase AC/AC Sparse Matrix Converters (SMC) show a low realization effort and a low control complexity and are therefore of potential interest for industry applications. In this paper a novel gate drive circuit for a SiC J-FETs to be employed in an All-SiC-SMC is proposed. The gate drive requirements of SiC J-FETSs are clarified and the operating principle of the driver circuit is discussed and practically verified in a bridge leg topology. The experimental analysis shows significant advantages of the proposed system over known SiC J-FET driver circuits concerning switching delay time and switching losses.**

Keywords – Drive Circuit; Silicon Carbide; JFET; Switching Behavior; Sparse Matrix Converter.

I. INTRODUCTION

According to [1], [13], [14] three-phase AC/AC *Sparse Matrix Converters* (SMC) show significant advantages over conventional matrix converters concerning realization effort and control complexity and are therefore of special interest for future industry applications.

For realizing a SMC in Si-IGBT technology (cf. **Fig. 1(a)**) the switching frequency is limited to relatively low values. Therefore, the input filter constitutes a significant share of the total converter volume. As presented in [2] latest Silicon Carbide (SiC) J-FETs would provide a way to increase the switching frequency at limited switching losses and/or without impairing the semiconductor utilization or conversion efficiency. Also, SiC J-FETs are able to conduct current in the source to drain direction as an anti-parallel diode is part of the semiconductor structure like given for conventional Si MOSFETs with the advantage of very small reverse recovery times. The resulting SMC schematic is depicted in **Fig. 1**(b) shows a remarkably simple structure.

For realizing an All-SiC-SMC employing SiC J-FETs and SiC Schottky diodes, the J-FET gate drive circuit is a key component. In the case at hand we define as target specifications considering the limited current carrying capability of available SiC J-FETs:

$U_1 = 230\ V_{rms}$	input phase voltage
$P_2 = 2.5$ kW	output power
$f_P = 150$ kHz	switching frequency.

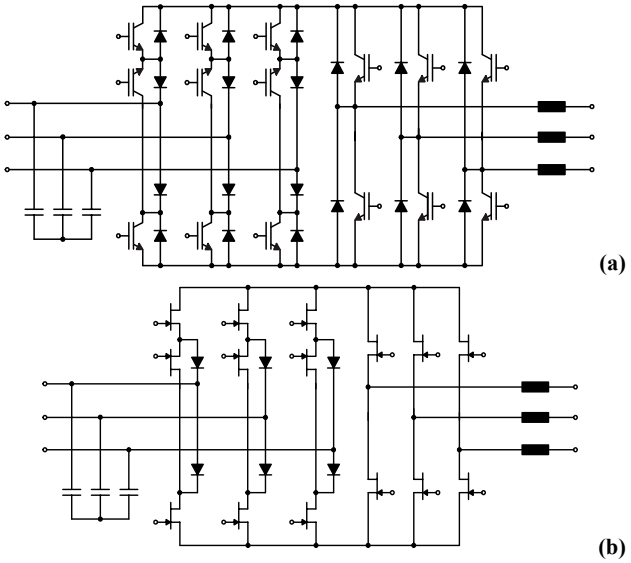

Fig. 1: Basic structure of the power circuit of a Sparse Matrix Converter (SMC); **(a)** realization based on Si-IGBTs; **(b)** SMC employing SiC J-FETs.

II. SIC J-FET DRIVER REQUIREMENTS

In the research on new materials and components for power electronics utilization SiC components show a large potential [5], [7], [15] as the conduction and switching losses could be reduced by a factor of 10 compared to Si devices and the device operating temperature could be significantly increased. SiC Schottky diodes are already available in the market [3], [7], [12], SiC turn-off power semiconductors [3]–[7], specifically SiC J-FET (Junction Field Effect Transistors) are under development and available as samples in the form of a cascode comprising the SiC J-FET and a low voltage Si power MOSFET (cf. **Fig. 2**) from Infineon/SiCED/IXYS [4], [6], [8].

These devices are specified for 4.5 A drain current and 1300 V breakdown voltage. The main reason for the cascode arrangement is the normally-on behavior of the J-FET which requires a negative gate voltage for turn off. The cascode is a normally-off device therefore the gate drive is identical to a conventional MOSFET. However, it results in higher conduc-

tion losses as another power semiconductor is inserted into the current path. Furthermore, the maximum admissible rate of change of the switching voltage (*dv/dt*) is limited by the intrinsic anti-parallel Si MOSFET diode. Another disadvantage is the limitation of the maximum device operating temperature caused by the Si MOSFET.

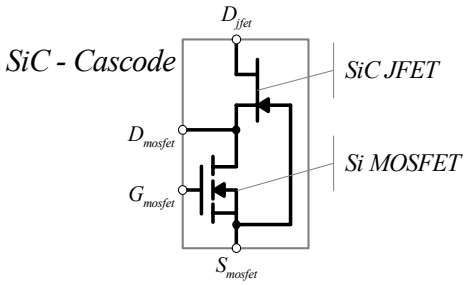

Fig. 2: SiC J-FET/Si low voltage MOSFET cascode.

Therefore, in the case at hand only the SiC J-FET should be utilized. There, special attention has to be paid to the gate driver circuit. The device pinch-off voltage is about -30 V [6], in order to avoid a turn on due to *dv/dt*, temperature drift, or different sample characteristics an even lower voltage should be applied. Here, a limiting factor is the gate source avalanche voltage, which should be approximately -40 V for this technology but varies between samples (a diagram showing the gate voltage/current characteristic in given e.g. in [10]). For the turn-off of the J-FET, the gate driver circuit has to apply a gate source voltage lower than the pinch-off voltage within very short time and it should also be capable to limit the gate rms current in order to limit the losses in case an avalanche does occur. A gate driver exhibiting such characteristics was proposed in [10] where also a comparison of the resulting J-FET switching losses to the cascode driven by a MOSFET driver circuit was performed. It has been found that for employing only the J-FET the switching losses are reduced by 9%. Therefore, the aim of this work is to achieve a further reduction of the switching losses for the same conditions.

III. PROPOSED GATE DRIVER CIRCUIT

A. Driver Circuit

Since the pinch-off voltage and the avalanche breakdown voltage of available SiC J-FET samples are not well defined, a gate current limiting has to be provided in order to limit the losses in case the gate voltage which has to be defined considering the most negative pinch-off voltage exceeds the avalanche voltage of a device. The basic idea of the proposed driver is to create a circuit which is able to adapt to the device to be driven concerning the presented requirements. The simplified circuit schematic is presented in **Fig. 3**.

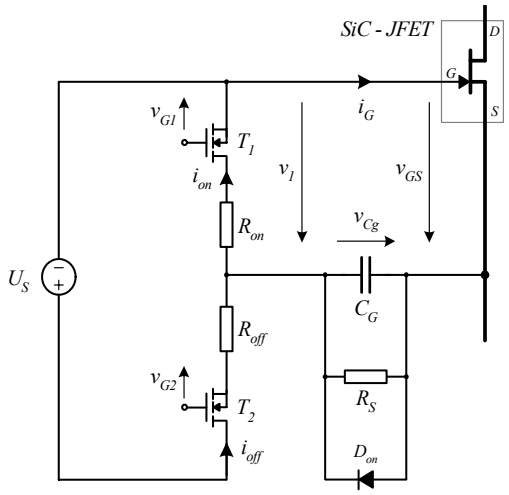

Fig. 3: Proposed SiC J-FET gate drive circuit.

B. Operating Principle

The circuit composed of T_1, T_2, R_{on}, R_{off} and U_S operates as a half-bridge, with limited peak output current capability and generates the voltage v_1 which is applied to the series connection of the J-FET gate and the parallel circuit R_S and C_G. A voltage higher than the maximum pinch-off voltage of any device to be driven is supplied by the voltage source U_S, what means that this voltage could cause an avalanche condition for a device showing a low avalanche breakdown voltage. In order to prevent such condition the parallel circuit R_S // C_G // D_{on} is placed in series with the J-FET gate and creates an impedance which is capable to limit the current and at the same time capable to supply high current peaks during the transitions at turn-on and turn-off. The resistor R_S is of high value and should just ensure a current flow within the device turn-off interval. The capacitor C_G should be dimensioned large enough in order to provide the desired transient current peaks but small enough in order not to let the gate to source voltage v_{GS} remain at a voltage higher than the breakdown voltage for longer time, thus reducing the gate driver losses. Diode D_{on} guarantees that the gate to source voltage is kept close to zero within the turn-on interval and prevents voltage oscillations caused by stray inductances, the capacitor C_G and the J-FET gate to source impedance.

In the following the simplified operating behavior of the gate drive circuit is described based on Fig. 3 and on the waveforms depicted in **Fig. 4**. For limiting to the essentials the discussion is based in the following simplifications:

1. The J-FET gate to source impedance is modeled as a variable capacitance, which increases rapidly when the gate to source voltage is close to the breakdown voltage;
2. MOS-FETs T_1 and T_2 and Diode D_{on} are considered ideal.

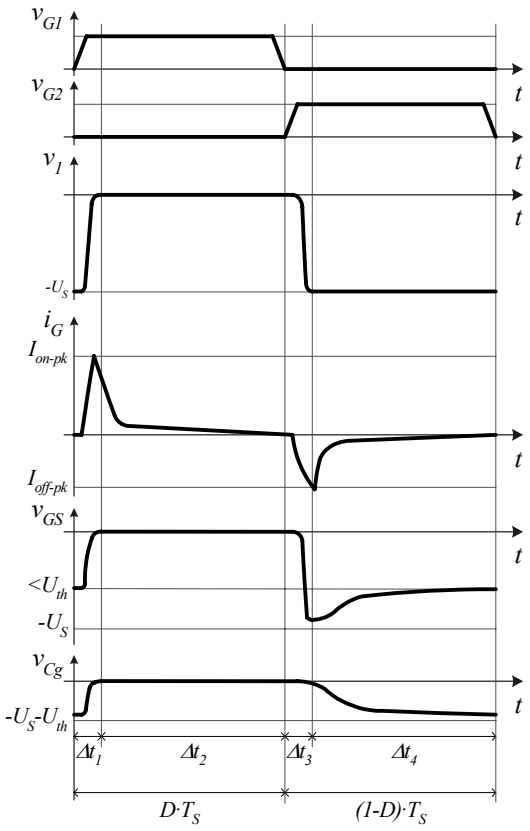

Fig. 4: Theoretical time behavior of characteristic quantities of the proposed driver circuit.

Time interval Δt_1: Voltage v_{GS} is previously set to values lower than the pinch-off (threshold) voltage of the J-FET (U_{th}), T_2 is turned-off and the voltage v_{Cg} is positive. The transistor T_1 is then turned-on what causes voltage v_1 to rise with a rate limited by the series impedance of R_{on}, C_G and the J-FET gate to source impedance. The charge stored in C_G helps the gate current to increase thus decreasing the v_{GS} rise-time and forcing a faster turn-on. At the end of Δt_1 the turn-on of the SiC J-FET is completed.

Time interval Δt_2: The gate current i_G decreases until the C_G is discharged and then is kept at low value since v_{GS} is zero. The JFET is conducting during this period which ends when T_1 is commanded to turn-off.

Time interval Δt_3: Previously, the voltage v_{GS} is close to zero, T_1 is turned-off and the voltage v_{Cg} is zero. The transistor T_2 is then turned-on what causes voltage v_1 to fall to its minimum (U_S - v_{Cg}) with a rate limited by the series impedance of R_{off}, C_G and the JFET gate to source impedance.

Time interval Δt_4: The gate current i_G increases further due to the J-FET gate running into avalanche mode. The increasing current causes a decrease of v_{Cg}, and/or increase of the charge stored in C_G and results correspondingly is an increase of v_{GS}. This reduces the avalanche current in the J-FET gate until v_{GS} goes below the avalanche limit and i_G is reduced to a level that only ensures that the J-FET remains in the turn-off state.

IV. Experimental Analysis

A. Experimental Setup

The switching behavior as well as the performance of the proposed driver circuit are evaluated using the test circuit shown in **Fig. 5**. There, the Si MOSFETs (M_1 and M_2) are kept out of the main current paths by connecting the gate to the source. The upper J-FET S_1 operates as free-wheeling diode, accordingly U_{G1} is set at a voltage lower than the pinch-off voltage; the lower J-FET S_2 is operating in switching mode gated by the proposed driver circuit. The inductor L_L impresses the load current and ensures a constant current within the switching intervals.

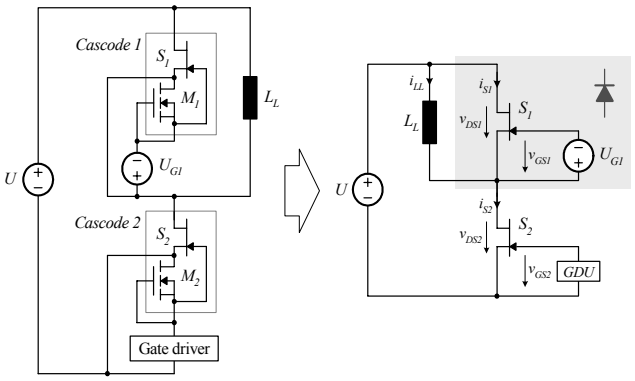

Fig. 5: Test circuit employed for analyzing the switching behavior.

The actual gate driver circuit schematic is shown in **Fig. 6**. The input pulses are created by a pulse generator and isolated using an opto-coupler. Since high speed switching is required, MOSFETs rated for 60 V are employed for T_1 and T_2. For driving the MOSFETs the circuit composed of C_2, C_3, R_3, R_4, R_5, R_6, T_4, T_5, D_1, D_2 and D_3 is applied. This circuit provides 15 V gate pulses with fast turn-off and slower turn-on time providing a reduction of the peak current resulting during the commutations between T_1 and T_2.

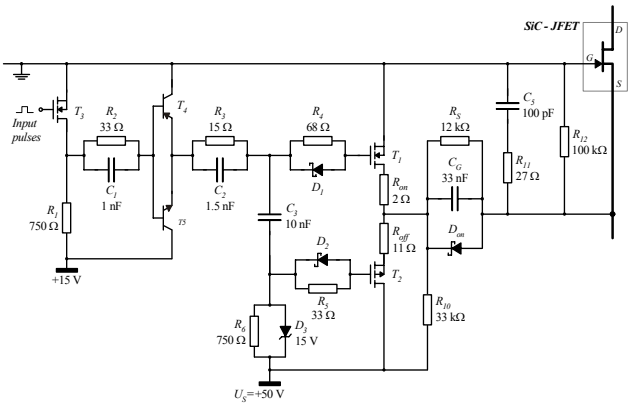

Fig. 6: Gate driver circuit schematic.

In order to obtain measurement results that could be compared to [10] a power circuit presenting equal characteristics was designed. Especially, the same inductor and the same cur-

rent probe were employed. The measurement setup schematic is depicted in **Fig. 7**.

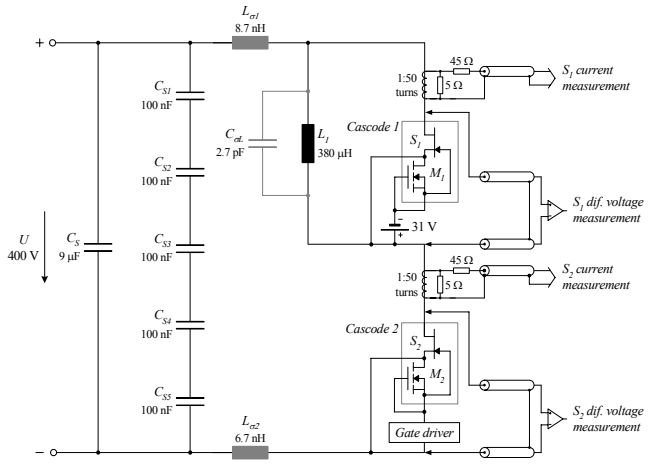

Fig. 7: Measurement setup.

The capacitor C_S is realized using 6 polypropylene capacitors of 1.5 µF in parallel; capacitors C_{S1} to C_{S5} are SMD capacitors placed close to the power switches in order to avoid large stray inductances ($L_{\sigma 1}$ and $L_{\sigma 2}$). The power switches are connected to an aluminum heat-sink carrying a heating resistor which allows setting a defined device junction temperature ranging from room temperature up to 125 °C. The inductor L_L [10] is realized with minimum stray capacitance $C_{\sigma L}$ using a series connection of four partial inductors, each constructed with 10 turns on a ferrite core EPCOS B66291 with an air gap of 0.1 mm. The resulting inductor shows an inductance of approximately 380 µH in parallel with a 2.7 pF capacitance and a saturation current around 9 A.

The switching losses were calculated using the osciloscope by multipling and integrating the measured voltages and currents after deskewing the probes. Table I lists the equipments used for the switching loss measurements.

TABLE I. MEASUREMENT EQUIPMENTS

Equipment	**Characteristics**
Digital storage scope	LeCroy *Wavepro* 950 (1 GHz, 1 GS/s);
Differential voltage probe	LeCroy DXC100A (100:1, 1 MΩ, 10.5 pF, 1 kV)
Differential amplifier	LeCroy DA1855A
Current measurement	R10/N30 ferrite core employed as an AC current transformer with a turns ratio of 1:50 [11]

B. Experimental results

1) Gate driver

In **Fig. 8** the main waveforms for the gate driver circuit operating are shown for zero drain current, 125 °C J-FET junction temperature, 400 V DC link voltage, and at a switching frequency of 150 kHz. The rise and fall times for the JFET gate to source voltage v_{GS} are about 50 ns and 20 ns respectively. A gate current peak current of approximately 2.5 A is observed for the device turn-on transition. The voltage v_{Cg} across the capacitor in series with the gate is shown in Fig. 9(a). The total measured power dissipation in the driver circuit is approximately 2.65 W for the worst operating point. The main part of this power loss is supplied by the supply voltage U_S where the measured power consumption is 1.75 W.

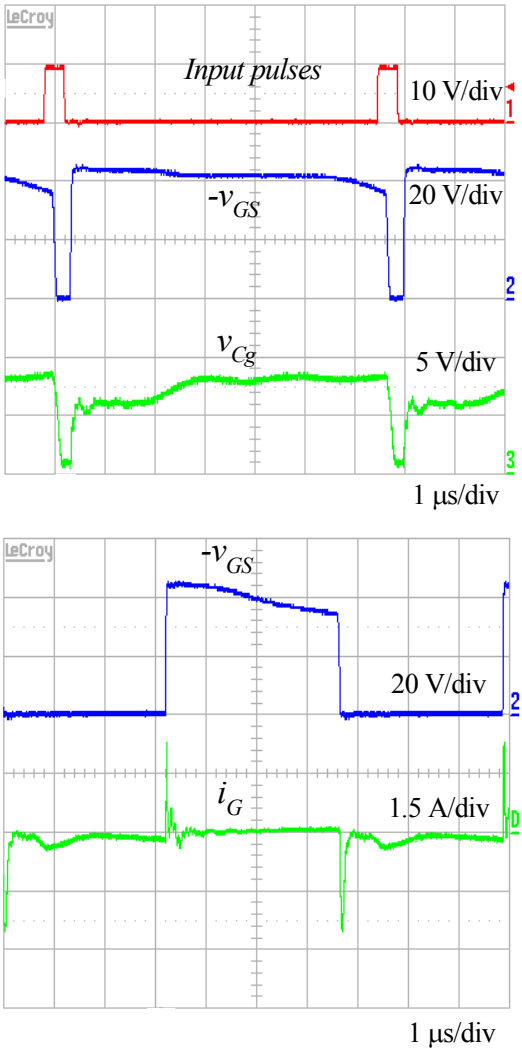

Fig. 8: J-FET gate-to-source voltage v_{GS}, gate current i_G, and capacitor voltage v_{Cg} for two different duty cycles.

Waveforms for switching 4 A / 400 V under 125 °C junction temperature are depicted in **Fig. 9**. The turn-on losses of S_2 are increased by the reverse recovery current of S_1 (cf. Figs.9(a) and (c)). The reverse recovery behavior is shown in **Fig. 10** for different junction temperatures. The turn-on time of S_2 and/or turn-off time of S_1 is approximately 40 ns.

The turn-off waveforms for S_2 are shown in Fig. 11(b). Although the voltage rises in a very short time of ≈ 20 ns, no overshoot or strong oscillations occur. At these conditions, the measured *dv/dt* is approximately 16 kV/µs for the turn-off transition and 13 kV/µs for the turn-on of S_2.

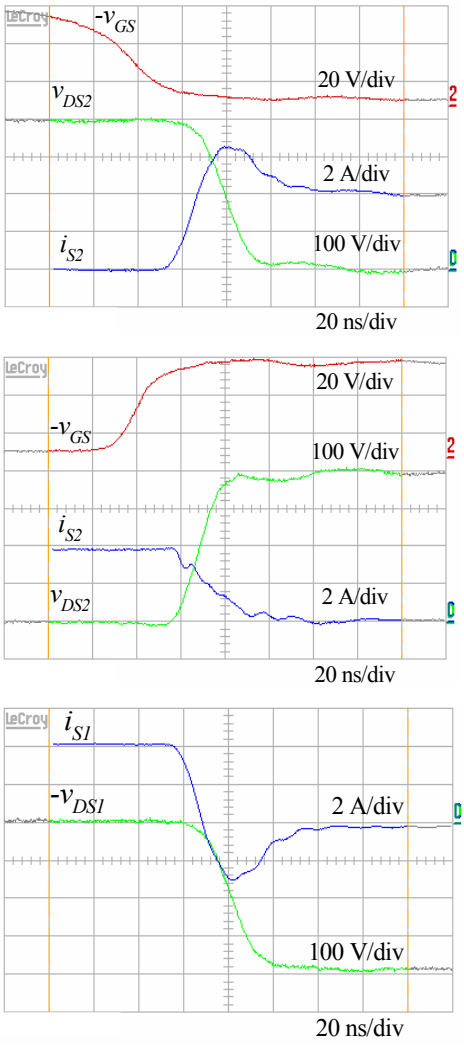

Fig. 9: Switching waveforms for 125 °C junction temperature; **(a)** turn-on of S_2; **(b)** turn-off of S_2; **(c)** turn-off of S_1. Shown are: J-FET gate-to- source voltage v_{GS}, current and voltage, i_{S1} and v_{DS1} of transistor S_1, and i_{S2} and v_{DS2} of transistor S_2.

The resulting switching loss components, i.e. the reverse recovery losses $E_{r\text{-}r}$ of S_1 and the turn-on losses E_{on} and turn-off losses E_{off} of S_2 are shown in **Fig. 11** for different junction temperatures and switched currents while maintaining a constant DC supply voltage of 400 V.

A comparison to the measurement results given in [10] is provided in **Fig. 12** for 125 °C junction temperature, 4 A switched current and constant supply voltage (400 V) where the total losses are again splitted into components according to Fig.11.

According to Fig. 12 employing the proposed gate drive circuit results in a reduction of the switching losses of ≈ 50% as compared to the cascode devices and of 45% as compared to [10].

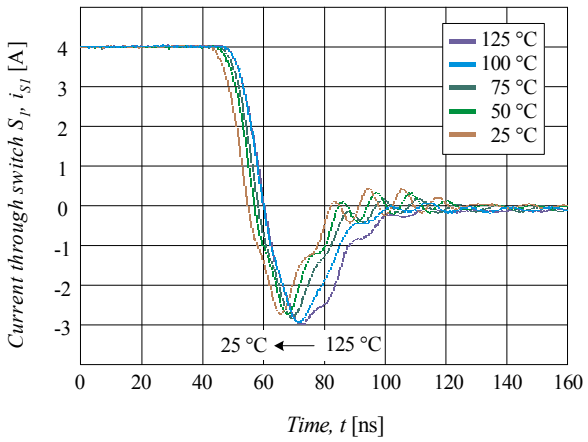

Fig. 10: Dependency of the reverse recovery current of S_1 on the junction temperature.

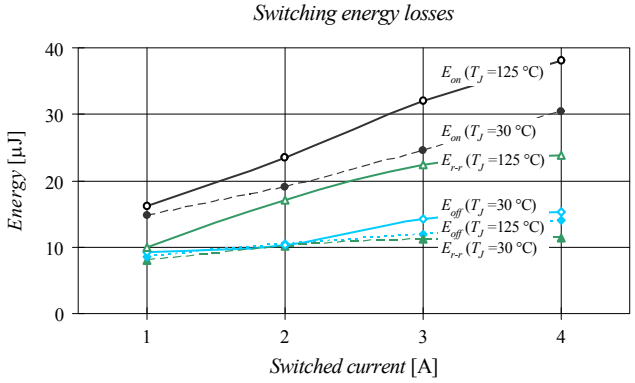

Fig. 11: Switching energy loss in dependency on the switched current.

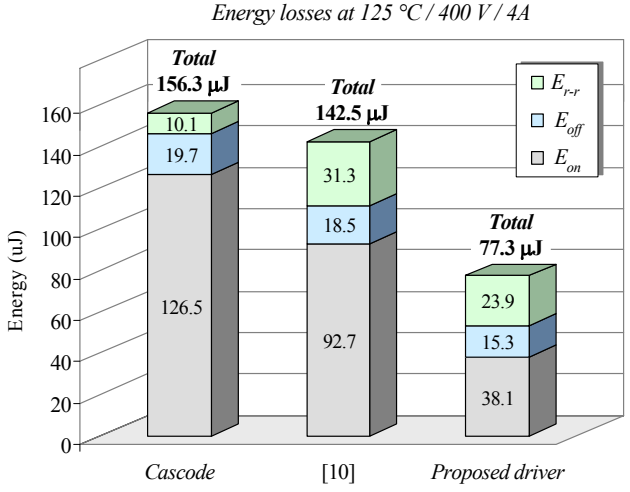

Fig. 12: Switching energy losses for different driver circuits and semiconductor technologies when switching 4A / 400 V at a junction temperature of 125 °C.

V. CONCLUSIONS

The gate drive circuit proposed in this paper is part of a research effort which is aiming for the realization of a 2.5kW All-SiC-SMC switching at 150 kHz. The operation of the gate driver circuit was proven to follow the theoretical considerations and to provide low switching times and/or J-FET switching losses. The power consumption of the driver circuit is 2.65 W for a switching frequency of 150 kHz.

The switching behavior of the SiC J-FET in combination with the proposed driver circuit was analyzed. In comparison to [10] a considerable reduction of the switching losses has been achieved which would account for approximately 8 W in the transistor S_2 of a bridge leg switching a current of 4A at 400V (output power in the range of 1kW) with a switching frequency of 150 kHz for a junction temperature 125 °C.

In summary, a SiC J-FET / Si MOSFET cascode configuration ensures simple controllability of the normally-on J-FET but does not represent the most advantageous choice concerning a minimization of the switching and conduction losses. However, for employing only the J-FET part of a cascode special attention has to be paid to the system start-up and shutdown and possible failures of the gate drive power supply in order to achieve a comparably high reliability of the system operation.

ACKNOWLEDGMENT

The authors would like to thank the *SiCED Electronics Development GmbH* for providing samples of latest SiC turn-off power semiconductor technology.

REFERENCES

[1] **Kolar, J.W., Baumann, M., Shafmeister, F, and Ertl, H.**: *Novel Three-Phase AC-DC-AC Sparse Matrix Converter*. Proceedings of the 17th IEEE Applied Power Electronics Conference and Exposition, Dallas (Texas), USA, March 10-14, Vol. 1, pp. 777-791 (2002).

[2] **Shafmeister, F, Herold, S., and Kolar, J.W.**: *Evaluation of 1200V-Si-IGBTs and 1300V-SiC-JFETs for Application in Three-Phase Very Sparse Matrix AC-AC Converter Systems*. Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach (Florida), USA, February 9-13, Vol. 1, pp. 241-255 (2003).

[3] **Reimann, T., Petzoldt, J., Zverev, I., Mitlehner, H., and Friedrichs, P.**: *Application of SiC Devices in Power Supplies*. Proceeding of the 10th International Power Electronic and Motion Control Conference, Sept. 9-11, Cavtat & Dubrovnik, Croatia (2002).

[4] http://www.siced.de/

[5] **Stephani, D.**: *Prospects of SiC Power Devices from The State of the Art to Future Trends*. Proceedings of the 45th International Power Electronics Conference, Nuremberg, May 14-16, K2 (2002).

[6] **Mitlehner, H., Friedrichs, P., Schörner, R., Dohnke, K.O., Elpelt, R., and Stephani, D.**: *Ultra Low Loss and Fast Switching Uunipolar SiC-Devices*. Proceedings of the 45th International Power Electronics Conference, Nuremberg, May 14-16, pp.137-142 (2002).

[7] **Lorenz, L., and Mitlehner, H.**: *Key Power Semiconductor Device Concepts for the Next Decade*. IEEE Industry Applications Conference 37th IAS Annual Meeting, Pittuburg, Pensilvania, USA, October 13–18, Vol. 1, pp. 564 – 569 (2002).

[8] **Tournier, D., Godignon, Montserrat, J., Planson, D., Raynaud, C., Chante, J.P., Sarrus, F., Bonhomme, C. and de Palma, J.F.**: *A 4H-SiC High Power Density VJFET as Controlled Current Limiter*. IEEE Industry Applications Conference 37th IAS Annual Meeting, Pittuburg, Pensilvania, USA, October 13–18, Vol. 1, pp. 570–575 (2002).

[9] **Ållebrand, B, and Nee, H.-P.**: *Design of a Gate Drive Circuit for Use with SiC JFETs*. Proceedings of the 2002 Nordic Workshop on Power and Industrial Electronics, Stockholm, Sweden, August 12-14 (2002).

[10] **Mino, K., Herold, S., and Kolar, J.W.**: *A Gate Drive Circuit for Silicon Carbide JFET*. Proceedings of the 29th Annual Conference of the IEEE Industrial Electronics Society, Roanoke (VA), USA, November 2-6, pp. 1162 - 1166 (2003).

[11] **Laimer, G., and Kolar, J.W.**: *Wide Bandwidth Low Complexity Isolated Current Sensor to be employed in a 10kW/500kHz Three-Phase Unity Power Factor PWM Rectifier System*. Proceedings of the 33rd IEEE Power Electronics Specialists Conference, Cairns, Australia, June 23-27, Vol. 3, pp. 1065-1070 (2002).

[12] http://www.cree.com/

[13] **Wei, L., and Lipo, T.A.**: *A Novel Matrix Converter Topology with Simple Commutation*. Record of the IEEE Industry Applications Society Annual Meeting, Chigago, USA (2001).

[14] **Wei, L., Lipo, T.A., and Chan, H.**: *Matrix Converter Topologies with Reduced Number of Switches*. Proceedings of the 33rd Power Electronics Specialists Conference, Cairns, Australia, June 23-27, Vol. 3, pp. 57-63 (2002).

[15] **Abou-Alfotouh, A., Radun, A., Chang, H.-R., and Winterhalter, C.**: *A 1MHz Hard-Switched Silicon Carbide DC/DC Converter*. Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach (Florida), USA, February 9-13, Vol. 1, pp. 132-138 (2003).

[16] **Yu, H., Lai, J., Huang, X., Zhao, J.H., Zhang, J., Hu, X., Carter J., and Fursin, L.**, *Gate Driver Based Soft-Switching SiC Bipolar Junction Transistor*. Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach (Florida), USA, February 9-13, Vol. 1, pp. 968–973 (2003).