Differential Mode EMC Input Filter Design for Three-Phase AC-DC-AC Sparse Matrix PWM Converters

M. L. Heldwein, T. Nussbaumer; and J. W. Kolar
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
ETH Zentrum / ETL H23, Physikstrasse 3
CH-8092 Zurich, SWITZERLAND / Europe
heldwein@lem.ee.ethz.ch nussbaumer@lem.ee.ethz.ch kolar@lem.ee.ethz.ch

Abstract — The design of a differential-mode EMC input filter for a three-phase AC-DC-AC Very Sparse Matrix Converter intended for electrical machine drive applications is discussed in this paper. A review of the steps to be performed in the course of the filter design is presented and a detailed mathematical model of the EMI test receiver for quasi-peak measurement of conducted emissions in the frequency range of 0.15…30 MHz is established. Furthermore, formulas for the estimation of the quasi-peak detector output based on the LISN output voltage spectrum are provided. As experimentally verified by using a novel three-phase CM/DM separator this procedure allows an accurate prediction of the converter differential mode conducted emission levels and therefore could be employed in the design process for ensuring compliance to relevant EMC standards.

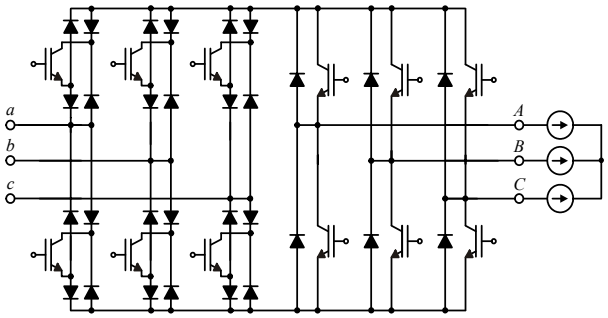


Fig.1: Basic structure of a three-phase AC-DC-AC Very Sparse Matrix Converter (VSMC).

I. INTRODUCTION

There are two main reasons for employing EMC input filters, namely: (i) to prevent electromagnetic interference of the considered power electronic converter with electronic systems present in the neighboring environment, and (ii) to avoid a disturbance of the power converter operation by sources of electromagnetic noise in the surrounds [1], [2]. With this aim, international organizations have been constantly working on standards which have to be considered when designing the EMI filter of a power electronic system. The main requirements and critical aspects are compiled in **TABLE I**.

In this paper, the design of high performance differential mode (DM) input filters for a three-phase AC-DC-AC Very Sparse Matrix Converter (VSMC) [3] (cf. **Fig.1**) is discussed. The filter design steps presented in **Section II** provide general guidelines being applicable to any current-source type PWM converter system. The design procedure is based on a detailed mathematical model of the EMI test receiver for measuring

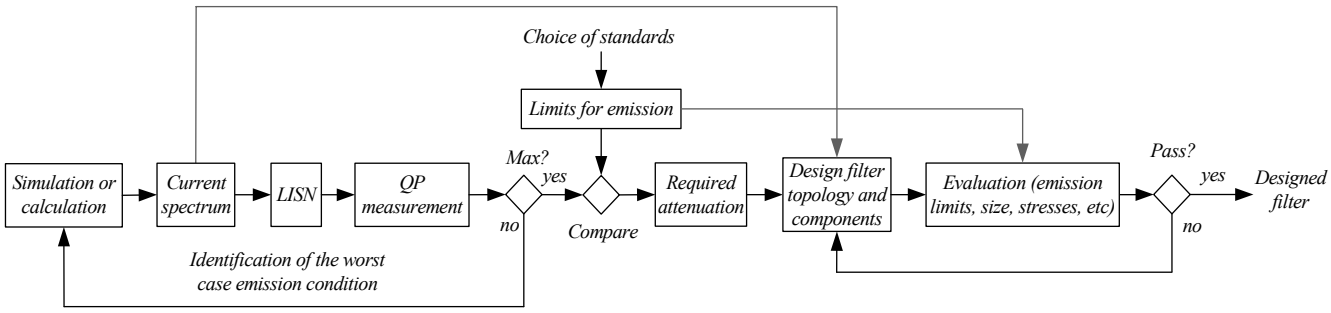


Fig.2: EMC input filter design procedure shown in graphical form.

TABLE I – DM INPUT FILTER DESIGN REQUIREMENTS AND CRITICAL ASPECTS.

General requirements	Critical aspects
- Fulfillment of international EMC regulations on differential mode what translates into minimum filter attenuation requirement at given frequencies; - Minimization of input current fundamental displacement factor ($\cos\phi_1$); - Limitation of the physical size/energy stored in the filter components; - Sufficient passive damping causing minimum losses, in order to avoid oscillations also for no-load operation ; - Avoidance of filter resonances at multiples of the switching frequency; - Minimization of the filter output impedance, in order ensures system stability and minimizes control design restrictions.	- Uncertainty in the mains impedance which could shift given resonant frequencies or introduce novel resonant circuits with low damping; - Modeling of the EMC test receiver in order to properly define the required filter attenuation in the design process; - Prediction of the high-frequency filter behavior which is influenced / determined by parasitics of the filter elements; - Low complexity and/or low component count of the filter (translating into low costs); - Influence of the filter on the overall system control stability.

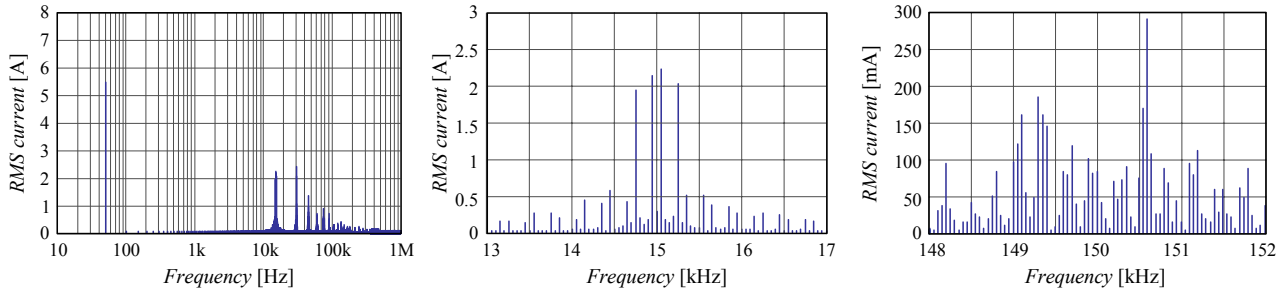


Fig.3: (a) Frequency spectrum of the converter input current I_{dm}; **(b)** zoom around the switching frequency at 15 kHz; **(c)** zoom around the first switching frequency harmonic being located in the frequency range 0.15…30 MHz (at 150 kHz).

conducted emissions (CE) in the frequency range of 0.15…30 MHz (cf. Section II.E). As verified by experimental analysis (cf. **Section III**) employing a novel three-phase common mode/ differential mode (CM/DM) noise separator this allows an accurate prediction of the converter behavior regarding DM emissions. Accordingly, compliance to applicable EMC standards can be ensured already in the design process what represents an important step towards a virtual prototyping of the converter system resulting in shorter total design time and/or reduced overall development costs. Finally, in **Section IV** topics to be treated in the course of further research are summarized and discussed briefly.

II. FILTER DESIGN PROCEDURE

In the following the filter design procedure and the test receiver modeling are discussed. **Fig.2** illustrates the design steps in graphical form.

A. Applicable Standards and Limits for Emission

As a first step of the filter design one has to specify the admissible maximum DM conducted emission levels with reference to relevant EMC standards taking into consideration the type of equipment, the region and the environment where it will be utilized. Usually specific regulations for the equipment at hand are applied and in case no specific standard is available, generic standards are employed. In this paper the focus will be on the frequency range of **0.15…30 MHz**, the measurement techniques defined in **CISPR 16** [4] and the emission limits for drive systems defined in **EN 61800-3**, **Tab.6** [5] which are in the case at hand identical to **CISPR 22 class B** [6].

B. Identification of the Worst Case Operating Condition

As a basis for defining the required filter attenuation the largest emission condition in the frequency band of interest has to be identified. There, one has to analyze the input current frequency spectrum of the converter in the whole operating range, i.e. for varying modulation depth, output power, input and output frequencies and further parameters which might take influence on the spectral composition of the input current.

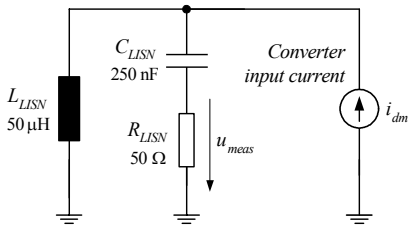


Fig.4: Simplified high-frequency model considered for determining the conducted emissions. The converter is replaced by a current source i_{dm}; no input filter is present. Based on the measurement results the required filter attenuation is calculated.

The DM conducted emissions for the VSMC are due to the discontinuous input currents with pulse frequency. For a Sparse Matrix Converter the following variables are taking direct influence on the high-frequency input current harmonics: (1) **type of load,** where for purely resistive load the highest output current ripple and/or the highest input current harmonics are observed. However, as the main application of the converter is for variable-speed drives this is not considered further but an inductive load (sinusoidal output current) is assumed in the following; (2) **modulation index** (M) where the highest amplitudes of the input current harmonics are occurring around M = 0.5; (3) **the output frequency** (f_2), where the switching frequency harmonics are increasing with increasing output frequency. Accordingly, we use as worst case conditions for the following digital simulations:

Input RMS line voltages (U_1)	**3 x 400 V**
Modulation index	M = **0.5**
Output frequency	f_2 = **200 Hz**
Output power	P_2 = **3.75 kW**
Current displacement angle	ϕ_2 = **30° .**

The spectrum of the simulated converter input current resulting for this operating point is depicted in **Fig.3**.

C. Converter Single-Phase Equivalent Circuit

Due to the phase symmetry of the converter topology and the

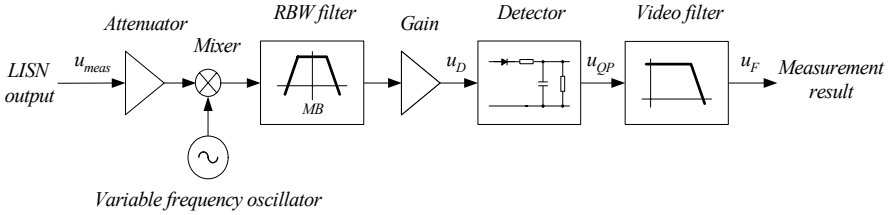


Fig. 5: Simplified heterodyne measurement and QP detection model of the test receiver. Dependent on the *Oscillator* frequency the *Mixer* shifts the frequency of interest to an intermediate frequency (IF) where the measurements is performed employing a fixed-frequency band-pass filter (RBW filter, cf. Fig.6a) according to CISPR 16.

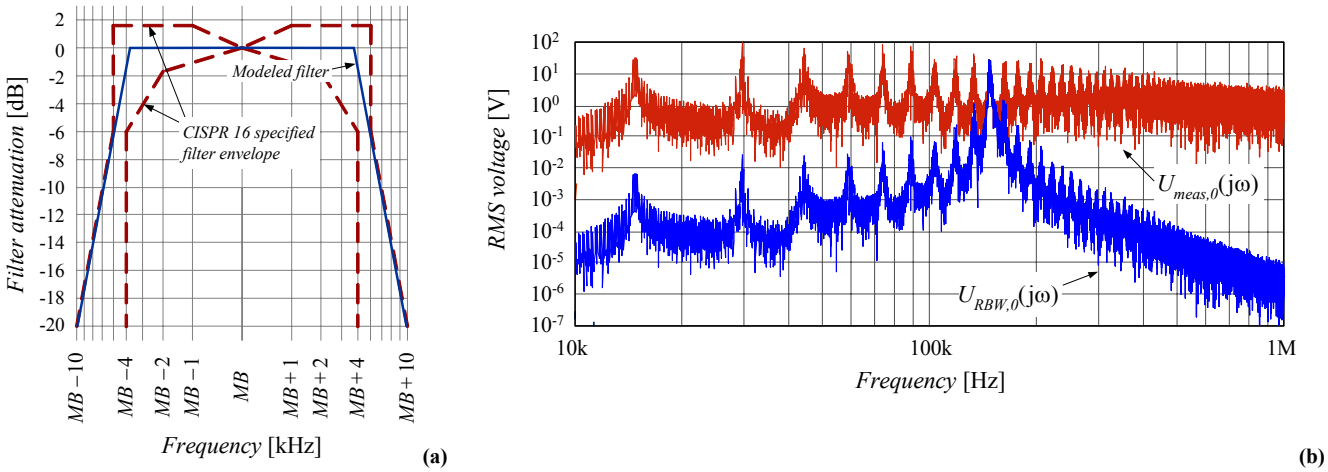


Fig.6: (a) Upper and lower envelope of the characteristic of the resolution bandwidth (RBW) filter as specified in CISPR 16 and filter characteristic used when modeling the RBW filter; **(b)** voltage at the input and at the output of the RBW filter for *MB*=150 kHz. Index *0* denotes that no input filter is present.

control and the missing connection of the converter power circuit to the mains neutral the filter design can be restricted to a single-phase equivalent (cf. **Fig.4**), i.e. the converter can be replaced in the following steps by a single phase current source with a current spectrum defined by the simulated worst case operating condition.

D. LISN

A Line Impedance Stabilizing Network (LISN) is specified for most of the conducted emission tests in order to guarantee the reproducibility of the measurements. Furthermore, a LISN provides an interface between the equipment under test and the test receiver. A simplified mid- to high-frequency (0.15 to 30 MHz) equivalent circuit of the LISN according to CISPR 16 is shown in Fig.4. The voltage u_{meas} at the LISN output is applied to an EMC test receiver or appropriate spectrum analyzer (R_{LISN} = 50 Ω is the input resistance of the test receiver).

For determining the measured voltage spectrum of u_{meas} the converter current spectrum $I_{dm}(j\omega)$ is multiplied by the LISN transfer-function

$$U_{meas}(j\omega) = I_{dm}(j\omega) \cdot \left[\frac{U_{meas}(j\omega)}{I_{dm}(j\omega)} \right] . \qquad (1)$$

E. Test Receiver

The input signal (u_{meas}) of the receiver is processed according to CISPR 16 using a heterodyne technique, i.e. for measuring at a given frequency *f* the spectrum is shifted to a fixed frequency (*IF*) where the band-pass filtering according to Fig.6(a) is performed. This allows analyzing a wide frequency range without changing the center frequency (MB) of the band-pass filter by properly adapting the oscillator frequency defining the frequency shift. A block diagram showing the basic functions of the frequency measurement system is depicted in **Fig.5**.

The bandwidth of the band-pass filter (*RBW filter*) differs dependent on the frequency band of interest and is defined as 9 kHz at -6 dB for 0.15…30 MHz as shown in **Fig.6**(a) where also the simplified filter characteristic employed for simulation the receiver output is depicted. The fixed value *MB* denotes the band-pass center frequency. In the simulation model of the test receiver the *MB* can be directly located at the frequency under consideration and shifted for a frequency sweep, therefore, a modeling of the oscillator and the mixer can be omitted.

The effect of the *RBW filter* when applied to the spectrum of the measured LISN output voltage u_{meas} is shown in Fig.6(b) for the specified operating conditions of the VSMC and *MB*=150 kHz. It can be seen that the spectral components around *MB* (i.e. within the band-pass range) maintain their amplitude while the remaining spectral components are suppressed and therefore don't contribute to the measurement result.

Finally, signal level is adapted in a way (block *Gain* in Fig.5) that in case the input signal is formed by only a single harmonic component inside the RBW the RMS value of this sine-wave results as output signal. This means that the total DC gain of the whole measurement system should be 1/√2.

The Quasi-Peak (QP) *Detector* is also specified in CISPR 16 and shows different time constants for the charging and discharging of the output capacitor C_{QP}. Furthermore, different sets of time constants have to be considered for different frequency ranges under consideration. The QP *Detector* can be modeled [2], [7], [8] as shown in **Fig.7**(a). For *0.15…30* MHz the charging time constant is specified as *1* ms, while the discharging

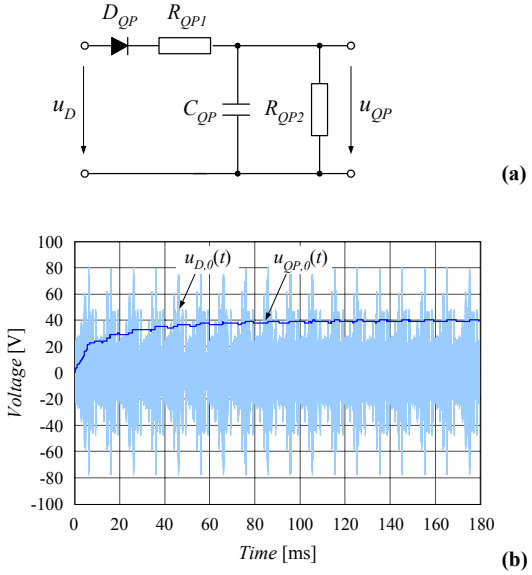


Fig.7: (a) Quasi-peak (QP) detector model; **(b)** Effect of the quasi-peak detector to the voltage $u_{D,0}$. The index 0 denotes that the measurements are performed without input filter.

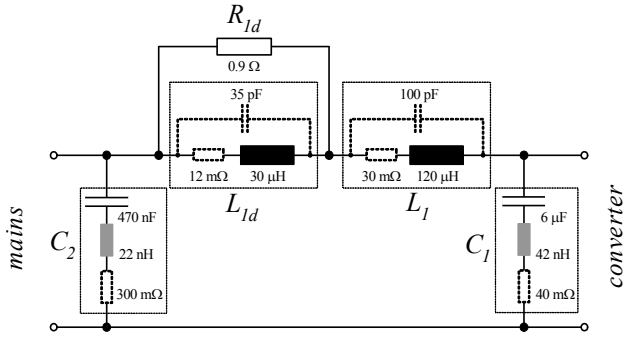


Fig.8: Input filter single-phase equivalent circuit providing the required attenuation including the parasitics of the inductive and capacitive elements.

time constant is *160* ms. The final value for the measurement is obtained through the averaging of the output voltage of the QP detector what is performed in the *Video filter* which is characterized by a time constant of *160* ms for 0.15…30 MHz.

As a result of the QP detection, the measured value is larger than the RMS value of the voltage at the LISN output in case more than one harmonic is present inside the RBW. Therefore, the filter design cannot be based only on an individual harmonic of high amplitude but has to consider the calculated QP detection output values.

F. Calculation of Required Attenuation

Due to the low time constant the measured *Video filter* output voltage $u_{F,0}$ is close to the average value of $u_{QP,0}$ and in the case at hand for *MB=150* kHz it is

$$u_{F,0} = u_{QP,0,avg} = 35.7\ \text{V} = 151\ \text{dBµV}. \tag{2}$$

By comparing the result to the limits specified for *f=150* kHz, the required attenuation of the input filter including a margin of *6* dB is calculated as

$$\begin{aligned} Att_{req}\left[\text{dBµV}\right] &= U_{meas,0,150kHz}\left[\text{dBµV}\right] - Limit_{CISPR,150kHz}\left[\text{dBµV}\right] \\ &+ Margin\left[\text{dBµV}\right] = 91\text{dB} \end{aligned} \tag{3}$$

G. Selection of the Filter Components

In order to achieve the required attenuation a two-stage filter as shown in **Fig.8** is employed where *Section 1* is formed by C_1-L_1-L_{1d}, and *Section 2* is formed by C_2 and the inner impedance of the LISN/test receiver (Z_{LISN}).

For the filter dimensioning several degrees of freedom (basically, the positioning of cut-off frequencies and the type and extent of damping) are given and some nonlinear restrictions (like discrete available capacitance values, the maximum admissible output impedance, the maximum admissible reactive power - which defines the current consumption at no load, and maximum current and voltage stresses) have to be considered.

Furthermore, the parasitics of the filter components have to be taken into account. Therefore, the dimensioning can not be in closed form, but has to be performed step-by-step starting with the determination of the ranges of the component values.

- **Capacitor C_1**

The capacitor C_1 is placed directly at the rectifier input and is selected such that the voltage ripple peak-to-peak value is limited to about ±*5…8* % in order to prevent a distortion of the output voltage and to limit the voltage stress on the power semiconductors. In the case at hand this translates into C_1=*4…8* µF.

- **Inductor L_1**

Both filter sections are contributing to the required filter attenuation. For stability reasons the attenuation of *Section 1* has to be higher than that of *Section 2*, which leads to a lower cut-off frequency of *1* compared to *2* [9]. Usually, $f_{cutoff,sec1} \approx 0.1 f_{cutoff,sec2}$ is an advantageous selection, which results in an attenuation range for *Section 1* of Att_{sec1}[dB]=*0.6…0.7*Att_{req}[dB]. With

$$f_{cutoff,\text{sec}1} = \frac{150\text{kHz}}{\sqrt{10^{Att_{\text{sec}1}[\text{dB}]/20}}} = \frac{1}{2\pi \cdot \sqrt{L_1 C_1}} \tag{4}$$

the inductance value is found in the range of

$$L_1 = \frac{10^{Att_{\text{sec}1}[\text{dB}]/20}}{4\pi^2 \cdot C_1 \cdot (150\text{kHz})^2} = \frac{10^{(0.6...0.7)\,Att_{\text{sec}1}[\text{dB}]/20}}{4\pi^2 \cdot (4...8)\,\mu\text{F} \cdot (150\text{kHz})^2} = \tag{5}$$
$$= 76...431\ \mu\text{H}$$

- **Inductor L_{1d}**

The inductor L_{1d} is normally determined by the damping ratio, $n=L_{1d}/L_1$, which should be selected only high enough in order to provide sufficient damping. A high value of n would provoke high filter output impedance which would take influence on the converter stability (for higher filter output impedances the stability of the converter control is more difficult to ensure [10], [11]). Here n=*0.1…0.5* is selected and accordingly L_{1d}=*7.6…215* µH is obtained.

- **Damping Resistor R_{1d}**

For an optimum damping of the filter resonanceR_{1d} has to be selected according to (6)

$$R_{1d} = \sqrt{\frac{L_1}{C_1}} \cdot \frac{1+n}{n} \cdot \sqrt{\frac{(2+n)\cdot(4+3n)}{2\cdot(1+n)\cdot(4+n)}}\ . \tag{6}$$

(only valid for the filter topology at hand, for other topologies details can be found in [11], [12]).

- **Capacitor C_2**

The second stage of the filter (*Section 2*) is formed by the capacitor C_2 in combination with the LISN/test receiver network (R_{LISN} = *50* Ω, L_{LISN} =*50* µH, C_{LISN} =*250* nF (cf. Fig.4 and Fig.8) and has to provide an attenuation of Att_{sec2}[dB] = Att_{req}[dB]−Att_{sec1}[dB] at *MB=150* kHz. This directly determines the value of C_2.

- **Optimization and Final Selection of Filter Components**

After determining the ranges for all filter components as described above, a recursive optimization process has to be followed considering the following points:

- Total gain value ($U_{meas}/I_{dm} \rightarrow Att_{req}$). This transfer function has to include finally all parasitics of the inductors and capacitors. As presented in Fig.8, inductors are modeled including a series resistance and a parallel capacitance and capacitors are modeled including a series resistance and a series inductance. In the case at hand the influence of the parasitics is about *1.72* dB at *150* kHz but will be more pronounced at higher frequencies.
- The maximum energy in the inductors and the maximum capacitor charge should be minimized in order to ensure a low overall filter volume, i.e.

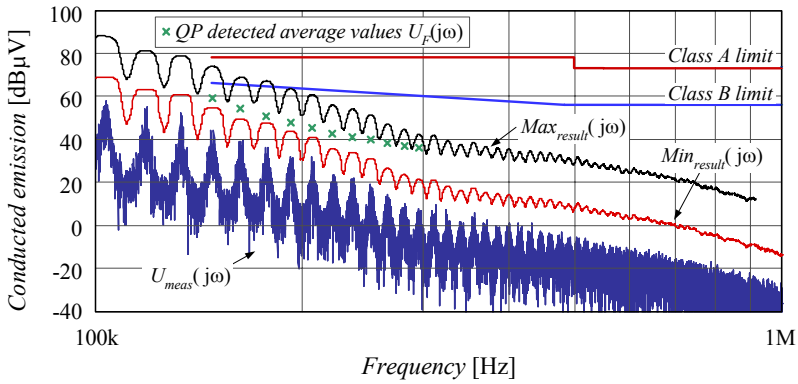


Fig.9: Simulation of the quasi-peak measurement (based on average values of voltage U_F(jω), cf. Fig.5) after inserting the designed input filter (cf. Fig.8) compared to the spectrum of the voltage U_{meas}(jω) at the LISN output terminals. Furthermore shown: Minimum (Min_{result}(jω)) and maximum (Max_{result}(jω)), signal levels resulting from QP detection, and conducted emission limits according to EN 55022, Class A and B.

$$E_L = \frac{LI_{\max}^2}{2} \rightarrow \min \quad Q_C = C \cdot U_{\max} \rightarrow \min \tag{7}$$

- Losses P_{R1d} in the damping resistor should be minimized for ensuring a high efficiency of the energy conversion.

Obviously, not all design requirements can be met simultaneously, so design priorities have to be defined in accordance to the application.

The characteristic values of the filter designed in this paper are compiled in TABLE II.

TABLE II – CHARACTERISTIC VALUES OF THE PROPOSED FILTER.

Characteristic	Value
Input current displacement angle for nominal load	-4.3°
Power factor cosφ for nominal load	0.997
Maximum capacitor charge of C_1	2.0 mC
Maximum inductor energy of L_1	4.4 mJ
Maximum fundamental reactive power of C_1	-165.8 VAr
Maximum fundamental reactive power of L_1	4.9 VAr
Maximum power losses of R_{1d}	300 mW

For certain applications it could be useful to insert additional filtering elements, e.g. an input inductor which defines the filter characteristic also for large tolerances of the inner mains impedance. In order to avoid a resonance with C_2 there another damping network has to be provided.

H. Test and Evaluation of the Design

The QP detected averaged values U_F(jω) resulting form the simulation model are depicted for selected frequency values in **Fig.9** (marked by "**x**"). It can be seen that the resulting emission values are well below the Class B limit. At f_{meas} *=150* kHz the selected margin of 6 dB margin can be observed.

Furthermore, Fig. 9 clearly shows that amplitudes of individual harmonics of the LISN output voltage are far below the value obtained with the QP weighting measurement (*15* dB at *150* kHz). This underlines the importance of a proper modeling for the measurement system, i.e. a filter design procedure relying only on a LISN modeling and considering only the amplitudes of individual harmonics would not be sufficient unless large design margins are provided.

As can also be seen from Fig. 9 the predicted quasi-peak values are always lying between a lower $Min_{result}(j\omega)$ and an upper limiting curve $Max_{result}(j\omega)$. The lower limit can be obtained as the square root of the sum of the squares of the RMS value of all harmonic components $U_{meas}(j\omega)$ located within the *RBW*

$$Min_{result}(j\omega) = 20 \cdot \log\left(\frac{1}{1\,\mu\text{V}} \cdot \sqrt{\sum_{f=\left(MB-\frac{RBW}{2}\right)}^{\left(MB+\frac{RBW}{2}\right)} \left(U_{meas}(j\omega)\right)^2} \right) \text{ [dB}\mu\text{V]} \tag{8}$$

The resulting signal $Min_{result}(j\omega)$ is the equivalent RMS value and can be seen as signal showing equal spectral power at the frequency ω as given for the original signal within the *RBW*.

Assuming no correlation of the individual harmonics a limiting maximum value

$$Max_{result} = 20 \cdot \log\left(\frac{1}{1\,\mu\text{V}} \cdot \sum_{f=\left(MB-\frac{RBW}{2}\right)}^{\left(MB+\frac{RBW}{2}\right)} U_{meas}(j\omega) \right) \text{ [dB}\mu\text{V]} \tag{9}$$

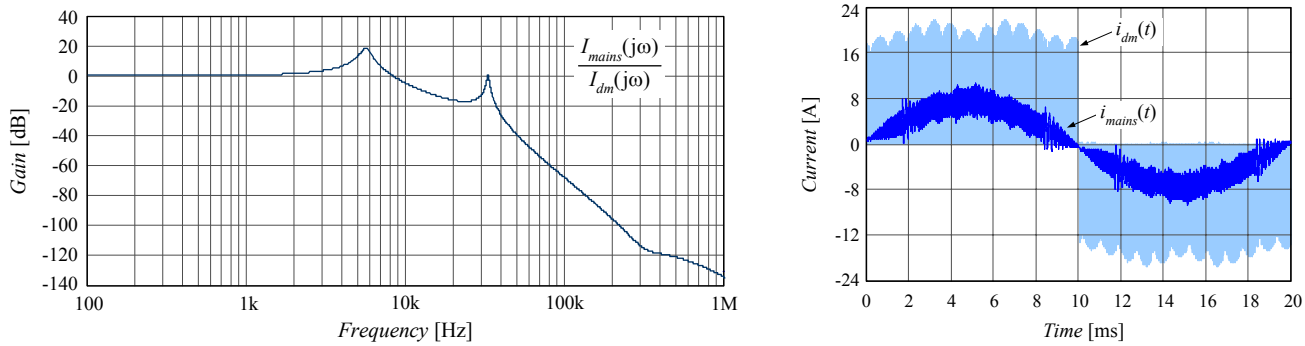
can be calculated by linearly adding the RMS values $U_{meas}(j\omega)$ of the spectral components within the RBW. $Max_{result}(j\omega)$ can be calculated with lower effort and can be taken for a simplified filter design, where the influence of the QP measurement is neglected. This, however will result in increased input filter volume.

The filter attenuation curve $I_{mains}(j\omega)/I_{dm}(j\omega)$ being present in case the VSMC is connected to the mains shows two main resonances (cf. **Fig.10**(a)). The resonant frequencies are defined by the filter parameters in connection with the inner mains impedance, which is assumed as L_{mains}*=50* µH in this case. It is also seen, that the parasitics of the filter elements are taking influence on the filter attenuation beyond 300 kHz.

Fig.10(b) shows that for employing the proposed input filter a sinusoidal shape of the mains current is obtained. As verified by the experimental analysis the mains current ripple in practice shows a lower value. This is due to ohmic components of the inner mains impedance and due to core losses of the inductive filter components.

III. EXPERIMENTAL VERIFICATION

In the following the experimental verification of the input filter design will be presented based on quasi-peak conducted emission measurements according to CISPR 22 and EN 61800-3 as described above.



(a) **(b)**

Fig.10: (a) Filter frequency response; **(b)** time behaviour of the converter input current $i_{mains}(t)$ with an inner mains impedance of L_{mains}=50 µH.

A. *Common / Differential Mode Noise Separator*

For conventional EMC compliance testing DM and CM mode emissions cannot be separated. Therefore, a novel three-phase DM/CM noise separator has been designed in order to allow an evaluation of the DM input filter design procedure. The basic schematic of the separator circuit is shown in **Fig.11** where noise components are represented by a common mode and differential mode noise voltage sources, u_{CM} and $u_{DM,a}$, $u_{DM,b}$, $u_{DM,c}$.

The noise separator comprises three transformers Tr_a, Tr_b, Tr_c with star-connected primaries and delta-connected secondaries. The primary star point is connected to the ground via a resistor $R/3$ while the secondaries are terminated by resistors R. Employing $R=50\ \Omega$ ensures an equivalent resistance of the noise separator inputs against ground of $50\ \Omega$ and allows to derive the CM and DM noise voltages directly (with unity gain) from the respective outputs. For measuring a differential mode noise voltage the corresponding output is connected to the input of the test receiver (50 Ω input impedance) after removing the explicit 50 Ω termination. Considering parasitic coupling capacitances of the transformers the measurement with reference to ground causes an asymmetry of the circuit which could result in a transformation of CM into DM noise. In order to achieve a high common mode rejection ratio (CMRR), therefore, common mode inductors L_a, L_b and L_c ensuring equal impedances of the transformer output terminals against ground for high frequencies are inserted into the differential mode outputs.

For applying the separator, a three-phase LISN must allow simultaneous access to all three phases. In case this is not possible, three individual single-phase LISNs could be employed. A photo of a first practical realization of the three-phase CM/DM noise separator is shown in **Fig.12**.

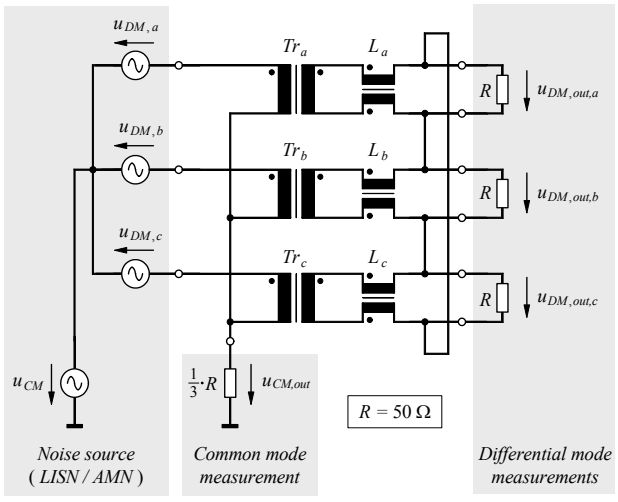


Fig.11: Circuit schematic of the three-phase CM/DM noise separator [13].

The detailed analysis of the proposed circuit a including a description of the operating principle, aspects of the practical realization and further variants of realization will be presented in a future publication in combination with a detailed experimental analysis.

B. *Measurement Results*

A verification of the input filter design described in the previous sections was carried out experimentally according to CISPR 22 using the setup shown in **Fig.13**. The measurement equipment used is listed in **TABLE III**. One has to note that parasitic circuit elements (like impedances of the cables connecting the EUT and the load, impedances of the connections to safety ground, etc.) which are not shown in Fig.13 could take significant influence on the measurement result by forming resonant circuits for common-mode current circulation and therefore have to be considered by proper arrangement of LISN, EUT, cables and load.

The specifications of the VSMC prototype are as follows:

Input (3-ϕ AC):

Input RMS line voltages (U_1)	**3 x 400 V +/- 20%**
Maximum input RMS phase current	$I_{1,max}$ = **18 A**
Mains frequency	f_1 = **50 Hz**
Current displacement angle	ϕ_1 = **0°**

Output (3-ϕ AC):

Output RMS line voltages (U_2)	**3 x 0 – 400 V**
Maximum output power	S_2 = **7.5 kVA (M = 1)**
Output frequency	f_2 = **0 – 200 Hz**
Current displacement angle	ϕ_2 = **0° – 90°**
Switching frequency:	f_p = **15 kHz**

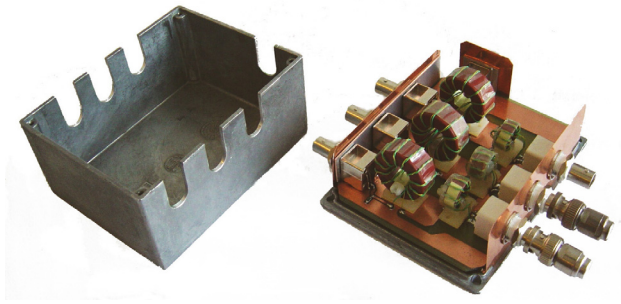


Fig.12: Three-phase CM/DM separator prototype photograph. Overall dimensions: 12.0x9.5x5.7 cm.

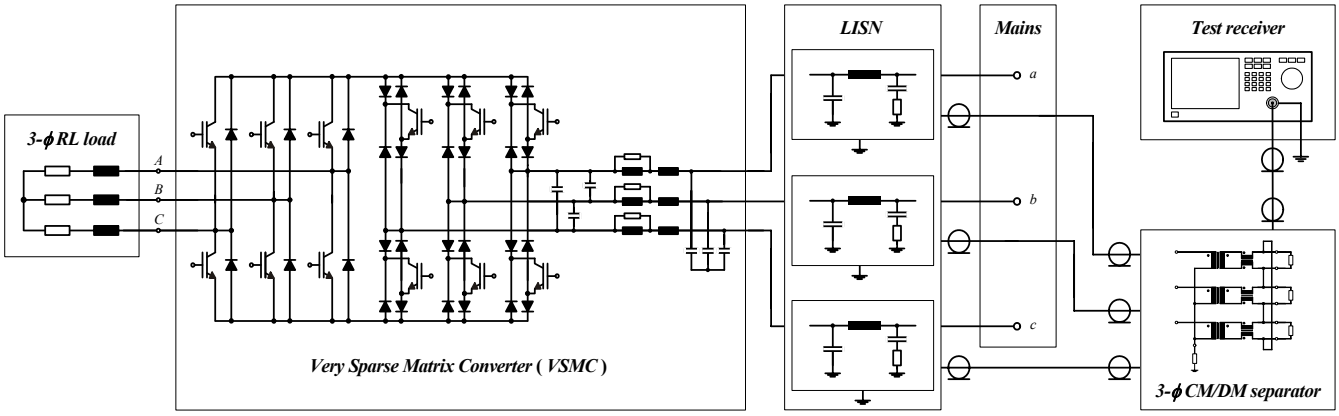


Fig.13: Conducted emission test setup employing the proposed three-phase CM/DM noise separator.

TABLE III – MEASUREMENT EQUIPMENT EMPLOYED IN THE TEST SETUP.

Qty.	Equipment	Specification
1	Test receiver	Rohde & Schwarz – ESPI 9 kHz … 3 GHz
2	LISN	Rohde & Schwarz – ESH3-Z5 Two-lines, V-network
1	LISN	Rohde & Schwarz – ESH2-Z5 Four-lines, V-network

Since no three-phase LISN with simultaneously accessible phase outputs was available for the tests the VSMC prototype supplying a three-phase RL star-connected load was fed via three individual LISNs (cf. **TABLE III**). An analog power amplifier with low inner impedance was used simulating the mains so that the conditions were close to the conditions assumed for simulating the system. The components employed in the input filter are listed in **TABLE IV**.

TABLE IV – INPUT FILTER COMPONENTS.

Qty.	Component	Specification
6	Capacitor	Evox-Rifa – PHE844 R, 1 μF / 440 V_{ac}
3	Capacitor	Evox-Rifa – PHE840 M, 470 nF / 275 V_{ac}
3	Inductor	Micrometals – T184-52, 41 turns / 2 mm^2
3	Inductor	Micrometals – T184-52, 12 turns / 2 mm^2
3	Resistor	0.82 Ω / 5 W

For analyzing the worst-case condition (cf. Section II.B) the modulation index was set to M = 0.5. The output frequency f_2 = 200 Hz was selected. The power consumption of the three-phase load ($R_{load} \cong 8.7\ \Omega$ in series with $L_{load} \cong 150\ \mu$H) was measured as 3.2 kW.

The level of the DM emissions taken from one DM output and recorded in quasi-peak detection mode is depicted in **Fig. 14**. The emission level is below the limit defined by CISPR 22 class B up to 5 MHz and the levels for 150 kHz are close to the predictions. The differences to the simulated DM noise characteristic (cf. Fig.9) are due to several reasons as listed in the following:

1. The CM/DM separator has a finite CM rejection ratio (CMRR) which changes with frequency and is around −40 dB@150 kHz. That means that in practice CM emissions (≈80 dBµV@150 kHz) are taking influencing on the DM measurement. Due to the decreasing CMRR this effect is pronounced at higher frequencies what explains the higher DM emission levels measured for frequencies >5MHz.
2. A resonance was present in the CM path at f≈850 kHz what can be seen in the increased DM levels at this frequency (again due to the limited CMRR).
3. Due to tolerances of the filter capacitances a lower filter attenuation than simulated was achieved; furthermore, the tolerances are causing an asymmetry of the filter which results in a transformation of CM into DM noise.
4. The output inductors used in the course of the test were smaller than for the simulations what leads to higher output current ripple and therefore higher input current switching frequency harmonics.

Taking all this into account the experimental result is in good correspondence with the simulations and/or verifies the proposed dimensioning procedure.

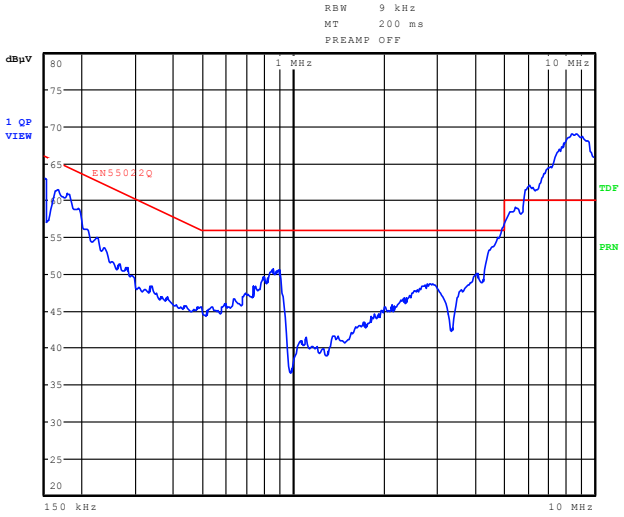


Fig.14: Measured conducted emission levels at a DM output of the three-phase CM/DM noise separator.

IV. CONCLUSIONS

In this paper a systematic procedure for the design of the DM input filter of a three-phase Very Sparse Matrix Converter (VSMC) is presented which can also be applied to other three-phase current-source-type converter topologies. The procedure is based on a detailed modeling of the RF measurement system with emphasis on the EMC test receiver. Following the design approach results in compliance to the considered harmonic standards (e.g. EN 61800-3) as verified by the experimental analysis of a VSMC prototype. There, the DM noise component was determined using a novel three-phase CM/DC noise separator. For calculating a first worst-case estimation of the EMC test receiver QP output the amplitudes of all harmonics of the LISN

LISN output voltage located in the RBW of the band-pass filter for a given MB frequency could be linearly added. This allows to omit the modeling of the QP detection and therefore considerably reduces the simulation/calculation effort, but results in a slightly over dimensioned filter circuit.

In the course of further research the CM/DM separator will be analyzed in detail in order to further increase the CMRR. Furthermore, the CM part of the VSMC input filter will be designed and finally both filter parts will be joined in a single optimum, i.e. minimum volume filter topology.

V. REFERENCES

[1] **Nave, M. J.**: *Power Line Filter Design for Switched-Mode Power Supplies*. New York (NY), USA: Van Nostrand Reinhold; 1991.

[2] **Williams, T.**: *EMC for Product Engineers*. Oxford, UK: Newnes; 2nd ed. 1996.

[3] **Kolar, J.W., Baumann, M., Shafmeister, F, and Ertl, H.**: *Novel Three-Phase AC-DC-AC Sparse Matrix Converter*. Proceedings of the 17th IEEE Applied Power Electronics Conference and Exposition, Dallas (Texas), USA, March 10-14, Vol. 1, pp. 777-791 (2002).

[4] **IEC International Special Committee on Radio Interference – C.I.S.P.R**. (1977): *C.I.S.P.R Specification for Radio Interference Measuring Apparatus and Measurement Methods – Publication 16*. Geneve, Switzerland: C.I.S.P.R.

[5] **IEC** (1996-06): IEC 1800-3 Adjustable Speed Electrical Drive Systems – Part 3: EMC Product Standard Including Specific Test Methods. Geneve, Switzerland: International Electrotechnical Commission Central Bureau.

[6] **IEC International Special Committee on Radio Interference – C.I.S.P.R.** (1993): Limits and Methods of Measurement of Radio Disturbance Characteristics of information Technology Equipment – Publication 22. Geneve, Switzerland: C.I.S.P.R.

[7] **Albach, M.**: *Conducted Interference Voltage of AC-DC Converters*. Proceedings of the 17th Annual IEEE Power Electronics Specialists Conference, Vancouver, Canada, pp. 203 - 212 (1986).

[8] **Silventoinen, P.**: *Electromagnetic Compatibility and EMC-Measurements in DC-Voltage Link Converters* [Dissertation]. Lappeenranta, Finland: Lappeenranta University of Technology; 2001.

[9] **Erickson, R.W.**: *Optimal Single Resistor Damping of Input Filters*. Proceedings of the 14th Annual Applied Power Electronics Conference and Exposition, Dallas (TX), USA, pp. 1073 - 1079 (1999).

[10] **Middlebrook, R. D.**: *Design Techniques for Preventing Input-Filter Oscillations in Switched-Mode Regulators*. Proceedings of PowerCon 5, the Fifth National Solid State Power Conversion Conference, San Francisco (CA), USA, pp. 153-168 (1978).

[11] **Middlebrook, R. D.**: *Input Filter Considerations in Design and Application of Switching Regulators*. Proceedings of the IEEE Industry Applications Society Annual Meeting, Chicago (IL) USA, pp. 366 - 382 (1976).

[12] **Phelps, T. K., and Tate, W. S.**: *Optimizing Passive Input Filter Design*, Proceedings of the Sixth National Solid-State Power Conversion Conference, (PowerCon 6), Miami Beach (FL), USA, pp. G1-1 - G1-10 (1979).

[13] **Kolar, J.W., and Ertl, H.:** *Vorrichtung zur Trennung der Funkstörspannungen dreiphasiger Stromrichtersysteme in eine Gleich- und eine Gegentaktkomponente* (in German). Swiss Patent Application, March 2004.

[14] **Nagel, A.**: *Leitungsgebundene Störungen in der Leistungselektronik: Entstehung, Ausbreitung und Filterung* [Dissertation]. Aachen, Germany: Rheinisch-Westfälischen Hochschule Aachen (2001).

[15] **Sokal, N. O.**: System Oscillations From Negative Input Resistance at Power Input Port of Switching-Mode Regulator, Amplifier, DC/DC Converter, or DC/AC Inverter. Proceedings of the 4th Annual IEEE Power Electronics Specialists Conference, Pasadena (CA), USA, pp. 138 - 140 (1973).

[16] **Guo, T., Chen, D.Y., and Lee, F.C.**: *Separation of the Common-Mode- and Differential-Mode-Conducted EMI Noise*. IEEE Transactions on Power Electronics, Vol. 11, No. 3, pp. 480 – 488 (1996).

[17] **Erich, S. Y., and Polivka, W. M.**: *Input Filter Design Criteria for Current-Programmed Regulators*. IEEE Transactions on Power Electronics, Vol. 7, No. 1, pp. 143 – 151 (1992).

[18] **Kohut, C. R.**: *Input Filter Design Criteria for Switching Regulators Using Current-Mode Control*. IEEE Transactions on Power Electronics, Vol. 7, No. 3, pp. 469 – 479 (1992).

[19] **Zargari, N. R., Joos, G., and Ziogas, P. D.**: *Input filter design for PWM current-source rectifiers*. Proceedings of the 8th Annual Applied Power Electronics Conference and Exposition, Seattle (WA), USA, pp. 824 - 830 (1993).

[20] **Tedder, R. M.**: *An alternate analysis of the current programmed model leads to simplified input filter design criteria*. Proceedings of the 7th Annual Applied Power Electronics Conference and Exposition, Boston (MA), USA, pp. 756 - 763 (1992).

[21] **Chandrasekaran, S., Borojevic, D., and Lindner, D.K.**: *Input filter interaction in three phase AC-DC converters*. Proceedings of the 30th Annual IEEE Power Electronics Specialists Conference, Vol. 2, Charleston (SC), USA, pp. 987 - 992 (1999).

[22] **DeMaw, M. F.**: *Ferromagnetic-core design and application handbook*. Englewood Cliffs (NJ), USA: Prentice Hall; 1981.