A simple, low cost gate drive method for practical use of SiC JFETs in SMPS

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Keywords

«Silicon Carbide», «JFET»

Abstract

The silicon carbide JFET has many promising advantages over silicon. However it requires a more complicated gate drive than conventional MOSFETs. In this paper a simple and effective method of driving the new devices with existing monolithic gate drive circuits is proposed. The basis of the proposed method lies in applying a constant negative DC bias to the gate in order to minimize the required voltage swing on the gate to enable switching to take place. The method is supported with experimental data and proves to be effective. The negative gate bias does however lead to additional losses and derating of the device is required. The derating data for a constant power loss is given as well.

Introduction

Much has been reported on the advantages of silicon carbide power devices [1][2]. These include high temperature operation, high voltage ratings and high switching frequencies. Currently one of the most promising silicon carbide turn off devices available is the JFET. This switch exhibits all the advantages of silicon carbide, but has the drawback that it is normally on and requires a relatively high negative gate voltage to turn it off. This problem has been overcome by the use of the so-called cascode configuration[3], where a low voltage silicon MOSFET is used to overcome these driving problem. The cascode configuration however has the conventional silicon device in close proximity to the silicon carbide device and as such the cascode configuration is limited to the same temperature constraints as conventional silicon. The application of the cascode configuration is well documented in [3] and will not be discussed in this paper.

It is therefore very desirable to be to drive the JFET directly, without the accompanying silicon MOSFET device. From a driving perspective the silicon carbide JFET can be considered similar to any other JFET. The equivalent circuit between the gate and source appears to be a diode junction orientated as shown in Fig. 1.

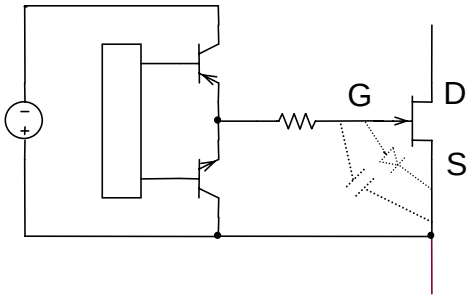

Fig. 1 Conventional approach to a JFET drive

This pn junction is normally never forward biased. With no bias on the pn junction, the main conduction channel is also normally unconstricted and exhibits a low resistance. In order to turn off the transistor, and close the channel by pinching it off, it is necessary to apply a negative bias to the pn junction between the gate and the source. For the different versions of the devices currently available, this pinch off voltage varies between -25V and -33V. A complication arises due to the fact that at a voltage approximately 8V lower than the pinch off voltage, the reverse biased pn junction will undergo breakdown and start to rapidly conduct current.

The reverse biased gate-source pn junction has a similar capacitive impedance characteristic as a conventional MOSFET. Turning the device on and off requires charging and discharging this capacitance typically from zero to a voltage below the pinch off voltage. This may be accomplished in a similar manner as for a conventional MOSFET and a typical drive circuit is shown conceptually in Fig 1. The only difference being a negative gate voltage with an amplitude somewhat larger than that of a conventional MOSFET. A problem that arises is that due to the relatively high voltages involved, it is not possible to make use of conventionally available driver circuits that are low cost and well proven. In general a discrete solution for the final gate drive stage is necessary [4][5]. This solution may be completely discrete in nature, or consist of a conventional driver circuit followed by a high voltage buffer.

Proposed gate drive method

This paper investigates the possibility of making use of some of the unique transfer characteristics of the JFET to ease the gate drive requirements. With no gate voltage applied, the drain-source channel exhibits a low conduction resistance. As a progressively larger negative gate voltage is applied, the channel starts to narrow until eventually blocking current totally. For a large portion of the range however the drain-source voltage is very low (the JFET is on) and therefore the internal electric field from drain to source is negligible. The channel remains in the linear region. This can be best illustrated in Fig. 2 where the on-state drain-source voltage of the JFET is plotted as a function of the negative bias on the gate.

As can be seen in the figure, at gate voltages below about 20V the on state voltage of the device varies linearly as a function of the negative gate bias. It can be seen that the transistor remains on with a low conduction voltage even for a considerable negative drive voltage. As the gate voltage approaches the pinch off voltage the resistance rises rapidly and the device turns off.

It is this property of the device that is to be utilized to aid in the simplification of the gate drive. It is possible to place a constant negative bias on the gate of the JFET and then to pulse the gate negative past the pinch off voltage to switch it. The excursion from the constant negative bias to a point past pinch off is not so large and can be accomplished with a conventional monolithic gate driver.

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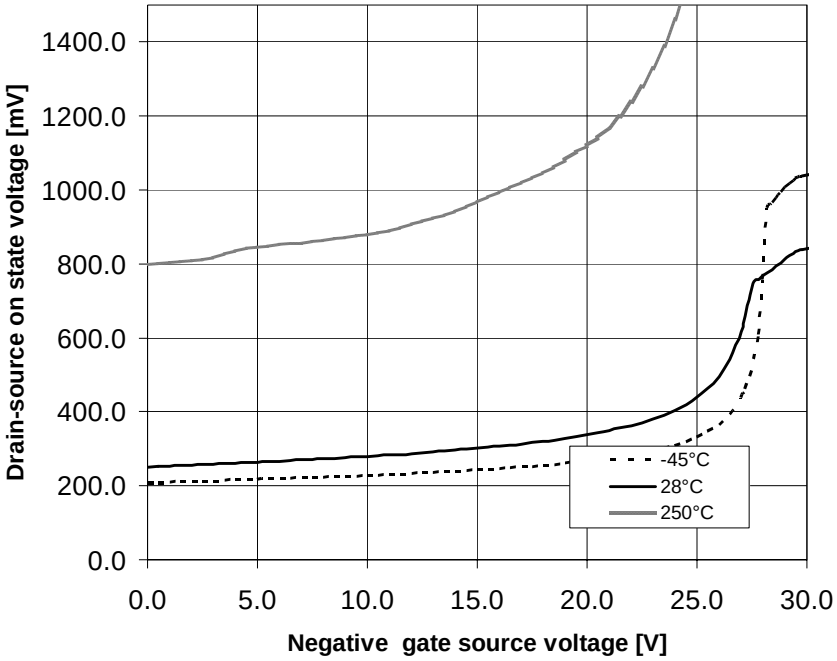

Fig 2. On state voltage when conducting a constant current of 4.8A.

This naturally leads immediately to the question of the effect of the constant gate bias on the conduction losses of the device. The on state voltage and therefore the conduction losses are increased by this driving method. However the device will switch faster and there are lower gate charge demands on the driver circuit. The reduction in performance of the JFET with this type of driving scheme needs to be controlled.

A derating factor can be defined that will keep the losses in the device constant at the same level that exists when there is zero bias. This derating factor is shown in figure 3 for constant negative dc bias voltages up to 15V. The derating factor is shown for both high and low temperatures and high and low currents. It remains relatively constant at all these extremes. Derating of approximately 1% per volt of negative dc bias is required.

Experimental Results

The operational experimental results were obtained by using a low parasitic test circuit realized as a chopper (see Fig. 4). It was realized using the HCNW3120 high-speed, high-voltage opto-coupler together with a 1 Ohm gate resistance. The Silicon Carbide devices used were 3rd generation JFET devices packaged in a Semitop package with 1200V blocking voltages and 5A current rating provided by SICED GmbH.

The test circuit was operated as normal at a nominal switching frequency of 200kHz. The switching waveforms of the circuit are shown in figure 5. The zero line of all three traces in the figure is the thick center line. The gate voltage is clearly being pulsed negative, however the more positive level of the gate signal is at approximately -9V.

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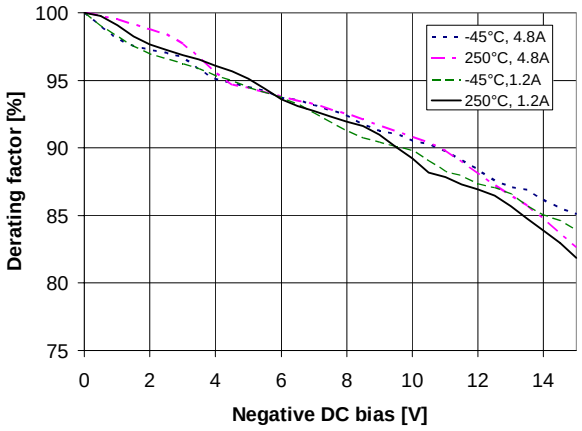

Fig. 3. Derating factor of the proposed driving scheme.

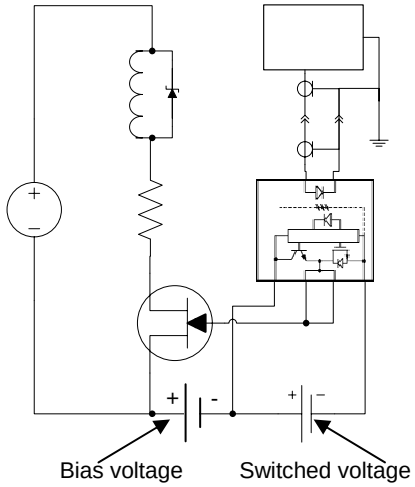

Fig. 4. Test circuit setup

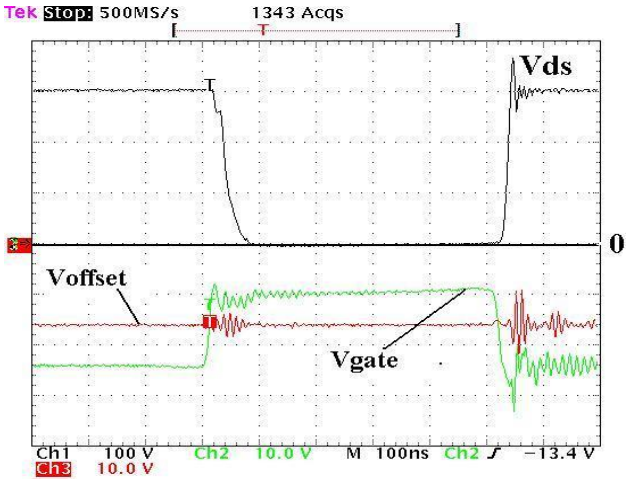

Fig. 5 The switching waveforms with offset voltage on the gate

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As can be seen from switching waveforms the -9V gate voltage offset remains constant whereas the only addition - 13V driving voltage is used to switch the device off. In this case any commercially available drivers can be used.

In order to further demonstrate the low additional losses that are introduced due to the constant negative bias, thermal images of open die devices were taken during switching conditions. These results are shown in Fig. 6. Clearly the device on the left with a conventional full voltage swing on the gate has a smaller hot spot. However the maximum temperature of the two devices appears to be very closely matched. The new proposed gate drive does however lead to a larger hot spot due to a small increase in losses.

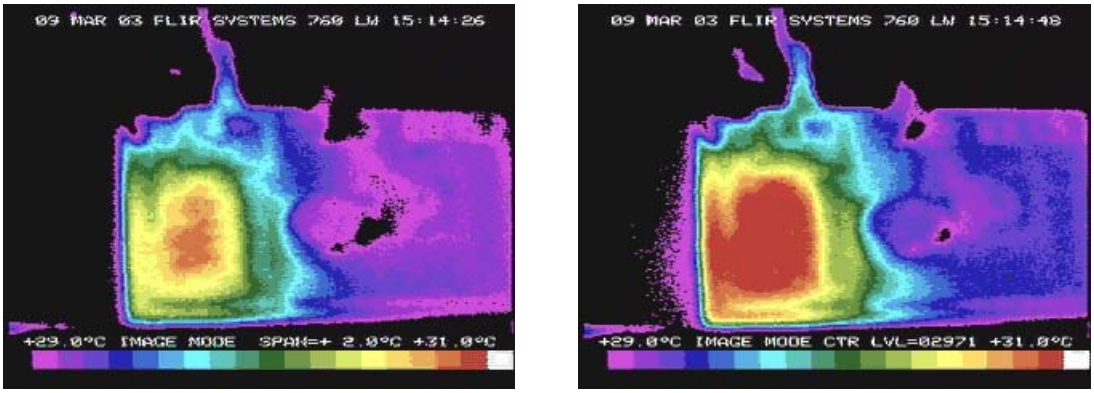

Fig 6. Thermal image of the JFET die under switching conditions a) conventional, b) with offset on gate.

Conclusions

The paper shows that it is possible to make use of conventional MOSFET / IGBT drivers to drive the new generation of silicon carbide turn off devices if attention is paid to the constant negative gate bias. The trade off that needs to be made for the simple drive circuit is that the total conduction losses are increased due to a narrower channel. Whether or not this is acceptable will depend on the actual application concerned.

The devices should be derated by approximately 1% per volt of negative gate bias applied. Alternatively the devices will exhibit larger conduction losses which will lead to higher operation temperatures. Given the inherent high temperature characteristics of silicon carbide this may be acceptable. However in order to achieve optimal operation a gate drive circuit that exhibits the full voltage swing as required by the gate will be required.

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