Enhanced Control Scheme for Three-Phase / Three-Level Rectifiers at Partial Load

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Abstract--**A prominent boost-type three-level topology, which proved to represent a cost effective and highly efficient solution for switched mode rectifiers is inspected towards its operation at discontinuous conduction mode (DCM). This mode of operation occurs not only at high input voltage in conjunction with low load currents but even at medium loading in the vicinity of mains voltage zero crossings. And since the requirements on THD conflict with the actual behavior of the circuit when operated at DCM measures are needed for optimization. A detailed analysis of DCM and associated states is performed. Basic rules for the location of error voltages can be found. This leads to a novel measure to optimize the modulation and control scheme respectively, facilitating designs without additional inductance. Selected simulation and measurement results prove the enhanced modulation scheme.**

I. Introduction

Three-phase high power factor switched mode rectifiers (PFC-SMR) are undergoing rapid development in recent years due to tough regulations, such as IEC 1000-3-2/4, hard economic constraints and a large potential market. Telecommunication devices, electrical drives, welding power supplies and many types of industrial electronic equipment need a high amount of electrical power supplied by PFC-SMR. In [1] and [2] the well-known three-phase / three-level boost-type switched mode rectifier (Vienna Rectifier, Fig. 1) is introduced, characterized by a lower blocking voltage of semiconductor devices and reduced size of boost inductors. Since only half of the voltage as compared to the common boost topology is effective, the switching frequency can be increased yielding a better current-shaping with a lower THD. This is facilitated by the applicability of 500 V to 600 V Semiconductors, that are common in all single phase applications though the 3-level SMR is supplied from 530 $V_{rms,L-L}$ maximum mains voltage.

The circuit presented was implemented as a utility interface in a 10 kW isolated power supply for telecommunication systems, because this state-of the art topology turned out to combine high power density due to high switching frequency with high flexibility, due to an operation in a wide voltage range and at single-phase conditions [7]. In this paper problems of DCM are explored in conjunction with this topology. At first the control and modulation concept at continuous conduction mode (CCM) is described briefly in chapter II. A detailed analysis of relevant switching states is described in III. In IV. a new control solution is presented, that solves and omit the penalty in terms of cost and size in comparison to the solutions given in [7]. This now approach is verified by selected measurement and simulation results.

*) This work was conducted during our common time at University of Paderborn.

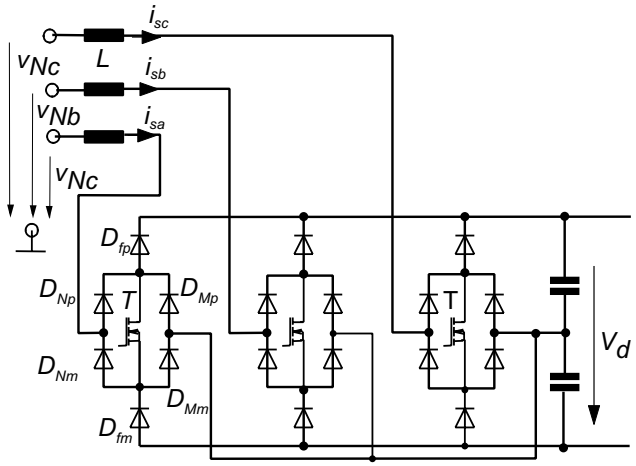

Fig. 1. Three-level rectifier presented in [1] (Vienna Rectifier).

II. Description of Problem

A. Control and Modulation at CCM

Contrary to single-phase systems the control of the SMR in Fig. 1 is more complex. Different control concepts have were in [2], [1], [6]. Operating rectifiers in universal applications leads to the demand to cope with a wide input voltage range [7] and load ranges (0 - 100%). Not only at high input voltage levels and low load DCM cannot be avoided, but even at medium load levels DCM can be found in the vicinity of mains voltage zero-crossings. This nonlinear behavior causes distortion in the current control loops, which are - contrasting to single-phase systems - more complex to investigate due to couplings and interactions between the three phases on the one hand and current control loops on the other hand.

The switching vectors according to the three-level rectifier in Continuous Conduction Mode (CCM) are shown in Fig. 2, with 19 distinct voltage vectors representing 25 switching states. Contrary to three-level inverters at one single switching cycle only 8 space-vectors are applicable,

that are determines by the signs of the three input currents (see Fig. 2). Typically the phase-shift φ_N between mains voltage $\boldsymbol{v_N}$ and rectifier input voltage $\boldsymbol{v_s}$ is small ($\varphi_N < 2°$), due to a small inductance values L and high switching frequencies respectively. For the context, discussed in this paper $\varphi_N \approx 0$ is assumed. Here $m_s = \hat{v}_s / V_d$ is the (controlled) modulation index of the rectifier while the ratio of mains voltage to output voltage is defined similarly as $m_N = \hat{v}_N / V_d$. V_d is the DC-link voltage while $\varphi = \omega t$ is selected as a variable to represent the angle within a line cycle.

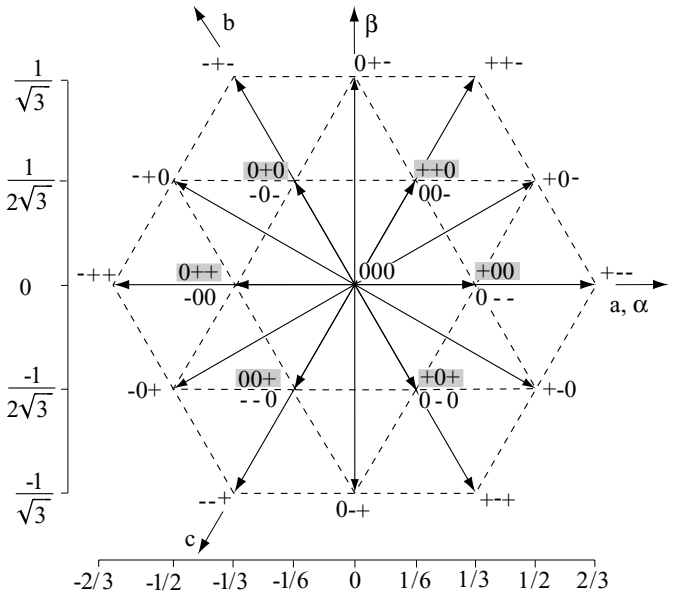

Fig. 2. Space vector representation of all possible switching states without DCM

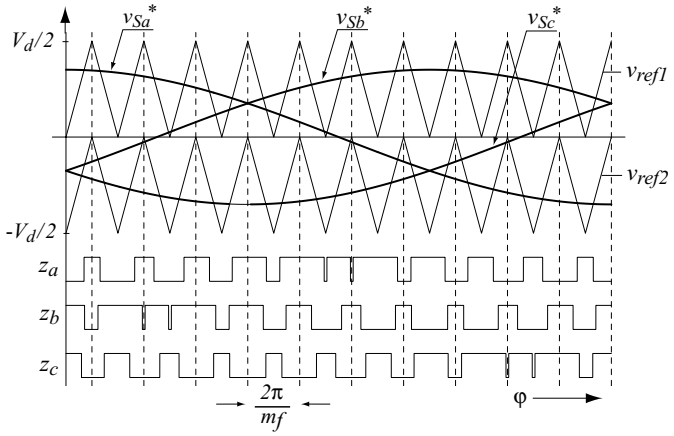

Fig. 3: Modulation scheme based on Double-Ramp Comparison Technique

This limitation of phase shift φ_N is bound directly to the basic difference between three-level rectifiers and three-level inverters: not all space-vectors can be applied actively, as the input currents needs to be considered. Nevertheless, at nominal operating conditions and $\varphi_N \approx 0$ the behavior is similar to three-level inverters.

Hence, similar modulation algorithms can be applied. But the dependence on the high frequency waveforms of the input currents causes problems not only at low input currents, but also in the vicinity of zero-crossings. Zero-crossings of the currents have to be detected carefully in order to select the right hexagon and switching states, respectively. '+', '0' and '-' in Fig. 2 represent the possible input terminal voltages ($+V_d/2$, 0 and $-V_d/2$) of the rectifier depicted in Fig. 1, if the output voltage centerpoint is the reference. Note, '0' represents the positive gating signal of respective transistor, connecting the inductor to the centerpoint and allows inductor-currents independent of sign and direction. Because all other switching states are selected passively, the inductor currents might become discontinuous in case the free-wheeling diodes are blocking while the associated transistor is in off-state. This leads to additional switching stages, where one or all phase currents are zero.

III. Analysis of DCM

A. Additional Switching states

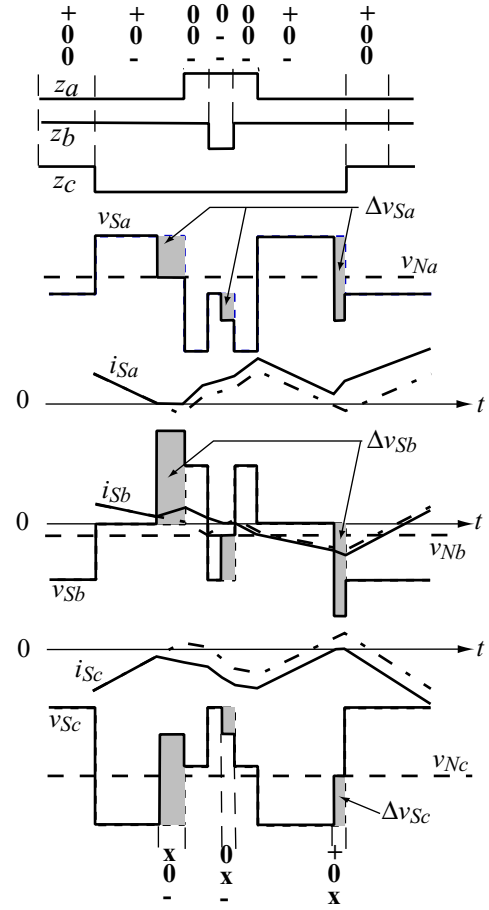

Fig. 4. Voltages and inductor currents during DCM

In Fig. 4 inductor currents and associated voltages at DCM are shown as an example. At state (+0-) the current in phase a becomes discontinuous at first, which means current i_{sa} remains zero until the associated switch is

turned on and state (00-) is activated respectively. As an example the associated switching cycle is shown in Fig. 5.

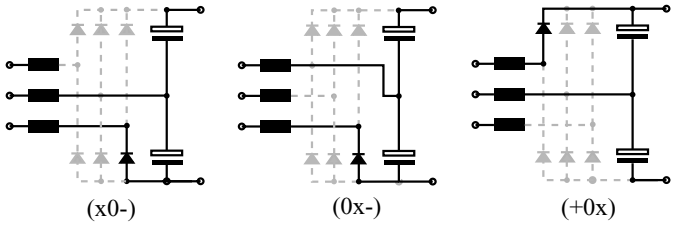

Fig. 5: Three Examples for Switching States during DCM: for phase a (x0-), for phase b (0x-) and for phase c (+0x)

In Table 1 all switching states for the entire operation range and line period are depicted, including the additional states resulting from DCM. The supplementary state 'x' is introduced, representing no current flow in the related phase. Thus all respective semiconductors of this phase are non-conductive.

No.	DCM	1-ph DCM	3-ph DCM
1	000		
2	+00	x00	
3	-00		
4	0+0	0x0	
5	0-0		
6	00+	00x	
7	00-		
8	+00	x+0	
9	+-0	+x0	xx0
10	--0	x-0	
11	-+0	-x0	
12	0++	0+x	
13	0-+	0x+	0xx
14	0--	0-x	
15	0+-	0x-	
16	+0+	+0x	
17	-0+	x0+	x0x
18	-0-	-0x	
19	+0-	x0-	
20	+--	+-x	
21	++-	+x-	
22	-+-	x+-	xxx
23	-++	-+x	
24	--+	-x+	
25	+-+	x-+	
Sum	**25**	**21**	**4**

Table 1: Possible Switching States at CCM and DCM

In total 25 additional switching states can be found, thus the total number of possible switching states is 50. Here DCM in a single phase and DCM in all three phases is distinguished. Single-phase-DCM means exactly one out of the three inductor currents is zero, while in case of three-phase-DCM all three currents are zero. Under consideration of the fourth state 'x' theoretically $4^3 = 64$ switching states can be found totally, but practically impossible states remain unconsidered. For example state (x--) is impossible, because two inductor currents cannot be negative while the third current is zero.

B. Location of space vectors at DCM

During DCM the voltage across the inductor of the associated phase is zero, that means the voltages of the inverter side is equal to the line voltage ($v_{sx} = v_{Nx}$) of the associated phase. That means, the phase voltage v_{sx} is no longer determined by the pulse pattern, but by the exact current waveforms and by the line voltage. Thus, the space vector is no longer at the expected fixed location.

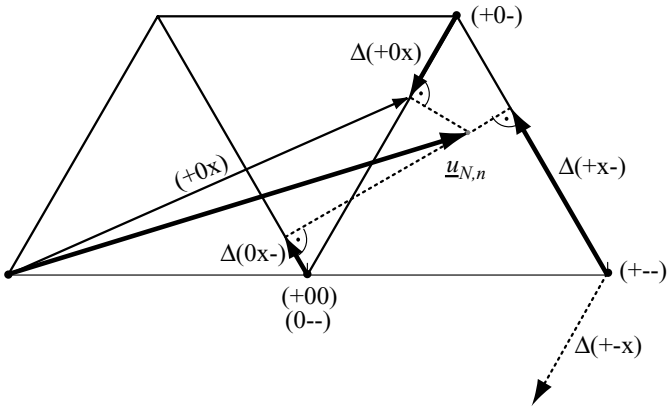

Fig. 6: Location of space vectors at DCM-states

Under consideration of the complex vector $\underline{a} = e^{j2\pi/3}$ the new space vector can be described by eq. 1. That means, the vector of the error voltage, has always the same direction as the associated phase quantity. For example state (+0-) turns into (+0x) if the current in phase *c* becomes zero. Than the resulting error voltages $\Delta v_{s,c}$ has the same direction as the voltage for phase *c*.

$$\begin{aligned} v_{s,c} &= \tfrac{2}{3}(a^0(\tfrac{1}{2}) + a^1(0) + a^2(-\tfrac{1}{2} + \Delta v_{sc,n})) \\ &= v_{s,c}\big|_{(+0-)} + \Delta v_{s,c} \end{aligned} \qquad (1)$$

A detailed analysis of the behavior at DCM leads to a set of rules. The occurrence of switching states is bound to special zones in the hexagon, depending on the current level, modulation index and angle within the line period.

C. Calculation of Switching states and Error voltages

Contrary to single-phase boost-type rectifiers, the behavior at DCM in case of three-phase circuits is much more complex. For single-phase rectifiers three states have to be distinguished, 'on', 'off' and no-current flow at DCM. As a result of DCM disturbances in the current control loop cannot be avoided, as long as it is designed for CCM. Due to the settings of minimum load power, the boundary between CCM and DCM should be known.

A representative interval of the line period ($0 < \varphi < 30°$) was analyzed in detail. Due to symmetries within the three-phase systems, the results can be generalized for the entire

line cycle. This was conducted in an iterative manner by implementing rules in Math-software package MATHEMATICA. These assumptions were considered for the calculations:

- Line voltage remains constant during a single switching cycle.
- Inductors are pure inductive, parasitic resistors are neglected. Thus inductor currents are piece-wise linear.
- The behavior of semiconductors is ideal, that means neglecting of on-state losses and switching transients.
- The calculations were conducted by using per unit quantities to come to more general results on one hand and simplification of the calculations on the other hand. Voltages are related to the DC-link voltage V_d currents to the base $I_B = V_d \cdot T_s / L$.
  $v_{Nx,n} = v_{Nx}/V_d \qquad v_{Sx,n} = v_{Sx}/V_d$
  $i_{Sx,n} = i_{sx}/I_B$ with $x \in \{a,b,c\}$
  Thus the connected quantities power and line-side conductivity g_N can be found by
  $p_n = P/V_d I_B$
  $g_{N,n} = g_N \cdot V_d / I_B$
- The pulse pattern and duty cycles respectively are calculated based on the assumption that the average rectifier voltages per switching cycle are equal to the line voltage ($v_{Sx} = v_{Nx}$).
- Additionally the exact high frequency current waveform depends also on the zero-quantity. Similar to 2-level inverters, for each switching cycle of 3-level rectifiers a pair to switching states can be found, leading to the same space-vector. The ration between these equivalent states can be given by $\rho = d_+/d_0$, where d_0 represents the on-time of both states while d_+ represents the on-time of the states associated to the upper capacitor. These states are grey shaded in Fig. 2. For this analysis a ratio ρ is selected, that leads to optimal balanced DC-link voltages.

As an example, Fig. 6 shows the result for one switching cycle. The black bar on the bottom of the plots, represent the areas, where the associated switch is turned on. Similar to single phase circuits, during the on-time of the transistor DCM cannot occur. The duty cycles are selected in a way, that at CCM the inductor currents at the end of each cycle are equal to the levels at the beginning. Fig. 6 shows, that this is no longer true in case of DCM, if the duty cycles remain unchanged. Here the currents at the end are absolutely higher. This means, the error voltages due to DCM have always the opposite sign of the currents.

The average quantities of these error voltages are depicted in Fig. 7 and Fig. 8 depending on different per unit power levels and angels $\varphi = \omega t$ of the line period. At medium power levels, DCM occurs in the vicinity of zero crossings and leads to error voltages in the other phases, even if the associated currents are in CCM. At lower power

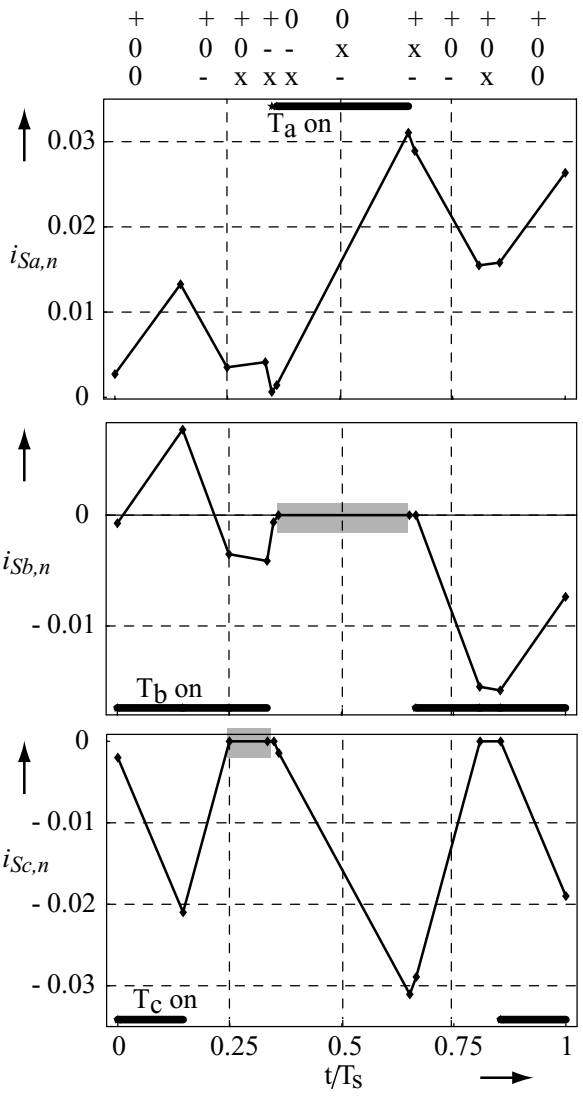

Fig. 6. Calculated Current Waveforms (m_N = 0.42, phi =15°, p_n= 0.17%).

levels error voltages with opposite sign of the phase currents can be found.

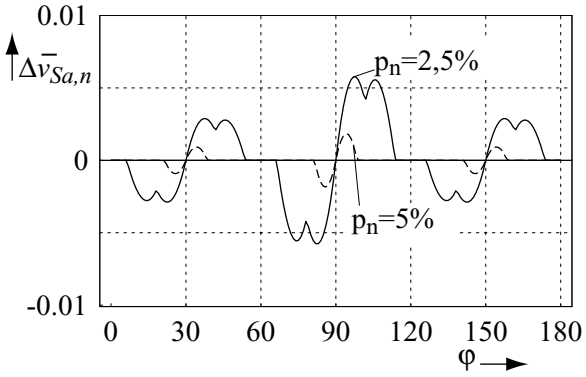

Fig. 7: Error voltages for one half-cycle (m_N = 0.44) at variable power levels

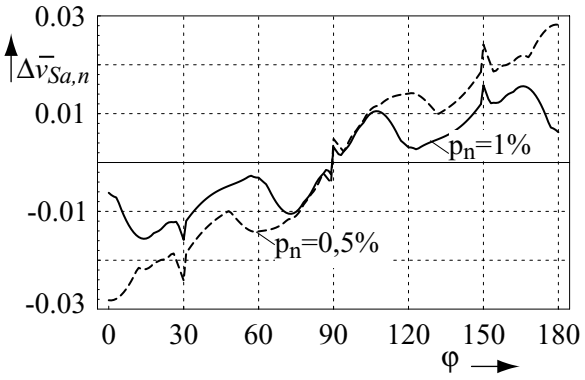

Fig. 8: Error voltages for one half-cycle (m_N = 0.44) at variable power levels

D. Boundaries between DCM and CCM

In Fig. 9 the boundary between DCM and CCM for different zero quantities ρ is depicted. ρ_E represents the zero-quantity, that leads to optimal balanced output voltages, while $\rho = 1$ means, that only one of the equivalent switching states associated with the zero quantity is selected. This is another important result: DCM depends also on the zero quantity. Under consideration of the per-unit ratio, it can be found, that DCM occurs at high modulation index at any power level at least for narrow intervals near the zero-crossings.

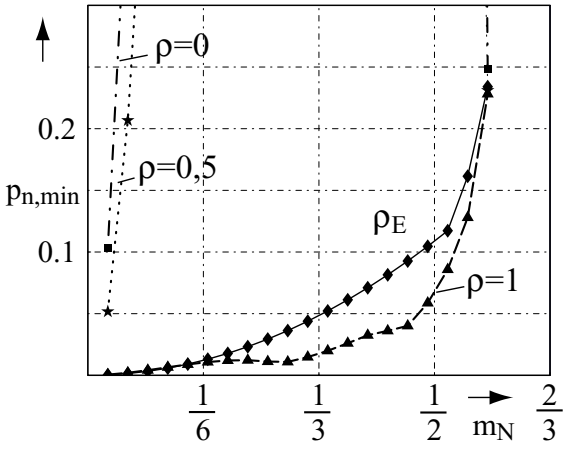

Fig. 9: Minimum Power without DCM for the entire line cycle depending on different zero quantities

IV. Control Concept

Typically the current control section in high power PFC circuits is designed for CCM by average current mode control independent of the modulation scheme. The rectifiers locally averaged voltages v_{sx} (based on one switching cycle) and the scaled command voltages v_{sx}^* respectively for the modulation scheme are very close to the mains voltage ($v_{sx} \approx v_{Nx}$), independent of the current or power level during CCM. Thus, in CCM pulse pattern can be easily determined by the assumption, that the average rectifier voltage v_{sx} has to be equal to the instantaneous mains phase voltage v_{Nx}. But due to the error voltages according to DCM, the determination of the pulse pattern is more complex. These error voltages cause disturbances of the current waveforms. Usually in the 3-phase systems only two current amplifiers are applied due to the coupling of the three input currents. But in case of DCM the linear relationships are lost, leading to asymmetric command voltages and disturbances. These effects are known also for 2-level inverters [4].

One important reason for the complex relationship between command voltages and pulse-pattern is the dependency on the instantaneous inductor currents i_{Sx}. Theoretically it should be possible to calculate pulse patter under consideration of the additionally switching states at DCM in a way that the current waveforms have sinusoidal shapes. But practically this leads to very high effort for implementation of the complex control and modulation algorithm on the one hand and for additional high bandwidth current sensing on the other hand. Additionally at low loads offset currents of current transducers may cause severe errors. Thus it seems to be impossible to implement a modulation scheme, that considers DCM related effects in detail.

Different solutions to avoid disturbances due to DCM were discussed in [8] following the concept to reduce the boundary between DCM and CCM to acceptable levels. The minimum power level depend on the product of inductance times switching frequency $L_1 f_S$. Hence, these concepts are based on the one hand on an increase of switching frequency and on the other hand on higher inductance at low current by nonlinear inductors. These measures reduce the boundary between DCM and CCM to lower power levels, but do not solve the root cause. Fortunately, modern core materials like molypermalloy powder cores or iron powder cores show these nonlinear characteristics, hence they seem to be suitable for these applications on the one hand. On the other hand at high power levels and high current levels respectively the inductors will become more bulky and expensive than solutions applying standard ferrite cores. A series or combined arrangement of a saturable inductor and an inductor designed for rated operation may also be a reasonable solution.

A. Adaptive Compensation Method

Different solutions have been investigated to achieve stable and reliable operation even at low load. Typically the power part is designed and optimized for a certain power level, thus the measures should basically affect the control section, especially since it is more cost-efficient.

The structure of the modified current control is shown in Fig. 9. In principle, the state variable (i_{Sx}) is rebuild by a reference model without any disturbance (i_{Sx}^R) and compared to the actual state variable (i_{Sx}). This difference is fed to a compensator and the output of this error amplifier is added to the output of the original error amplifier. The original error amplifier is a simple proportional unit, where

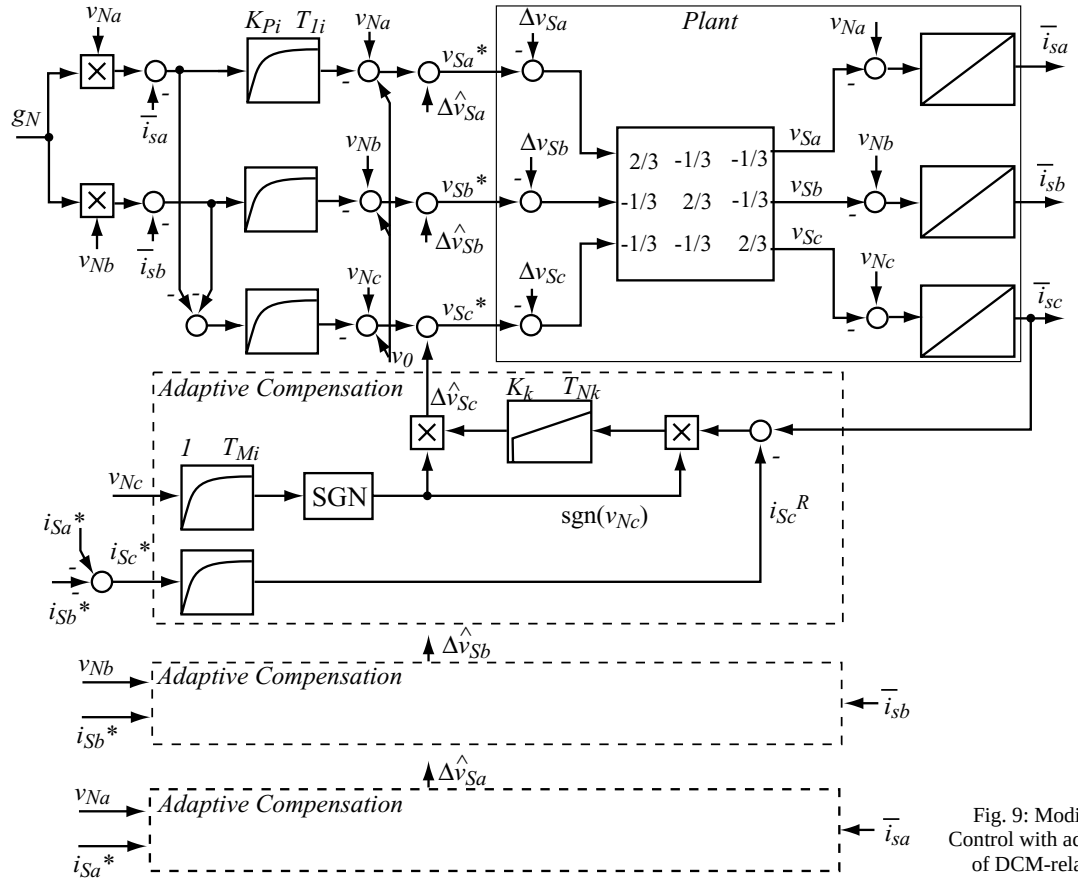

Fig. 9: Modified Current Mode Control with adaptive Compensation of DCM-related Error Voltages

the mains voltages are added in a feed-forward manner. The compensation is implemented by a proportional integration, where input and output have controllable inversions. This inversion is controlled by the sign of the inductor currents. For practical implementation it is more easy to select the sign of the line voltage v_{Nx} that is equal to the sign of the references signal of the associated inductor current instead of the inductor current i_{Sx} itself, because the sign of the inductor current is difficult to determine precisely especially in the vicinity of zero-crossings. But exactly there it is of great interest. The multiplier at input and output of the compensator switch between in version and non-inversion depending on this sign. This function can be implemented much more easy by switch between positive and negative gain, thus this function is called controlled inversion. The small signal behavior of this adaptive compensation is equal to a proportional integration. Thus the determination of the compensator settings K_k and T_{Nk} can start from the settings of the current error amplifier at CCM.

B. Simulation Results

Elaborated concept was verified by simulation. Different parameters for the compensation were investigated. The proportional gain K_K is reduced to 2% of the original gain for an error-amplifier in CCM, but the time constant T_{NK} is also reduced to 1/3. In Fig. 11 the simulation result during a load step from 5000 W to 100 W is shown. The deviation of the DC-link voltage v_d is very low, while the inductor current become mean-while very low.

C. Measurement Results

This structure is suitable for analogue implementation due to its simplicity. Applying this principle of operation, basically three items have to be considered:

- The offsets at current sensing should be low or compensated to avoid disturbances at low currents.

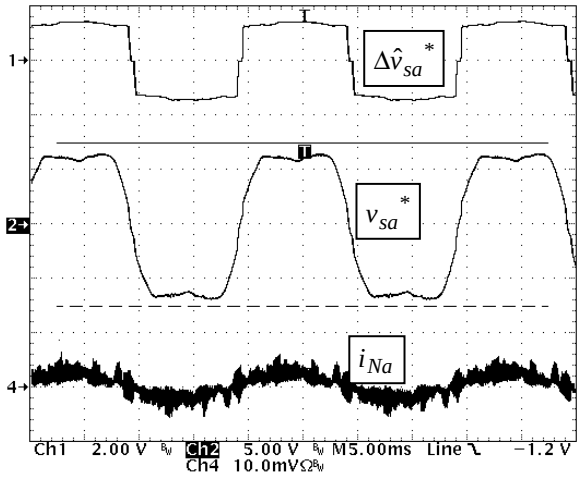

Fig. 10: Measurement Results at 150W

- The detection of signs for the controllable inversion should be done carefully.
- A dead time at switching the controllable inversion should be considered. That means, the switch acts as a three-state switch (positive gain of error signal, negative gain of error signal and zero). During this dead-time, that is selected to be as long as 3 switching cycles at switch over between the positive and negative gain the output of the compensator is zero.

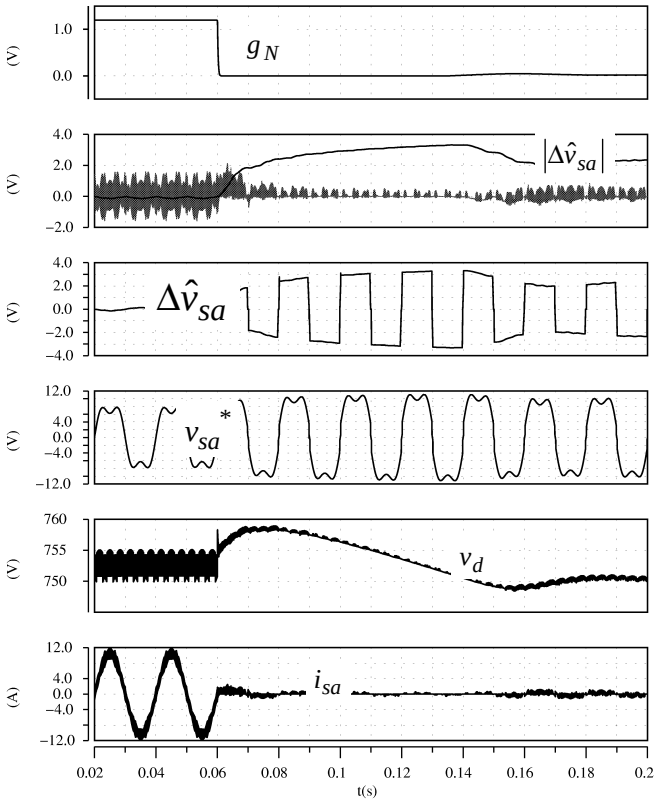

Fig. 11: Load Step from 5000W to 100W with adaptive Compensation (Simulation Result)

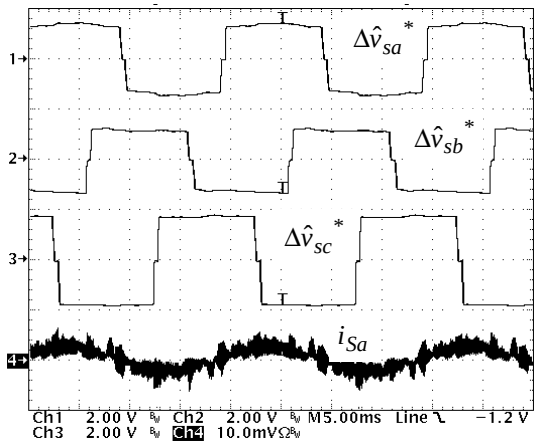

Fig. 12: Measurement Result at 50W (pn=0.26%)

The reduction of these parasitic influences effects the result of adaptive compensation more than the optimization of the parameters of the error amplifier. In Fig. 10 and Fig. 12 measurement results are shown, that prove the principle of operation. Even at 15 W, this concept leads to stable operation of the 10 kW rectifier, which means, that under consideration of housekeeping power, the circuit is now capable to handle no-power operation at continuos operation. Without this measure the circuit was switched on and off according to overvoltage conditions or certain levels of the voltage error amplifier output.

V. Conclusion

This paper describes the behavior of three-level rectifiers at low load. Discontinuous Conduction Mode in one or all phases can be found at low load and in the vicinity of zero-crossings. 25 additional switching states can occur at low load, most of them depend on the input voltage level and phase angle. Minimum power characteristics for the boundary between CCM and DCM are presented together with an adaptive control scheme, verified by simulation and measurement results. This enhanced current control scheme allows a wide operation range of the three-level / three-switch topology from nearly zero to full load, without disturbances in input current and DC-link voltage.

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