Comparison of the Chip Area Usage of 2-level and 3-level Voltage Source Converter Topologies

Mario Schweizer*, Ignacio Lizama†, Thomas Friedli* and Johann W. Kolar*
*Power Electronic Systems Laboratory
ETH Zurich, Physikstrasse 3, 8092 Zurich, Switzerland
Email: schweizer@lem.ee.ethz.ch
†Universidad Tecnica Federico Santa Maria
Email: special.edition@gmail.com

***Abstract*—In the low voltage converter range, 3-phase 3-level VSC topologies are not wide spread in industry because of the increased part count and higher costs, although they are more efficient for higher switching frequencies. In this paper an alternative 3-level topology referred to as T-type is presented, which is very high efficient for medium switching frequencies (4 - 20 kHz). Additionally, it is shown that the total silicon chip area of a 3-level topology can be lower than in a 2-level topology since the losses are distributed over more components leading to only a small increase in the junction temperature. This allows for the design of a chip area and cost optimized 3-level bridge leg module for the mass market.**

I. Introduction

In recent time, efficient energy conversion in the low voltage range has gained more and more attention. Applications such as photovoltaic grid inverters, rectifiers, and automotive motor inverter systems demand for an outstanding efficiency at low costs and weight. In order to have small passive components and a light weight system the switching frequency has to be increased to medium values of $10 - 25\,\mathrm{kHz}$, which leads to higher switching losses and lower system efficiency.

Previous work showed that multilevel converter structures have a very flat dependency of the converter losses on the switching frequency. If a standard 2-level VSC built with $1200\,\mathrm{V}$ IGBTs is compared to a 3-level NPC VSC built with $600\,\mathrm{V}$ devices, the efficiency of the 3-level converter can be better if the switching frequency is higher than $10\,\mathrm{kHz}$ [1].

The 3-level NPC topology is most often used as a drive inverter with direct torque control in the medium voltage range [2]. What prevented the 3-level NPC VSC of being successful in the low voltage market are increased costs and complexity. With 6 diodes and 4 IGBTs per bridge leg, also the necessary gate drive units double. The semiconductor chips assembled in a 3-level NPC bridge leg module are dimensioned and rated mostly in the same manner as for a 2-level VSC, neglecting the loss distribution over the specific elements which can be very uneven depending on the modulation strategy. This results in an oversized module with expensive and weakly utilized semiconductor area.

In this paper the 3-phase 3-level T-type topology [3]–[6] is proposed as an alternative to the 2-level VSC for a medium switching frequency range. Compared to the 3-level NPC topology, the T-type obtains an active bidirectional switch to the dc-link voltage mid-point and gets along with 2 diodes less per bridge leg. The topology is described in [7] for a single phase photovoltaic inverter and is patented by Conergy [8]. It is an alternative to several active clamped 3-level topologies presented in [9] which are more complex, and it can be extended to a multilevel topology [10]. In section II the 3-phase T-type topology is presented. A loss analysis with switching loss measurements on a test setup follows in section III. In section IV the loss calculation is extended to a variable chip area. This allows for a fair comparison of the 2-level

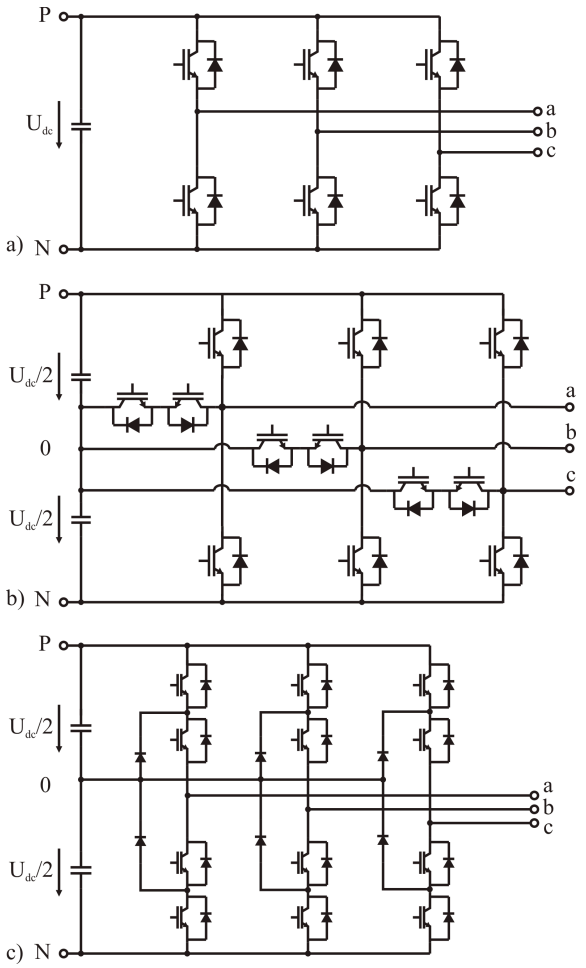

Fig. 1. Topologies of the a) 2-level, b) 3-level T-type and c) 3-level NPC voltage source converters.

VSC, the 3-level NPC, and the T-type converter. It will be shown that the losses in both 3-level topologies are decreased and distribute over many chip dies. This leads only to a small increase in the junction temperature and allows for choosing smaller semiconductor chip sizes. Surprisingly, the total chip area necessary for the 3-level NPC and the T-type converter is smaller than for the 2-level VSC already for switching frequencies above 10 kHz.

II. The T-Type Topology

The basic topology of the 3-phase 3-level T-type VSC is depicted in Fig. 1. The conventional low voltage 2-level VSC topology with 1200 V IGBTs and antiparallel diodes is extended with an active, bidirectional switch to the DC-link mid-point.

The bidirectional switch can be realized with several combinations of switch technology. Since it has to block only half of the DC-link voltage ($U_{dc} = 700\,\mathrm{V}$), it is possible to use switches with half of the blocking voltage. In this paper two possible implementations are investigated. First, a common emitter series connection of two 600 V IGBTs including antiparallel diodes is considered. This configuration has the advantage that just one additional isolated gate drive voltage has to be provided. The 600 V IGBTs are cheap and have a very good switching performance with a low forward voltage drop.

As an alternative two 600 V CoolMOS in a common source configuration are tested. The idea was to profit from the outstanding switching performance of the CoolMOS.

A. Commutation

The switch commutation has to be considered in detail for the T-type structure. Basically, the output of a bridge leg can be connected to the positive (P), neutral (0) or the negative (N) dc-link voltage level as can be seen in Fig. 2. The positive voltage level, for instance, could be achieved by closing T_1, the neutral level by closing T_2 and T_3, and the negative level by closing T_4 for both current directions. However, this strategy would require a current dependent commutation sequence. Fortunately, there is a simpler commutation strategy which works independently of the current direction.

If we close not only T_1, but T_1 and T_2 for the positive voltage level, T_2 and T_3 for the neutral, and T_3 and T_4 for the negative voltage level, the current commutates naturally to the correct branch independent of the current direction. A simple turn-on delay prevents from shoot-through equivalent to the 3-level NPC topology commutation.

As an example we consider Fig. 2a, where the output phase is connected to the positive (P) voltage level (T_1 and T_2 are closed) for positive output current. In order to commutate to the neutral level (0) T_1 is opened and after the turn-on delay T_3 is closed additionaly. During the turn-off of T_1 the current naturally commutates over T_2 and D_3 to the neutral level. For a negative phase current (cf. Fig. 2b), the current commutates to the neutral after T_3 is closed.

If we switch back from (0) to (P), first T_3 is opened and after the turn-on delay T_1 is closed. For a positive phase current (cf. Fig. 2c) during turn-off of T_3 the current continues flowing

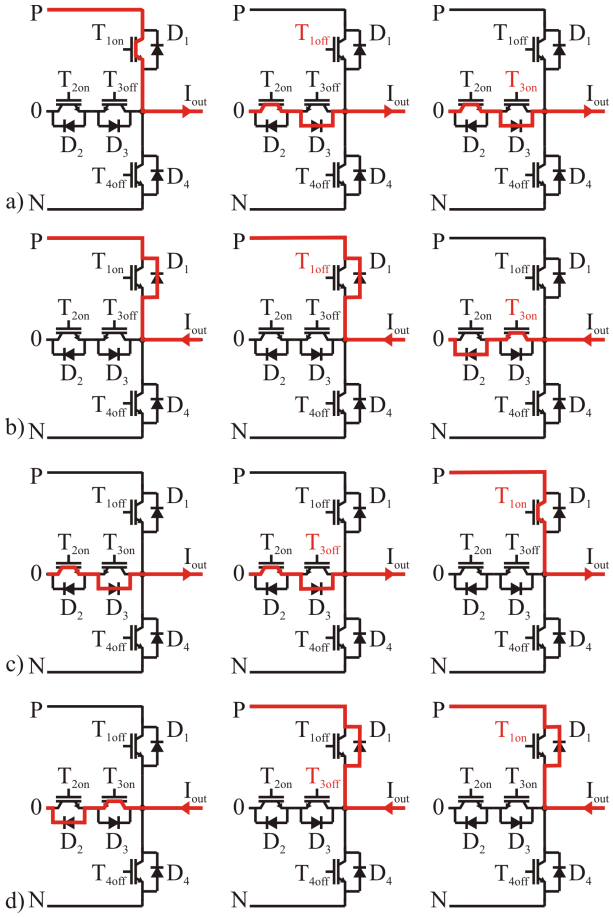

Fig. 2. Current commutation during switching transition (P → 0) for a) positive and b) negative output current. Current commutation during switching transition (0 → P) for c) positive and d) negative output current.

through D_3 and commutates to the positive voltage level after the turn-on of T_1. For a negative phase current (cf. Fig. 2d) the current commutates to D_1 during turn-off of T_3. This principle works for all remaining switching transitions.

The direct transition from (N) to (P) and vice versa is avoided by the implemented space vector modulation. This transition is not favorable for the T-type converter. For such a transition, a reverse recovery current pulse flows to the neutral voltage level because of the blocking voltage change from $-U_{dc}/2$ to $+U_{dc}/2$ over D_2 and D_3. This reverse recovery current produces additional losses in the diode and also in the IGBT.

B. Modulation

The T-type topology is modulated identically as the NPC converter. A space vector modulation scheme which incorporates optimal clamping of the phase with the highest current amplitude is implemented [11] in order to reduce the switching losses compared to sinusoidal PWM [12]. This strategy alternately loads the top and bottom DC-link capacitor with 3 times the fundamental frequency. If a DC-link balancing is necessary because of small capacitors the optimal clamping scheme cannot always be maintained as described in [13]. The

TABLE I
MEASURED SWITCHING LOSS ENERGIES FOR
$U = 300\,\mathrm{V}, I = 20\,\mathrm{A}, T_j = 125\,^\circ\mathrm{C}$.

Element	Energy	Datasheet difference
1200V IGBT turn on	0.81 mJ	-19%
1200V IGBT turn off	1.27 mJ	-5%
1200V Diode turn off	0.64 mJ	+22%
600V IGBT turn on	0.68 mJ	+90%
600V IGBT turn off	0.42 mJ	+9%
600V Diode turn off	0.31 mJ	+85%

variation of the neutral point potential can also be a problem under fault condition [14].

III. Efficiency Calculation and Comparison with the NPC Topology

A. Determination of the switching losses

The T-type topology is built with mixed semiconductor technology. 600 V IGBTs (or CoolMOS) and diodes are combined with 1200 V IGBTs. It would be inadequate to assume that the datasheet switching losses with simple scaling to the commutation voltage would be accurate enough to determine the switching losses of the T-type converter. The turn-on switching loss energy of the 1200 V IGBT will be lower if the commutating diode is only 600 V rated with considerably lower reverse recovery charge. In the same manner the 600 V device turn-on loss energy will be higher if the commutating diode is 1200 V rated.

In order to determine in which device switching losses occur depending on the switching transition and of what value these losses are a test setup with a single T-type bridge leg was assembled. The following devices have been tested:

- Infineon IGBT 1200V IKW25T120
- Infineon IGBT 600V IKW30N60T
- Infineon CoolMOS 600V IPW60R045CS

In table I the resulting switching loss energies and the deviation from the datasheet values are summarized. It can be seen that the 1200 V IGBT turn-on energy is 19% lower and the 600 V IGBT turn-on energy is 90% higher than the datasheet values (the datasheet switching loss energies are linearly scaled to a commutation voltage of 300 V, 20 A current and 125 °C junction temperature for this comparison). The switching losses will still be lower than for the 2-level VSC because the commutation voltage is only $U_{dc}/2$.

The implementation of the bidirectional switch with two 600 V CoolMOS obtained some severe disadvantages. Because the tested discrete devices do no have an optimized body diode, the reverse recovery charge is large. This manifests in the turn-on loss energy of the 1200 V IGBT which increased by factors compared to the datasheet value. Therefore, the 600 V IGBTs are used for the bidirectional switch in all further calculations.

B. Calculation of the converter efficiency

The T-type converter efficiency can be calculated if the operating point dependent losses are known. Conduction and switching losses are calculated with an algorithm described in [13], where a highly efficient 3-level NPC back-to-back converter prototype was presented (cf. Fig. 3). The calculation incorporates the space vector modulation such that the impact of optimal clamping is considered correctly. In order to use the algorithm, it has to be determined in which elements the switching losses occur depending on the switching transition. Table II summarizes the results. The diode turn-on energy is very small and is neglected. The direct transition from (P) to (N) and vice versa is omitted by the implemented space vector modulation.

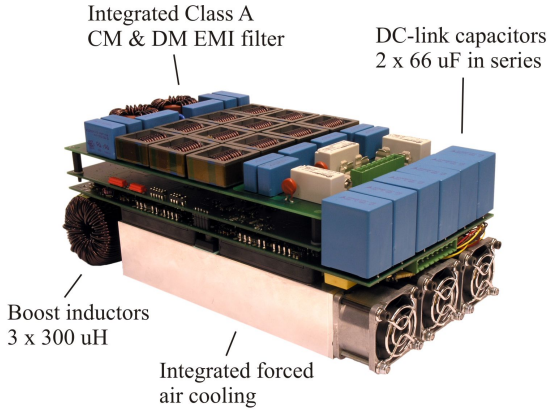

Fig. 3. 3-level NPC back-to-back converter prototype.

TABLE II
SWITCHING LOSS ENERGIES

Switching Transition	**Switching loss energies**
$I_{out} \geq 0$	
$P \rightarrow 0$	E_{T1off}
$0 \rightarrow P$	E_{T1on}, E_{D3off}
$N \rightarrow 0$	E_{T2on}, E_{D4off}
$0 \rightarrow N$	E_{T2off}
$I_{out} < 0$	
$P \rightarrow 0$	E_{T3on} E_{D1off},
$0 \rightarrow P$	E_{T3off}
$N \rightarrow 0$	E_{T4off}
$0 \rightarrow N$	E_{T4on}, E_{D2off}

The conduction losses are approximated piecewise linearly as described in [13] according to the datasheet values. Finally, the mean losses in each semiconductor and the efficiency of the 3-level T-type converter can be calculated. In Fig. 4 the pure semiconductor efficiency for rectifier operation ($\hat{U} = 325\,\mathrm{V}, \hat{I} = 21.5\,\mathrm{A}, \phi_1 = 180°$) and inverter operation ($\hat{U} = 325\,\mathrm{V}, \hat{I} = 21.5\,\mathrm{A}, \phi_1 = 0°$) of the T-type converter, the 2-level VSC with 1200 V IKW25T120 and the 3-level NPC with 600 V IKW30N60T switches is depicted. For the calculation of the 2-level and the 3-level NPC efficiency, the same algorithm accounting for the optimal clamping space vector modulation is used.

The efficiency of the T-type converter is outstanding for medium switching frequencies from $6-20\,\mathrm{kHz}$ (cf. Fig. 4). For a switching frequency above 20 kHz, the 3-level NPC topology is superior. The main benefit of the T-type topology comes from the reduced switching losses because the commutation

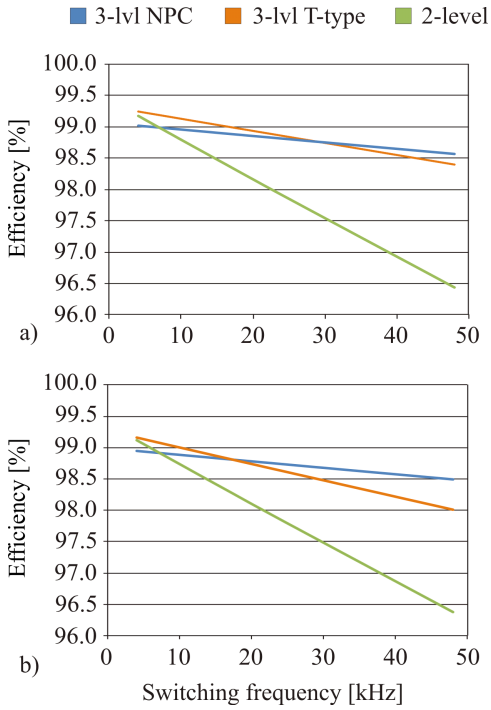

Fig. 4. Efficiency comparison between the different topologies. a) Rectifier operation with $\hat{U} = 325\,\mathrm{V}, \hat{I} = 21.5\,\mathrm{A}, \phi_1 = 180°$, b) inverter operation with $\hat{U} = 325\,\mathrm{V}, \hat{I} = 21.5\,\mathrm{A}, \phi_1 = 0°$. Switch types: Infineon IKW25T120 and IKW30N60T.

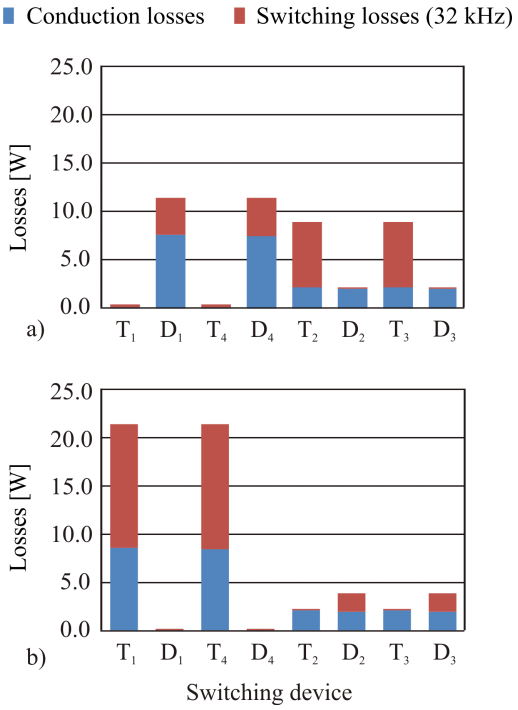

Fig. 5. Mean loss distribution in the T-type topology elements for a) rectifier operation, b) inverter operation.

voltage of the 1200 V devices is only 350 V instead of 700 V in the 2-level VSC. Compared to the 3-level NPC topology the conduction losses are lower because of only two devices being in series in the current path.

The comparison presented here is not completely fair because no switches with equivalent current rating have been available. Therefore, in the next section a loss comparison with variable semiconductor chip area is presented. This allows for a fair comparison of the three topologies and will reveal an interesting insight into the loss sharing between the different semiconductors.

IV. Chip Area based Comparison

The loss calculation algorithm provides the mean power losses in each semiconductor chip. If we have a look at these mean losses, depicted in Fig. 5, it can be seen that the loss sharing among the semiconductor chips is very uneven and depends on the operating point. For rectifier operation nearly no losses occur in the IGBTs T_1 and T_4, and for inverter operation the diodes D_1 and D_4 are almost not loaded. This unbalance is much more distinct than for the 2-level converter because of benefits in the modulation scheme. A similar unbalanced loss distribution can be observed for the 3-level NPC converter [13]. Furthermore, the power loss per semiconductor chip is small because the losses are distributed over many chips.

It is therefore advisable to reduce the chip sizes of the semiconductor chips with low power losses. Nowadays, the chip sizes in modules are over-dimensioned because they are designed as general purpose modules working in every possible operating point including reserves for fault cases. It is neglected that i.e. solar inverter or active rectifier modules always work with nearly constant modulation index and phase lag. The fundamental frequency is fixed to 50 or 60 Hz so only the mean chip losses are important and no peak power losses due to electrical stand-still can occur. If a big manufacturer for a mass product takes the decision for a converter topology, it should account for the possibility to produce a module optimized to this special application in order to reduce the semiconductor costs. Naturally, this makes only sense for fairly high product volume and if the converter failure modes are well defined.

The following chip area optimization has to be clearly understood as an optimization for the mentioned operating points, no reserves for fault cases are included.

The main idea is to adapt the chip sizes for each topology so that the junction temperature of each element reaches a mean value of $T_j = 125\,°\mathrm{C}$. The chip area for elements with low losses will be decreased, the area of elements with high losses will be increased. In order to perform this chip size optimization, the conduction loss model, the switching loss model, and the thermal model have to be adapted with the semiconductor chip area. A flow-chart of the optimization algorithm is depicted in Fig. 6.

The chip area of each element is limited to a minimum of $A_{min} = 2\,\mathrm{mm}^2$. This is due to unmodeled side effects becoming dominant for small chip sizes and due to the limits in the bonding technology.

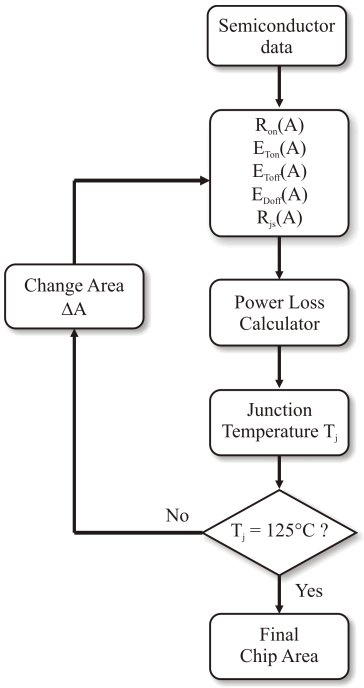

Fig. 6. Diagram of chip area optimization algorithm.

A. Chip area based loss modeling

The semiconductor loss models have to be adapted to account for a variable chip size. The approach has been presented in [15] for a semiconductor area based comparison of an indirect matrix converter, a current source converter and a 2-level voltage source converter.

The Infineon Trench and Field Stop 1200 V IGBT4 and 600 V IGBT3 series have been chosen as the data basis because of their good documentation and data availability. With a datasheet comparison, the chip die sizes depending on the current rating of the discretes are linearly fitted.

$$A_{T,1200V}(I_N) = 0.95\,\frac{\mathrm{mm}^2}{\mathrm{A}} \cdot I_N + 3.2\,\mathrm{mm}^2 \tag{1}$$

$$A_{D,1200V}(I_N) = 0.47\,\frac{\mathrm{mm}^2}{\mathrm{A}} \cdot I_N + 3.6\,\mathrm{mm}^2 \tag{2}$$

$$A_{T,600V}(I_N) = 0.55\,\frac{\mathrm{mm}^2}{\mathrm{A}} \cdot I_N - 0.32\,\mathrm{mm}^2 \tag{3}$$

$$A_{D,600V}(I_N) = 0.27\,\frac{\mathrm{mm}^2}{\mathrm{A}} \cdot I_N + 0.41\,\mathrm{mm}^2 \tag{4}$$

For each device, the conduction losses are modeled as follows:

$$P_{cond}(A,i) = U_{f,x} \cdot i + \frac{R_{on_N} \cdot A_N}{A} \cdot i^2 \tag{5}$$

The switching loss energies are also adapted to the area (cf. equations 6 to 11). This can be done in several ways. In this case, the datasheet values with the proposed gate resistors are linearly scaled to the same switched current and commutating voltage and linearly fitted over the area. In general, the switching losses scaled to the same current do not vary much with the chip size because a large chip is usually switched faster with a smaller gate resistor.

$$E_{Ton,1200V}(A,u,i) = (-5.4\mathrm{E}{-10} \cdot A + 1.9\mathrm{E}{-7}) \cdot u \cdot i \tag{6}$$

$$E_{Toff,1200V}(A,u,i) = (-4.3\mathrm{E}{-10} \cdot A + 2.1\mathrm{E}{-7}) \cdot u \cdot i \tag{7}$$

$$E_{Doff,1200V}(A,u,i) = (-1.6\mathrm{E}{-9} \cdot A + 1.2\mathrm{E}{-7}) \cdot u \cdot i \tag{8}$$

$$E_{Ton,600V}(A,u,i) = (6.8\mathrm{E}{-10} \cdot A + 4.4\mathrm{E}{-8}) \cdot u \cdot i \tag{9}$$

$$E_{Toff,600V}(A,u,i) = (3.1\mathrm{E}{-10} \cdot A + 5.7\mathrm{E}{-8}) \cdot u \cdot i \tag{10}$$

$$E_{Doff,600V}(A,u,i) = (9.3\mathrm{E}{-11} \cdot A + 2.7\mathrm{E}{-8}) \cdot u \cdot i \tag{11}$$

For the T-type topology the fitted switching loss energy curves have been simply shifted to the points determined with the test setup.

Finally, the thermal model has to be adapted. The same behavior for all chip types is assumed and the thermal resistor can be given with [15]:

$$R_{th,js}(A) = 23.94\,\frac{\mathrm{K}}{\mathrm{Wmm}^2} \cdot A^{-0.88} \tag{12}$$

The basic thermal model is very simple. The heat sink is assumed to be on a constant temperature of $T_{sink} = 80\,^{\circ}\mathrm{C}$. The junction temperature of each device can be calculated with:

$$T_j = T_{sink} + R_{th,js}(A) \cdot P_{tot}(A) \tag{13}$$

B. Chip area optimization results

The optimization algorithm calculates the losses for each topology and adapts the chip sizes until each element reaches a junction temperature of $T_j = 125\,^{\circ}\mathrm{C}$. This process also affects the total losses and the converter efficiency. Interestingly, the efficiency decreases only slightly because of the chip area is reduced for elements with low losses, and therefore, the absolute loss increase is very small.

If all chip sizes are summed up, the total chip area for a topology and the corresponding operating point is found. The total chip area is directly related to the costs. The major costs of a module are related to the chip area, the packaging technology and the bonding account only for 20% of the module costs.

The results of the optimization are depicted in Fig. 7. The total chip area is calculated for the 3 different topologies depending on the switching frequency.

Surprisingly, the total chip area of the 3-phase 3-level NPC and T-type topology is lower than for the 2-level VSC already for a switching frequency above 8 kHz in rectifier operation. The area increase with the switching frequency is the lowest for the 3-level NPC topology because of the small switching losses. At a switching frequency of 32 kHz, the necessary chip area for the 2-level VSC is nearly twice the area of the 3-level NPC. The same dependency for the total chip area can be observed for inverter operation (cf. Fig. 7b) although the detailed chip area allocation changes.

In order to make a statement about the chip sizes of a general purpose module, the maximum of the chip sizes from rectifier and inverter operation have been chosen (cf. Fig. 8). For a switching frequency of 8 kHz, the 3-level NPC topology needs the most chip area as expected. If the switching frequency is increased to 32 kHz the picture changes completely. The semiconductor area of the 2-level topology

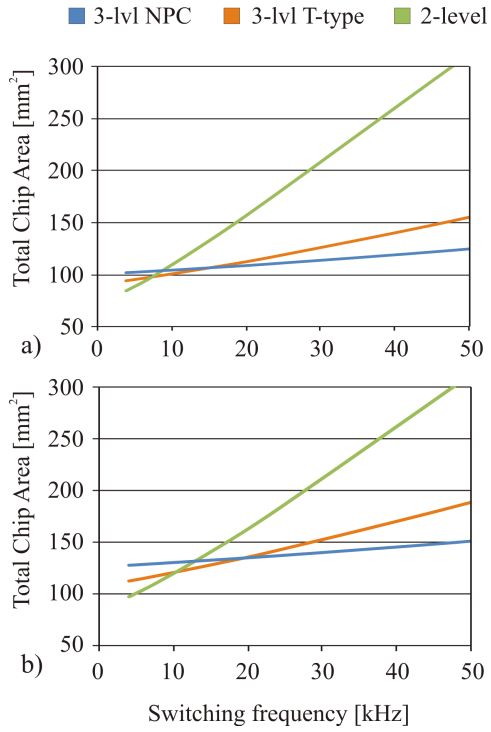

Fig. 7. Comparison of the total semiconductor area depending on the frequency. a) Rectifier operation, b) inverter operation.

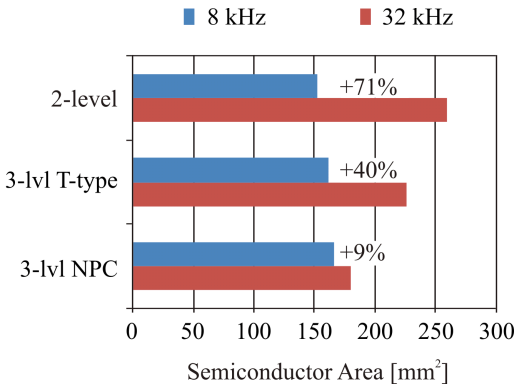

Fig. 8. Increase of total semiconductor area for mixed mode operation.

increases by 71% and is 45% higher than the 3-level NPC topology chip area.

The general belief that a 3-level topology would need more silicon chip area than a corresponding 2-level topology has been disproved. The part count and the count for external circuitry such as gate drives and isolated voltages is increased but the total chip area can be even lower for a high switching frequency. This will for sure have a positive impact on the costs of an optimized 3-level module.

V. Conclusion

In this paper a 3-phase 3-level T-type converter topology is presented. It is an alternative to the 2-level VSC for medium switching frequency applications and is very efficient in the range of $4 - 20\,\mathrm{kHz}$. The main advantage comes from the halved commutation voltage which reduces the switching losses compared to the 2-level topology. The conduction losses do not change considerably. The realization of the bidirectional switch to the mid-point of the dc-link with two anti-serial $600\,\mathrm{V}$ IGBTs or $600\,\mathrm{V}$ CoolMOS has been investigated. A simple commutation scheme which is independent on the current direction is presented.

In the second part of the paper a chip area comparison between 2-level VSC, 3-level NPC and T-type converter has been presented. The comparative evaluation reveals that the semiconductor chip area can be considerably reduced for the multilevel topologies as the losses are shared over many components. Surprisingly, the required total chip area is lower in the 3-level topologies for switching frequencies above $10\,\mathrm{kHz}$. The reduced semiconductor area can decrease the costs of a highly specialized 3-level module.

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