Three-Phase PWM Power Conversion – The Route to Ultra High Power Density and Efficiency

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Abstract. A review of three-phase PWM converter topologies which do show a low complexity / high reliability and high efficiency and power density and are therefore of main interest for a future industrial application is presented. A three-switch/level boost-type PWM rectifier (*VIENNA Rectifier*), a buck+boost-type PWM rectifier with wide output voltage range and the AC/AC *Sparse Matrix Converter* concept are discussed in detail and topics to be treated in the course of further research are identified. Finally, it is shown how the aspects being relevant for the realization of highly compact converter systems could be integrated into education in the field.

1. Introduction

Due to guidelines, recommendations and regulations concerning a limitation of the harmonic influence of power electronic systems on the mains and based on the requirement of operation in a wide input voltage range numerous three-phase PWM converter topologies with low effects on the mains have been proposed [1]. After the clarification of the basic operating behavior and the optimization of the modulation and control scheme of each converter topology current research is aiming for an increase of the power density and efficiency under application of novel power semiconductor technologies and materials (SiC), and novel interconnection and cooling concepts. There, the focus is on topologies which do show a low complexity and/or high reliability, a low stress on the power semiconductors and a low volume of the passive power components.

Therefore, in this paper a review of three-phase PWM converter topologies which are of main interest for a future industrial application, i.e. the *VIENNA Rectifier* (cf. **Section 2**), the three-phase buck+boost rectifier (cf. **Section 3**) and the *Sparse Matrix Converter* (cf. **Section 4**) will be given and topics for further research will be identified.

For the realization of ultra-compact power electronic systems a well founded knowledge in circuit theory and control engineering and a sound understanding of the basics of the thermal and electromagnetic behavior is a strict requirement. Therefore, in conclusion it is discussed briefly how these areas could be integrated into modern education in order to ensure a further dynamic development of the field.

2. Three-Switch/Level Boost-Type PWM Rectifier

An unidirectional three-phase PWM rectifier system with ohmic fundamental mains behavior and controlled output voltage can be realized in the form of a star-connection of single-phase AC/DC converters (*Y-Rectifier*, cf. **Fig.1**(a)) or, as proposed in [2] in the form of the *VIENNA Rectifier* (cf. Fig.1(b)). As compared to a conventional bidirectional (two-level) PWM AC/DC converter (cf. **Fig.2**) both circuit topologies do show a three-level characteristic of the bridge legs and accordingly a significantly lower voltage stress on the power semiconductors. Furthermore, for given rms value of the ripple of the input current and given switching frequency the three-level characteristic does allow a reduction of the inductance of the input inductors resulting in a high system power density.

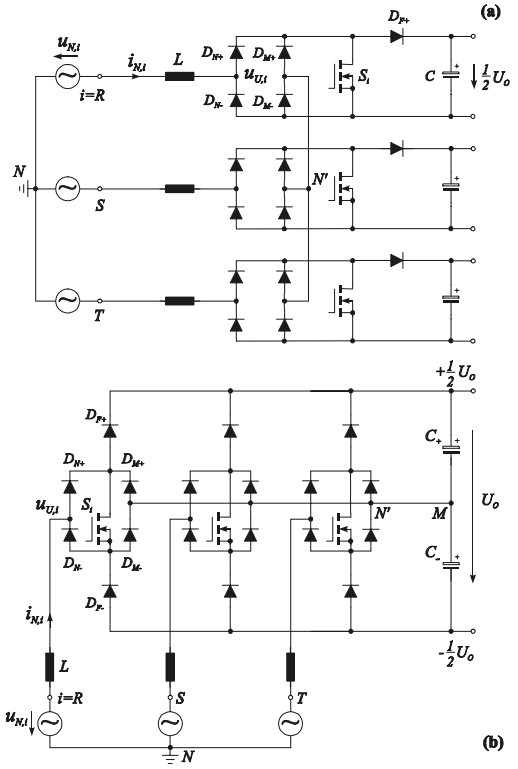

Fig.1: Realization of a three-phase unidirectional boost-type PWM rectifier system by star-connection of single-phase PWM rectifier systems **(a)** or in the form of the VIENNA Rectifier **(b)**.

The main advantage of the system shown in Fig.1(b) as compared to Fig.1(a) is a single output voltage being common to all bridge legs. This does allow to minimize the realization effort in case a mains voltage hold-up or a high-frequency isolation of the output voltage has to be provided. Accordingly, the system is applied in the industry in high-power telecommunications power supply modules, process technology power supplies and AC drives without requirement of feeding braking energy back into the mains.

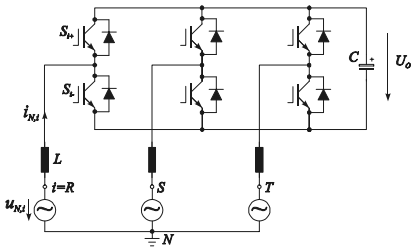

Fig.2: Structure of the power circuit of a conventional voltage DC link PWM converter (shown for application as PWM rectifier).

Further topologies for the realization of a bridge leg of the VIENNA Rectifier are shown in **Fig.3**. As Fig.3(b) clearly shows, the voltage formation $u_{u,i}$ at the input of a phase leg is not only dependent on the switching state of the power transistor S_i but also on the sign of corresponding phase current $i_{N,i}$. The space vectors of the phase voltages $u_{U,i}$ which can be formed for $i_{N,R}>0$, $i_{N,S}$, $i_{N,T}<0$ are depicted in **Fig.4**.

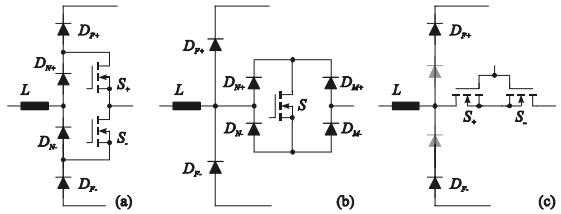

Fig.3: Bridge leg topologies of the VIENNA Rectifier alternative to Fig.1(b). As for the realization shown in Fig.1(b), for **(a)** (cf. [3]) the voltage stress on all power semiconductors is defined by half the output voltage. For **(b)** and **(c)** the blocking voltage of the diodes D_{F+}, D_{F-} is determined by the total output voltage; accordingly a series connection of two diodes with lower blocking capability and/or lower reverse recovery time should be employed.

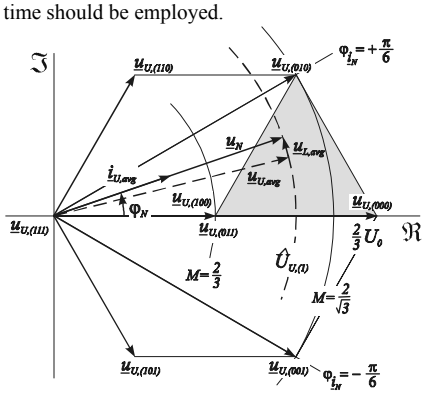

Fig.4: Space vectors of the VIENNA Rectifier available for the formation of the input voltage.

As for conventional three-level PWM converters the redundant switching states (cf. e.g. $\underline{u}_{U,(100)}$ and $\underline{u}_{U,(011)}$ in Fig.4) do allow a balancing of the partial output voltages u_{C+} and u_{C-}.

With respect to a continuation of the operation in the case of a failure of a mains phase the input current control does refer to phase quantities instead of employing space vector calculus as known from the control of three-phase AC machines. The cascaded control structure, i.e. the outer output voltage control loop and the underlying mains current control, is shown in **Fig.5.**

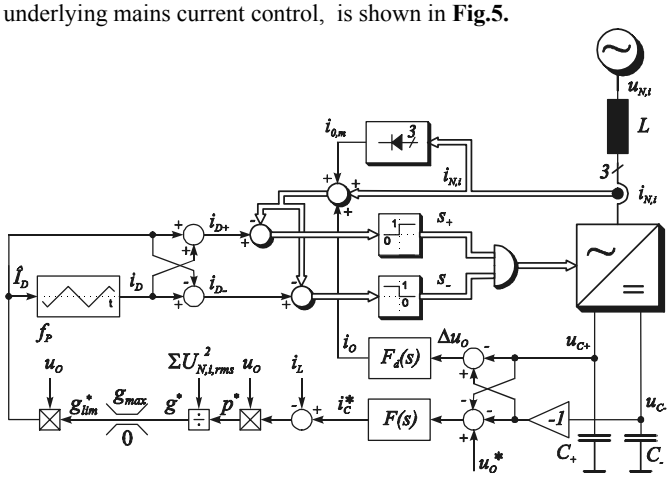

Fig.5: Control of the output voltage of the VIENNA Rectifier with underlying mains phase current control [4].

The output voltage controller *F(s)* shows a non-linear gain in dependency on the control error and does define the reference value i_C* of the current charging the output capacitors and/or the reference value p* of the input power, where a load current pre-control i_L is considered. Under consideration of the actual mains voltage condition p* is translated into a conductance reference value g* to be represented at the input of each phase. By limitation of g* the phase currents are limited in amplitude according to the dimensioning of the system, the conductance g^*_{lim} does directly define the amplitude $\hat{I}_D$ of the triangular carrier signal i_D of the multiplier-free phase current control [4] which in contrast to conventional average current mode control does not rely on a pre-control of the mains voltage. A full utilization of the output voltage for input current control is achieved by extending the measured actual phase currents $i_{N,i}$ by a triangular-shaped zero-sequence signal $i_{0,m}$ with three times the mains frequency. The balancing of the partial output voltages is realized by shifting the modulating signals by a positive or negative offset i_0. As a positive and a negative triangular carrier signal, i_{D+} and i_{D-} is employed, the dependency of the voltage formation on the sign of the phase currents can be considered by an AND gate combining the switching signals $s_{+,i}$ and $s_{-,i}$ in each phase.

The practical realization of a wide input voltage range ($U_{N,l-l}$ =320…530V_{rms}) 12.5kW / 800V_{DC} output *VIENNA Rectifier* employing CoolMOS power transistors and operating at f_P=38kHz in a bridge leg topology according to Fig.3(a) is depicted in **Fig.6**. There, in each phase the diode D_{F+} is replaced by a thyristor which does short-circuit the corresponding pre-charging resistor after start-up. The unit shows a height of 2-U; in combination with a footprint of 250x160mm^2 this results in a power density of ρ=3.5kW/dm^3.

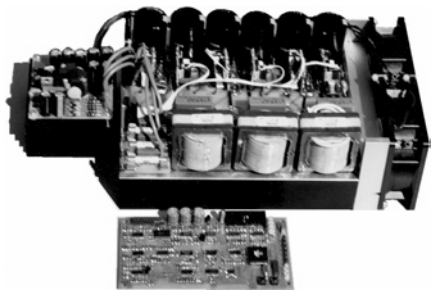

Fig.6: Prototype of the VIENNA Rectifier. The control board is shown in front of the power circuit, the auxiliary power supply is shown on the left hand side.

For the output voltage control and system management (start-up, failure handling etc.) a low-cost microcontroller is employed. Functions requiring a high bandwidth, e.g. the phase current control are realized in analog technique.

Results of an experimental analysis of the prototype shown in Fig.6 are depicted in **Fig.7** and **Fig.8.**

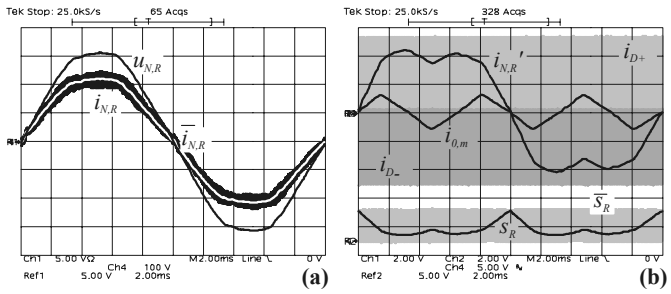

Fig.7: Time behavior **(a)** of a mains phase voltage $u_{N,R}$ (100V/div) and of the corresponding input current $i_{N,R}$ (5A/div) recorded in peak detection and high resolution mode and **(b)** modulating input current $i_{N,R}'$ (cf. Fig.5), triangular carrier signals i_{D+} and i_{D-} and switching signal s_R of phase R (instantaneous and local average value). Operating parameters: $U_{N,l-l}$=400V_{rms}, U_O=675V, P_O=5.1kW.

The mains phase currents are controlled proportional to the corresponding phase voltages, accordingly the distortion of the mains current of THD_I≈4% is mainly caused by low-frequency harmonics of the mains voltage which shows a total harmonic distortion of THD_V =2.7%. One has to point out the high system efficiency of η≈98% at rated mains voltage. For high-frequency isolation of the rectifier output voltage this does allow to achieve an overall efficiency of η_g≈93% despite the two-stage energy

conversion. In contrast, single-stage PWM rectifier systems with integrated high frequency isolation [5] are characterized by an efficiency of $\eta_g \approx 90\%$ due to the required higher blocking capability of the power semiconductors and/or the higher turn-of voltage causing significantly higher switching losses.

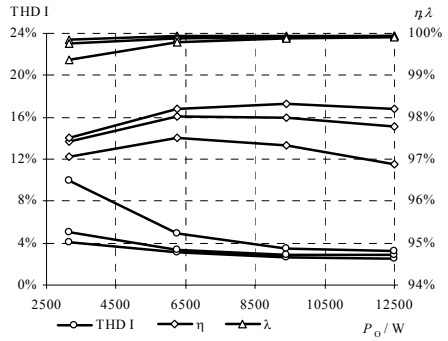

Fig.8: Dependency of the THD_I of the input current, of the power factor λ and of the efficiency η on the output power and input voltage.

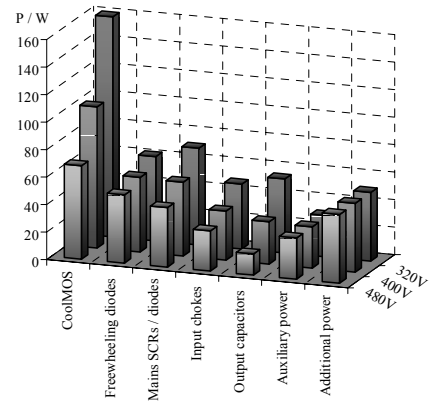

Fig.9: Losses of the power components for different line-to-line input voltages.

The distribution of the losses to the power components given for different input voltages is shown in **Fig.9**. At low input voltages the loss balance is dominated by the conduction losses of the power transistors which could be lowered by connecting two devices in parallel.

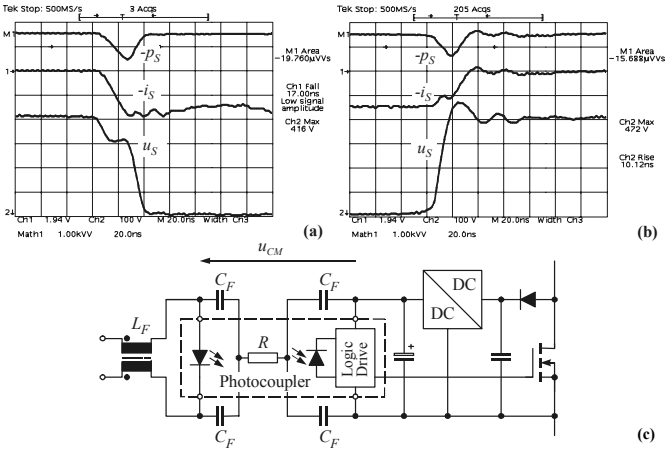

Fig.10: Switching behavior of a CoolMOS power transistor (Infineon, SPW47N60C2) in combination with two SiC freewheeling diodes SDB06S60 connected in parallel for application in a boost converter topology. Shown are transistor voltage u_S (100V/div), transistor current i_S (20A/div) and the transistor switching power loss p_S (10kW/div) for turn-on **(a)** and turn-off **(b)**. Furthermore shown: common mode filtering for lowering the du_{CM}/dt occurring across the photocoupler.

It has to be pointed out that an increase of the switching frequency would not result in a lower overall converter volume as the reduction of the volume of the input inductors would be overcompensated by the increase of the heat sink volume being required for remaining a given power semiconductors junction temperature at higher losses.

A higher converter power density could be achieved by employing SiC Schottky diodes as free-wheeling diodes. This however would require a low inductance wiring of the power semiconductors other than a PCB board in order to allow a full utilization of the high switching speed. There, also the du_{CM}/dt-immunity of the isolated gate drive circuits would have to be considered in detail. According to **Fig.10** for the combination of a CoolMOS power transistor and a SiC Schottky Diode in a boost converter topology a rate of change of the common mode voltage of du_{CM}/dt >40kV/µs does occur. Therefore, commercially available optically isolated gate drive circuits which are typically specified for du_{CM}/dt <15kV/µs could only be employed in combination with a common-mode filter (cf. Fig.10(c)).

In case an isolation of the output voltage has to be provided, for realizing a rectifier system with high power density alternatively to the VIENNA Rectifier a three-level Y-Rectifier (cf. **Fig.11)** which up to now has not been analyzed in the literature should be considered. There, for operation in the European $400V_{rms}$ (line-to-line) mains 300V power semiconductor technology could be employed for the free-wheeling diodes and the power transistors. As compared to the VIENNA Rectifier the system does allow a reduction of the inductance of the input inductors by a factor of 5(!) due to the lower transistor turn-off voltage and/or low switching losses and due to the larger number of switching states available for the input voltage formation. On the other hand the system shows higher conduction losses than the VIENNA Rectifier due to higher number of power semiconductors lying in the current path.

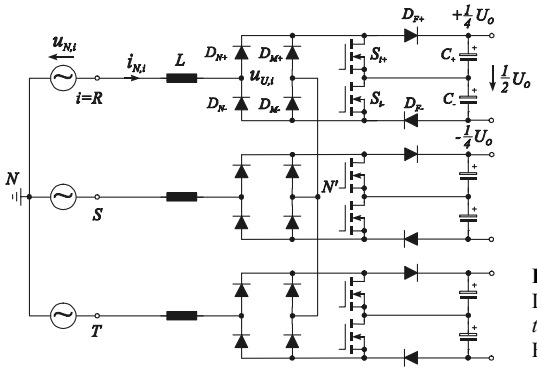

Fig.11: Three-Level *Y-Rectifier* (cf. also Fig.1(a)).

The high redundancy of switching states concerning the input voltage formation (cf. **Fig.12**) does allow a balancing of the partial output voltages as well as an equal distribution of the total output power to the phase systems. A detailed comparative evaluation of the three-level Y-Rectifier and the VIENNA Rectifier will be published by the authors in the near future.

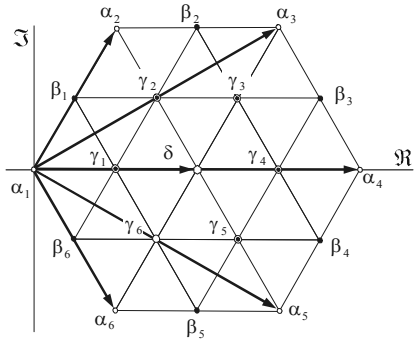

Fig.12: Input voltage space vectors of the three-level *Y-Rectifier* in comparison to the VIENNA Rectifier (α_i and δ). The redundancy r of switching state δ is r_δ =10, for the vectors β_i and γ_i we have r_β=2 and/or r_γ =6.

A further possibility of increasing the power density of boost-type PWM rectifier systems is given by the minimization of the volume of the mains side filter attenuating conducted EMI emissions.

There, it is important to point out that the realization of the input inductors on a three-limb magnetic core does not show a common-mode (zero-sequence) impedance in case the stray inductance of the phase windings and the yoke flux is neglected (cf. **Fig.13**). Therefore, a three-phase realization is of no direct advantage as compared to employing individual inductors in each phase.

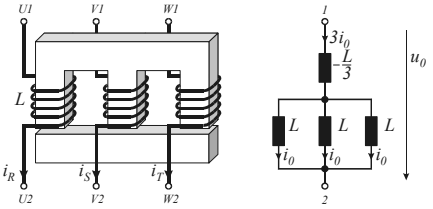

Fig.13: Realization of a three-phase inductor employing a three-limb magnetic core and common-mode equivalent circuit.

In contrast the application of ´zero´-ripple techniques which for the sake of clearness are shown in **Fig.14** and **Fig.15** for a DC/DC boost converter does allow a significant reduction of the EMI filter volume and losses. There, by arranging a secondary winding L_s on the input inductor L_p of the PWM rectifier and by realizing a defined magnetic coupling of both windings with the help of an

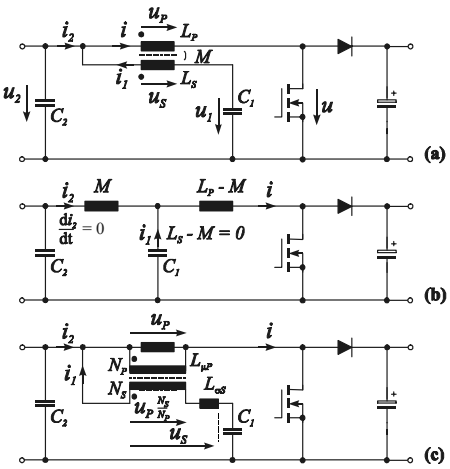

Fig.14: ´Zero´-ripple input filter of a DC/DC boost converter as proposed in [6]. As ´zero´-ripple condition we have L_s=M. This is identical to conventional ´zero´-ripple filtering according to Fig.14. The advantage of the approach shown as compared to Fig.14 is a lower number of turns N_s; however, the current i in L_p does show a switching frequency ripple.

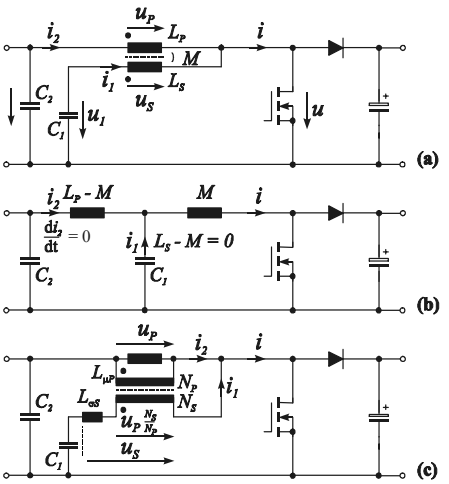

Fig.15: Conventional ´zero´-ripple input filter [7] shown for a DC/DC boost converter. As zero-ripple condition we have L_s=M. As compared to the realization depicted in Fig.13 the filter requires a higher number of turns L_s, however no switching frequency ripple is present in the current carried by the input inductor L_p.

auxiliary inductor $L_{\sigma s}$ (cf. Figs.14(c) and 15(c)) a two-stage LC-filter can be realized (cf. equivalent circuits Figs.14(b) and 15(b)). There, only L_p is carrying the load current. The current i_1 in L_s (and/or $L_{\sigma s}$) does not show a DC component, the rms value of i_1 is only determined by the ripple of the input inductor without filter. Therefore, at very low overall volume a filter attenuation in the range of 60…80dB can be achieved. A detailed analysis of the application of ´zero´-ripple techniques in three-phase boost-type PWM rectifier systems will be the topic of a paper to be published in near future.

3. Three-Phase Buck+Boost-Type PWM Rectifier

The function of a boost-type PWM rectifier system in principle is dependent on a DC output voltage level being higher than the amplitude of the mains line-to-line voltage. Therefore, in case the output voltage should be varied in a wide range a buck-derived system and/or a combination of a buck-type and a boost-type converter topology has to be employed.

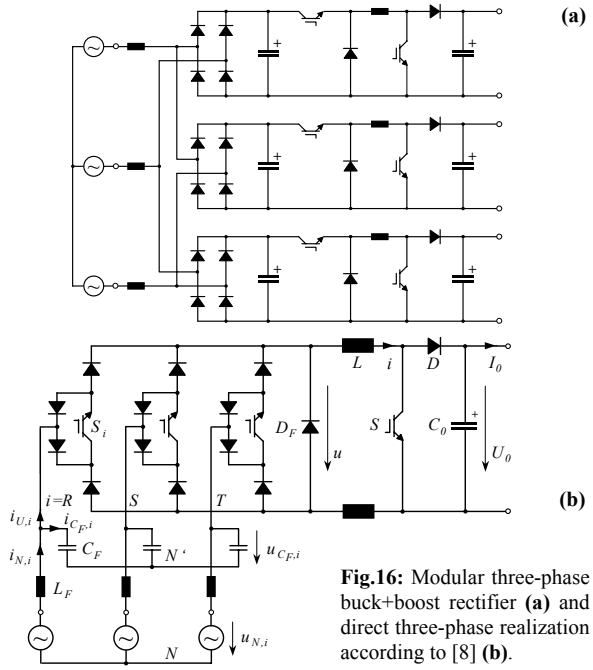

Fig.16: Modular three-phase buck+boost rectifier **(a)** and direct three-phase realization according to [8] **(b)**.

In [8] starting from a phase modular topology (cf. **Fig.16**(a)) a unidirectional buck+boost PWM rectifier system (cf. Fig.16(b)) has been proposed where analogous to the VIENNA Rectifier only a single power transistor is employed per phase for shaping the input current. By integration of a DC/DC boost converter stage into the converter output a sinusoidal shape of the mains current can be maintained also in the case of a phase loss. Therefore, the system could be employed for feeding the variable DC voltage link of square-wave inverter drives for HVAC applications as well as for the realization of the input stage of wide input voltage range high-power telecommunications power supply modules. There, the high frequency isolation of the output voltage advantageously could be realized as known from single-phase PWM rectifier systems with sinusoidal input current and typ. 385…400V_{DC} output. Further advantages as compared to boost-type systems are the possibility of a direct pre-charging of the output voltage at start-up and/or of an overcurrent limitation in the case of an output voltage short circuit condition.

For the turn-on state of the power transistor S_i the function of a bridge leg of the circuit shown in Fig.16(b) is equivalent to the bridge leg of a conventional diode bridge (cf. **Fig.17**). Accordingly, the current i being impressed by the buck+boost inductor can be distributed to the mains phases by proper PWM where after low-pass filtering a sinusoidal shape of the mains current does

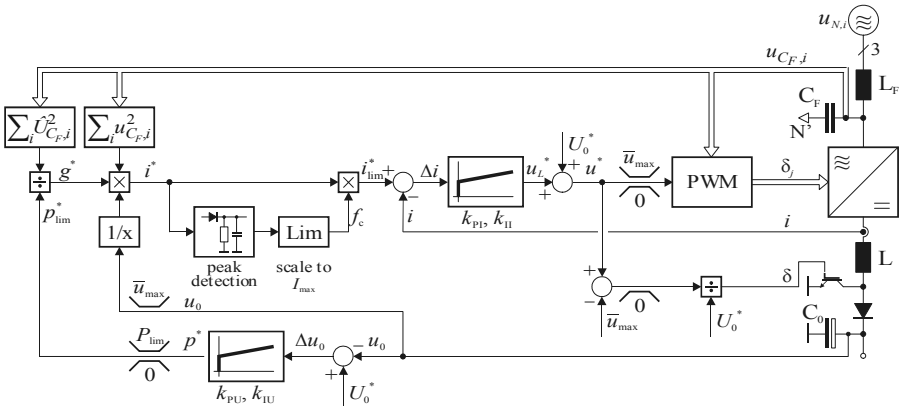

Fig.20: Structure of the control of a three-phase buck+boost rectifier guaranteeing unity power factor operation also under heavily unbalanced mains condition and/or for loss of a mains phase. For the sake of clearness the active damping of the input filter is not shown.

result. Therefore, for proper dimensioning of the filter capacitors C_F the system shows a power factor of $\lambda \approx 1.0$.

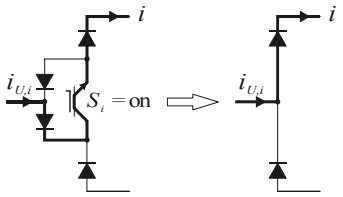

Fig.17: For the turn-on state of the power transistor S_i the function of a bridge leg is equivalent to the bridge leg of a conventional diode bridge.

Besides the switching states of the power transistors also the input voltage condition does take influence on the formation of the input phase currents $i_{U,i}$. The input current space vectors being available for $u_{N,R}>0$, $u_{N,R}>u_{N,S}>u_{N,T}$ are depicted in **Fig.18**. The redundancy of switching states concerning the resulting input current condition can be employed for an optimization of the system behavior.

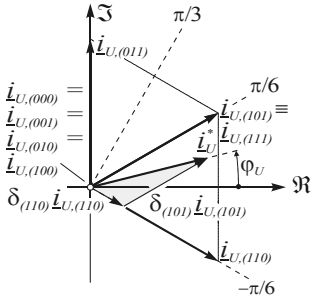

Fig. 18: Space vectors available for the formation of the input phase currents for $u_{N,R}>0$, $u_{N,R}>u_{N,S}>u_{N,T}$.

As shown in [9] for remaining always the power transistor of the phase showing the lowest absolute instantaneous value in the on-state (cf. **Fig.19**) a minimum rms value of the input filter capacitor voltage ripple and of the buck+boost inductor current ripple is achieved for given switching losses.

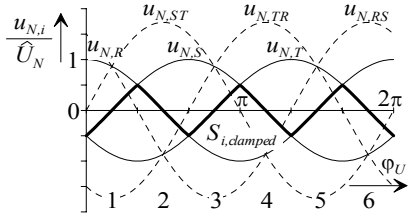

Fig.19: Optimum control of the buck+ boost rectifier. The bridge leg with the lowest absolute value of the corresponding phase voltage is clamped in the turn-on state.

The structure of the rectifier control [10] is shown in **Fig.20**. Analogous to Fig.5 the control is related to phase quantities. Again, an input conductance reference value g^* being essentially constant over a mains period is determined which does provide the basis for the calculation of the reference value i^* of the current in the buck+boost inductor where the actual mains voltage condition is considered. For asymmetric mains and/or loss of a phase, i.e. two-phase operation, the maximum output voltage $\bar{u}_{max}$ of the buck-stage is in intervals of a mains period lower than the output voltage reference value U_O^*. The desired output voltage therefore only can be achieved by activating the boost stage (cf. **Fig.21**).

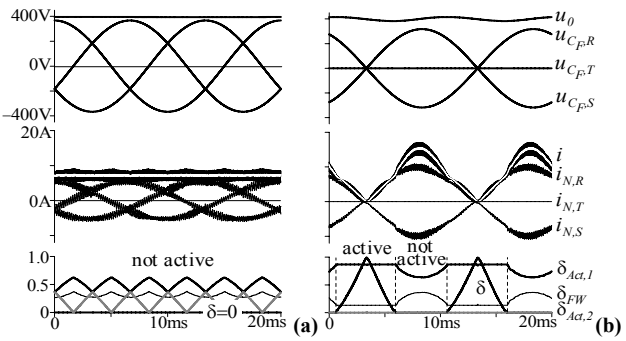

Fig.21: Simulation of the stationary operating behavior of the buck+boost rectifier for symmetric mains **(a)** and failure of mains phase *T* **(b)**. δ denotes the relative turn-on time of the boost stage power transistor, δ_{Act1}, δ_{Act2} and δ_{FW} do denote the relative on-time of the buck-stage current-forming states and of the free-wheeling state.

Results of an experimental analysis of the rectifier prototype (cf. **Fig.22**) are shown in **Fig.23** and **Fig.24**. For the failure of a mains phase (loss of phase *T*) the DC link current *i* assumes the shape shown in Fig.21(b) which is characterized by a pulsation with twice the mains frequency and the system continues to draw a sinusoidal current lying in phase with the remaining mains line-to-line voltage.

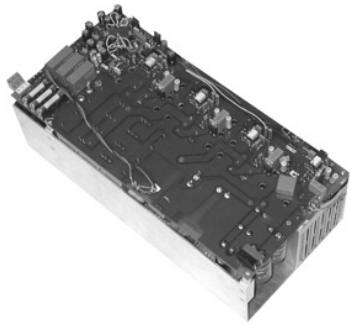

Fig.22: Prototype of the buck+boost rectifier system realized in IGBT technology (switching frequency f_P= 23.4kHz) and designed for wide input voltage range $U_{N,l\text{-}l}$ = 208…480V_{rms} and 6kW/ 400V_{DC} output. Overall dimensions: 34x16x12cm^3 corresponding to a power density of ρ= 0.92kW/dm^3. The system control is realized by a digital signal processor (not shown).

For an input power of $P_O \geq$2kW the rectifier system shows a power factor of PF=$\lambda \approx$0.98. For high input voltage and/or low output

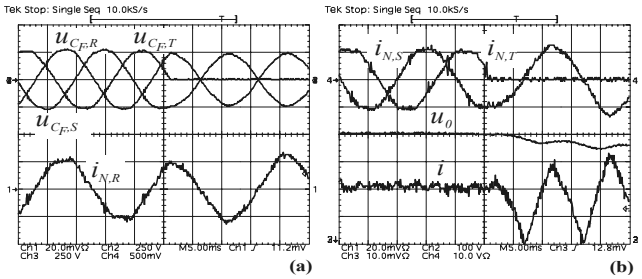

Fig.23: Experimental analysis of the rectifier operating behavior for loss **(a)** and reconnection **(b)** of mains phase *T*. Shown are the input filter capacitor voltage $u_{CF,i}$ (250V/div), the output voltage u_O (100V/div) and the mains phase currents $i_{N,i}$ and the DC link current i (5A/div). Operating condition: $330V_{rms}$ line-to-line input, $2.2kW/400V_{DC}$ output.

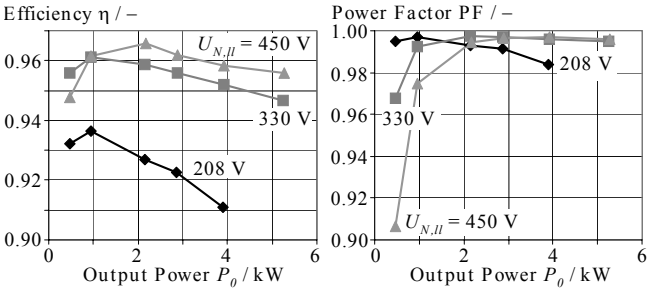

Fig.24: Dependency of the efficiency η and of the power factor PF(=λ) of the system shown in Fig.22 on the output power and on the input voltage (U_O=400V).

power the input current does show a relatively high share of the input filter capacitor current, accordingly lower values of the power factor do occur.

For P_O>1kW, i.e. for an output power being higher than 20% of the rated power and for rated input voltage $U_{N,l\text{-}l}$=$400V_{rms}$ the efficiency is close to η=96%. For low input voltage due to relatively high conduction losses of the power transistors and due to high ohmic losses in the buck+boost inductor winding a relatively low efficiency does result. Therefore, by employing high switching speed and/or ultra fast recovery power semiconductors only the efficiency at high input voltages (and/or high power semiconductor switching voltage) could be improved.

In summary, for the realization of a PWM rectifier system with high efficiency and wide input voltage range and low output voltage or wide output voltage range the system depicted in Fig.16(b) should be comparatively evaluated concerning losses and volume against a combination of a VIENNA Rectifier and a non-isolated DC/DC buck converter where the VIENNA Rectifier output voltage should be varied in dependency of the mains voltage in order to minimize the power transistor losses.

4. Three-Phase Sparse Matrix AC-AC Converter

For the conversion of the three-phase mains voltage into a three-phase voltage systems of defineable frequency and amplitude a combination of a voltage DC link or current DC link PWM rectifier and PWM inverter or a matrix converter topology could be employed (cf. **Fig.25**).

Conventional matrix converters (CMC, cf. **Fig.26**) do employ a large number of turn-off power semiconductors and are characterized by a complex multi-stage commutation strategy. In contrast, *Sparse Matrix Converters* (SMC) as proposed in [11] (cf. **Fig.27**) do show a significantly lower realization effort and furthermore do provide a degree of freedom for control

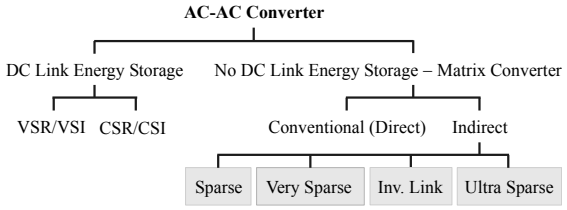

Fig.25: Classification of AC-AC converter topologies.

which is not available for CMC and which does allow to implement a commutation strategy of low complexity in order to ensure continuity of the load current and/or to avoid a short circuit of a line-to-line input voltage.

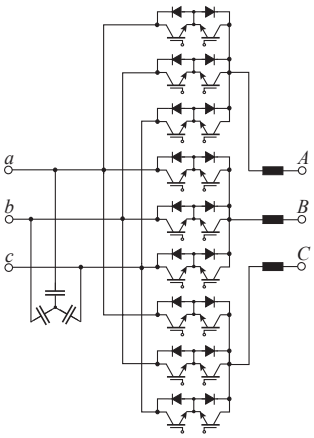

Fig.26: Structure of the power circuit of the conventional matrix converter (CMC) employing 18 unipolar turn-off power semiconductors and 18 diodes.

The advantages of a Sparse Matrix Converter as compared to a conventional DC voltage link AC-AC converter topology are immediately obvious from **Fig.28**. In case the DC link voltage is impressed by a DC link capacitor *C* switching losses do occur for the rectifier as well as for the inverter stage. In contrast, for the

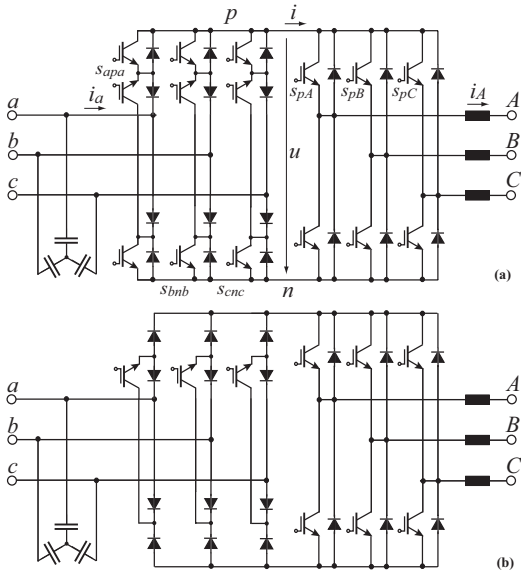

Fig.27: Topology of the *Sparse Matrix Converter* (SMC, [10]) (a) and of the *Ultra Sparse Matrix Converter* (USMC, [10]) (b). The USMC is limited to unidirectional power flow, i.e. rectifier operation.

SMC switching losses only do occur for the input *or* for the output stage. Therefore, the main advantage of a SMC as compared to a conventional DC link converter topology is not a lower volume of the passive power components (as also for the SMC for defining the input filter characteristic independent from the inner mains impedance input inductors have to be provided) but a potentially

higher efficiency of the energy conversion at high switching frequency. As a disadvantage of the SMC (and of the CMC) one has to accept a relatively low maximum amplitude of the output voltage.

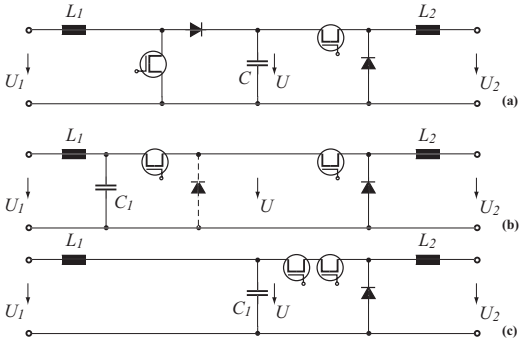

Fig.28: DC-DC equivalent circuit of a three-phase AC-AC converter with DC voltage link **(a)** and of a SMC **(b)**. The filter capacitor C_1 of the SMC could also be employed as a DC link capacitor (with low energy storage capability). Furthermore shown: functional equivalent circuit **(c)** of (b).

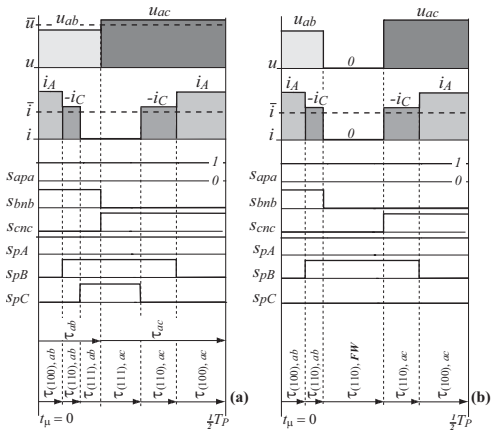

Fig.29: Commutation strategies of a SMC shown at the example of typical switching state sequences occurring within a pulse half interval. Commutation of the input stage at zero DC link current i=0 [12] **(a)** and commutation initiated by the input stage **(b)**.

Commutation strategies of the SMC are shown in **Fig.29**. In case the output stage is switched into the free-wheeling state in advance to the input stage commutation the change of the switching state of the input stage is at zero current, i=0. Therefore, (ideally) no switching losses do occur (cf. Fig.29(a), the dead time between turn-off of S_{bnb} and turn-on of S_{cnc} which has to be considered for a practical application is not shown). Alternatively, for positive DC link current the output stage could be forced into free-wheeling operation also by turning off a power transistor of the input stage (cf. Fig.29(b)). In case the switching state of the output stage is not changed, the input stage furthermore takes over the switching losses for applying the subsequent mains line-to-line voltage to the DC link and/or to the load. This allows to balance the thermal stress on the semiconductors of the SMC input and output stage.

A further degree of freedom of the modulation of the SMC is obvious from **Fig.30**. For the formation of an output voltage of high amplitude in each pulse half period the line-to-line mains voltages showing the highest and the second-highest instantaneous value are employed (cf. Fig.30(a)). In case an output voltage with low amplitude has to be generated the lowest positive and the second highest positive line-to-line voltage are applied to the DC link (cf. Fig.30(b)). As the switching losses of the output stage are in a first approximation proportional to the turn-off, i.e. to

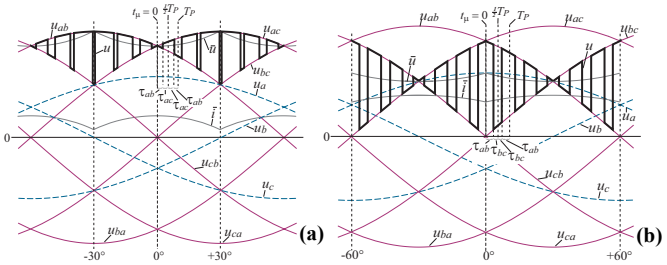

Fig.30: Modulation of the SMC for generating an output voltage of high amplitude **(a)** and for low output voltage **(b)**.

the DC link voltage this does result in a reduction of the output stage switching losses. A comparative evaluation of both modulation schemes concerning switching losses and the resulting rms value of the output current and input capacitor voltage ripple is the topic of current research and will be published by the authors in near future.

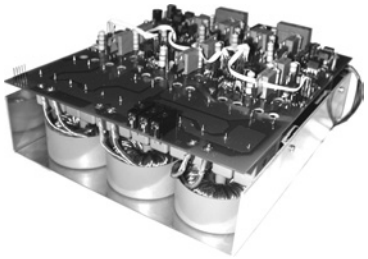

Fig.31: Protoype of a 10kW SMC. The system control (not shown) is realized by a DSP in combination with programmable logic devices. The overall dimensions of the system including the input filter are 24x20x8.5cm^3 resulting in a power density of ρ=2.5kW/dm^3.

Results of a digital simulation and of an experimental analysis of the SMC as derived from a 10kW prototype (cf. **Fig.31**) for modulation according to Fig.30(a) are compiled in **Fig.32.**

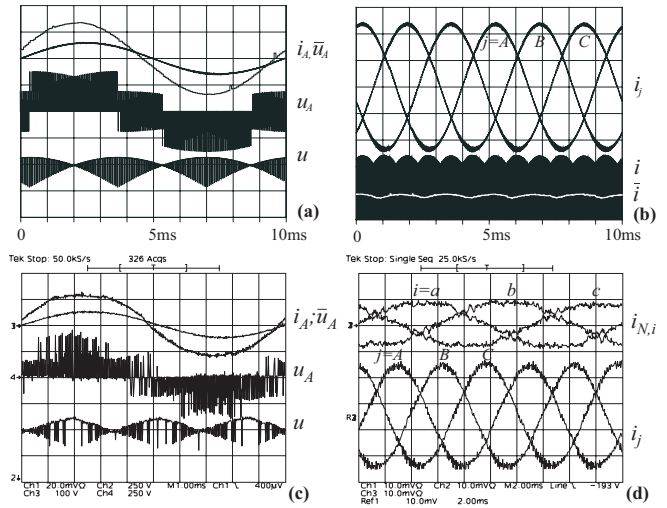

Fig.32: Digital simulation **(a)**, **(b)** and experimental verification **(c)**,**(d)** of the operating behavior of a SMC. Operating condition: $U_{1,l\text{-}l}$=400V$_{rms}$, f_1=50Hz, U_2= 95V, f_2=100Hz, P=2kW, switching frequency f_P=15.6kHz, ohmic mains behavior, phase displacement of output current and output voltage fundamental $\Phi_2\approx$0.

According to **Fig.33** [13] for a full thermal utilization of the power semiconductors (junction temperature T_j=120°C for a heat sink temperature of T_H=75°C, $U_{1,l\text{-}l}$=400V$_{rms}$) of a 10kW SMC realized in 1200V IGBT technology and a switching frequency of f_P=20kHz a very high overall efficiency of $\eta\approx$95% could be achieved (operating conditions: formation of the maximum output voltage $U_{2,l\text{-}l}$= √3/2 $U_{1,l\text{-}l}$, modulation according to Fig.30(a),

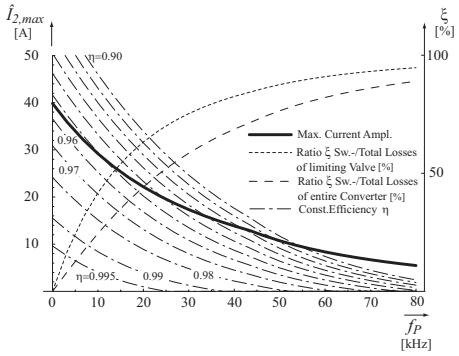

Fig.33: Maximum admissible output current amplitude of a SMC realized in IGBT technology in dependency on the pulse frequency. Modulation as shown in Fig.30(a). Furthermore shown: efficiency η and ratio ξ of switching and total losses. For details see [13].

feeding of a permanent magnet synchronous machine, i.e. phase displacement of output current and output voltage fundamental $\Phi_2 \approx 0$).

In the course of further research a realization of the SMC in SiC-technology has to be considered which does allow operation at high ambient temperature as present, e.g., for the motor-integrated converter systems and facilitates switching frequencies in the range of f_P=100..200kHz minimizing the input filter volume. However, the matrix converter concept basically might replace conventional DC link inverter drives in future only in areas where motor and inverter are developed by a single manufacturer for specific applications.

5. Conclusions

For the realization of ultra-compact and/or high-frequency and high efficiency three-phase PWM converter system besides

- novel circuit topologies and modulation and control schemes as discussed in this paper,
- novel low-inductance interconnection technologies,
- novel concepts of magnetic and electromagnetic components, and
- novel concepts for packaging and cooling

have to be developed. There, electromagnetic and thermal simulation will be of increasing importance for the converter design. Furthermore, digital simulation will be employed more and more also in parallel with the experimental analysis of converter systems as for highly integrated realizations currents and voltages in general could not be acquired directly. This fact also should be considered by the development of novel indirect measurement techniques, e.g. for determining the current in a conductor and/or power semiconductor from a near-field measurement.

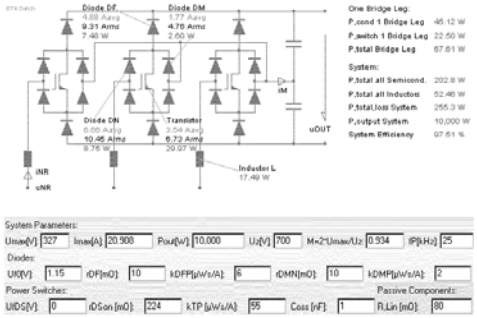

Fig.34: Interactive Power Electronics Seminar (*iPES)* on fundamentals of power electronics. *iPES* is under further development at the ETH Zurich and is available at no costs at www.ipes.ethz.ch

Besides technological aspects the education of future engineers is of paramount importance for ensuring a further continuous and dynamic development of the field. There, in order to achieve a high efficiency of the learning process new media and information technology, e.g. in the form of interactive web-based simulation (cf. **Fig.34**) should be employed. Furthermore, digital simulation

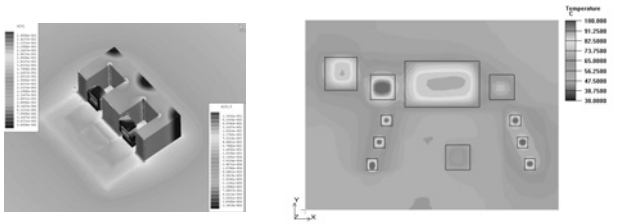

Fig.35: Electromagnetic simulation of the magnetic core of a series /parallel resonant converter and thermal simulation of a multi-chip power module as performed by students in the 4th semester on electrical engineering at the ETH Zurich.

should not be used only for circuit- and control-oriented simulation but also be used for showing the thermal and electromagnetic design of power electronic systems (cf. **Fig.35**).

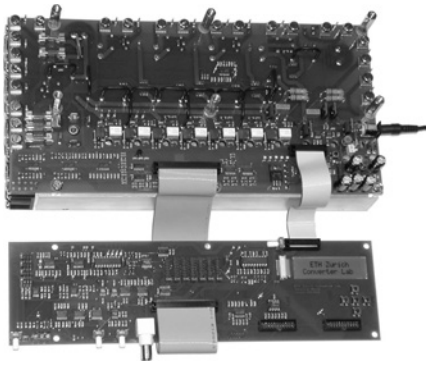

Fig.36: Highly versatile laboratory setup for teaching basics of power electronics developed at the ETH Zurich. The system does allow to analyze all basic single- and three-phase PWM AC/DC converters as well as isolated and non-isolated DC/DC converter topologies.

Finally, for the education of future engineers laboratory courses based on industry related hardware (cf. **Fig.36**) are a strict requirement. Such courses should clearly show all parasitic effects which might occur in industrial systems and should point out the importance of a practical verification of all theoretical results in the field of power electronics.

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