Novel Modulation Schemes Minimizing the Switching Losses of Sparse Matrix Converters

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Abstract. The switching losses of a three-phase *Sparse Matrix Converter* (SMC) operating in the lower modulation range are minimized by employing the lowest and the second largest input line-to-line voltage for the formation of the converter DC link voltage. The resulting current stresses on the power semiconductors and the switching frequency ripple RMS values of the filter capacitor voltages and output currents are calculated by digital simulation and compared to conventional modulation. Finally, a modulation scheme is introduced which allows the generation of reactive input power also for missing active power transfer via the DC link and/or purely reactive load. This is a basic requirement for operating the SMC in boost mode where the output filter capacitor voltages have to be controlled sinusoidally also for no-load operation.

1 Introduction

Sparse Matrix Converter (SMC, cf. **Fig.1**) systems [1] are functionally equivalent to Conventional Matrix Converters (CMC) but are characterized by a lower realization effort and a lower control complexity and are therefore especially interesting for an industrial application.

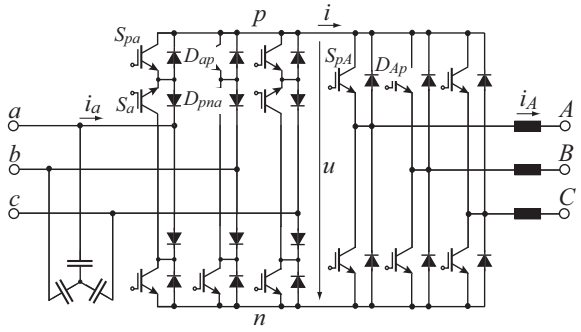

Fig.1: Topology of the Sparse Matrix Converter (SMC) according to [1].

Within each pulse half period two line-to-line voltages are switched into the DC link of the SMC by proper control of the input stage (cf. **Fig.2**). There, the input stage commutation is at zero current (cf. *i* in Fig.2, Fig.6 in [1], [2]) what allows to avoid a multi-step commutation scheme in dependency on the sign of the commutating voltage or commutating current as required for the CMC and/or results in low switching losses and high converter reliability.

For employing the largest and the second largest positive line-to-line voltage for the formation of the DC link voltage a maximum output voltage range is achieved, however, relatively large switching losses of the output stage do occur. The basic properties of this modulation scheme, which will be denoted as ***modulation scheme I*** in the following are shown in Fig.2. For low output voltage amplitude therefore a modification of the modulation scheme has to be considered which reduces the output stage switching losses by switching line-to-line input voltages of low instantaneous value into the DC link.

In this paper a novel SMC modulation scheme is proposed (denoted as modulation scheme II) where within each pulse half period subsequently the lowest positive and the second largest input line-to-line are switched into the DC link. In combination with the clamping of the SMC output stage bridge legs within π/3-wide interval in the vicinity of the maxima of the corresponding output phase currents this results in minimum system switching losses. In **Section 2** the relative on-times of the input and output stage switching states are calculated and a concept for shifting part of the output stage switching losses to the input stage is described.

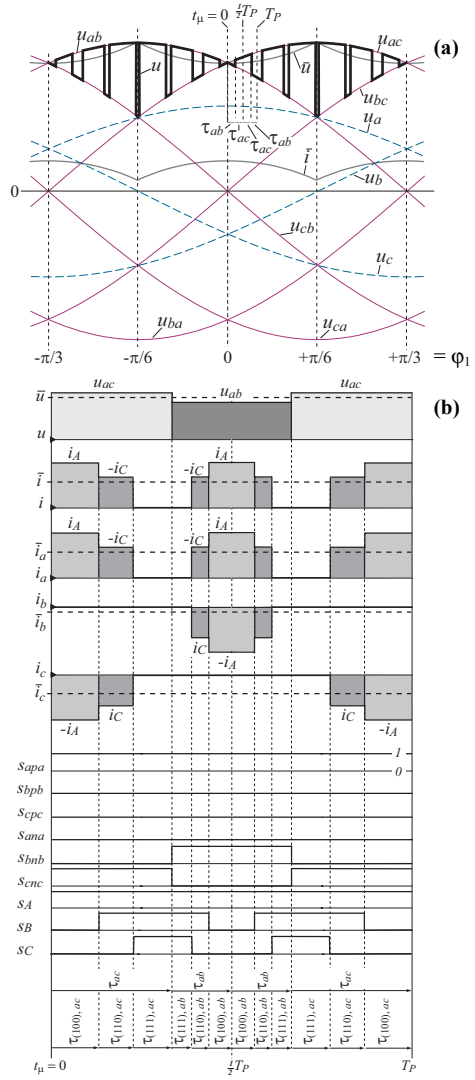

Fig.2: Modulation Scheme I (cf. Fig.9 in [1]); **(a)** time behavior of the mains phase voltages, the mains line-to-line voltages, the SMC DC link voltage *u* and of the local average value of the DC link voltage and the DC link current, $\bar{u}$ and $\bar{\imath}$, within a 2π/3-wide interval of the input period (φ_1=−π/3…+ π/3); **(b)** time behavior of *u*, *i*, the mains phase currents i_i, *i*=*a*,*b*,*c*, within a pulse period t_μ=0…T_P for φ_1 in 0…+π/6 and φ_2 in 0…+π/3 (φ_2 denotes the phase of the reference value of the output voltage space vector, cf. Eq.(14)); furthermore shown: switching functions of the rectifier and the inverter stage (s_{apa}=1 indicates a bidirectional connection of phase input *a* and the positive DC link bus *p*, and/or the turn-on state of S_a and S_{pa}; s_A=1 denotes the turn-on state of S_{pA} and/or the turn-off state of S_{nA}). For the sake of clarity a low pulse frequency is assumed and the ripple components of *u* and *i* are neglected.

In **Section 3** the modulation schemes I and II are comparatively evaluated based on the current stresses on the power semiconductors and the RMS values of the ripple components of the filter capacitor voltages and output currents. Finally, in **Section 4** a modification of modulation scheme I is proposed which allows the generation of reactive power at the converter input also for purely reactive load, i.e. without transfer of active power via the DC link.

2 Minimizing Switching Losses at Low Output Voltage

As shown in Fig.2 the commutation of the input stage is within the free-wheeling interval of the output stage, i.e. at zero DC link current i=0. Therefore, switching losses do occur only for the output stage and are determined by the instantaneous value of the DC link current i and the DC link voltage u.

The DC link current i is directly defined by the output current phase displacement Φ_2 for a given φ_2. Therefore, the only possibility for minimizing the switching losses is to employ sections of the input line-to-line voltage with minimum instantaneous value for the formation of the DC link voltage.

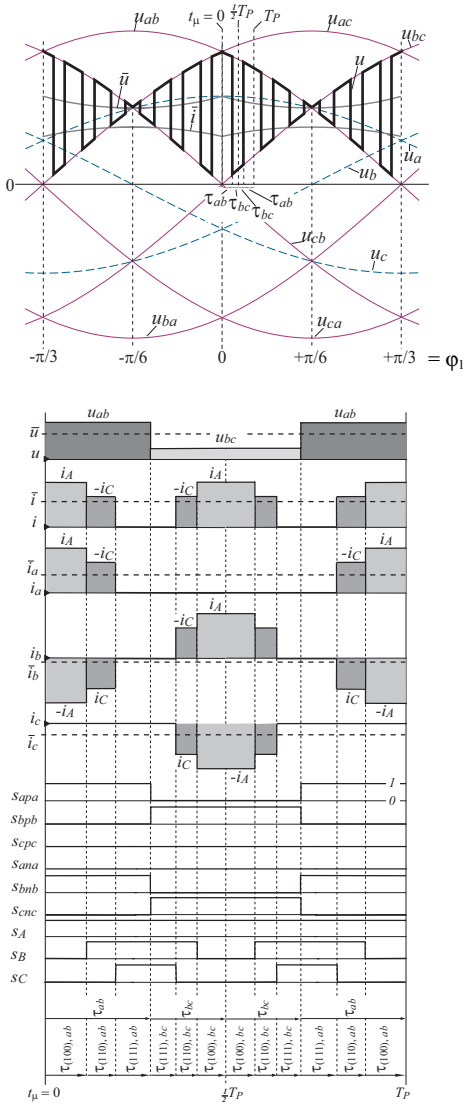

Fig.3: Proposed modulation scheme (modulation scheme II); representation of the voltages, currents and switching functions as for modulation scheme I in Fig.2. In contrast to modulation scheme I the input stage bridge leg *a* is switching with pulse frequency between the positive and negative DC link bus. As the commutation of the input stage is at zero DC link current this however does not result in switching losses.

There, the combination of the input phases has to be selected such that the distribution of the DC link current i to the input phases results in phase currents being proportional to the corresponding phase voltages, i.e. $i_{a,b,c} \sim u_{a,b,c}$ (cf. Eq.(6)). The resulting modulation scheme which is denoted as ***modulation scheme II*** in the following is shown in **Fig.3**.

In analogy to Section IV in [1] the calculation of the relative on-times of the power transistors of the input stage can be limited to a π/6-wide interval, φ_1=0…π/6, of the mains period. Based on this the turn-on times for further intervals can be derived by symmetry considerations.

Assuming a constant local average value $\bar{\imath}$ of the DC link current i for each rectifier switching state of a pulse half period (time intervals τ_{ab} and τ_{bc}, cf. Eq.(24) in [1]) we have for the local average values of the input phase currents

$$\bar{i}_a = d_{ab}\,\bar{i} \qquad \bar{i}_b = (d_{bc} - d_{ab})\,\bar{i} \qquad \bar{i}_c = -d_{bc}\,\bar{i}\ . \tag{1}$$

Under consideration of

$$d_{ab} + d_{bc} = 1 \tag{2}$$

Eq.(1) can be rewritten as

$$\bar{i}_b = (1 - 2d_{ab})\,\bar{i} \tag{3}$$

and/or

$$d_{ab} = \frac{\bar{i}_a}{\bar{i}_b + 2\cdot\bar{i}_a} \quad . \tag{4}$$

For ohmic fundamental mains behavior of the SMC input stage,

$$\phi_1 = 0° \quad , \tag{5}$$

and/or

$$\bar{i}_a \sim u_a \qquad \bar{i}_b \sim u_b \qquad \bar{i}_c \sim u_c \tag{6}$$

Eq.(4) results in

$$d_{ab} = \frac{u_a}{u_b + 2u_a} = \frac{u_a}{u_{ac}} \tag{7}$$

where a symmetric sinusoidal input phase voltage system

$$\begin{aligned} u_a &= \hat{U}_1 \cos(\omega_1 t) \\ u_b &= \hat{U}_1 \cos(\omega_1 t - 2\pi/3)\ . \\ u_c &= \hat{U}_1 \cos(\omega_1 t + 2\pi/3) \end{aligned} \tag{8}$$

is assumed. Furthermore, Eqs.(1), (2) and (6) yield

$$d_{bc} = \frac{-\bar{i}_c}{\bar{i}_b + 2\cdot\bar{i}_a} = -\frac{u_c}{u_{ac}}\ . \tag{9}$$

The time-dependent local average value of the DC link voltage (cf. Fig.3) now results as

$$\bar{u} = d_{ab}\,u_{ab} + d_{bc}\,u_{bc} = \frac{3}{2}\frac{\hat{U}_1^{\,2}}{u_{ac}} = \frac{\sqrt{3}}{2}\hat{U}_1\frac{1}{\cos(\omega_1 t - \frac{\pi}{6})}\ . \tag{10}$$

With reference to Eq.(10) the modulation limit, i.e. the maximum value of the amplitude of the output phase voltage fundamental is

$$\hat{U}_{2,\max,II} = \frac{1}{\sqrt{3}}\,\overline{u}_{\min} = \frac{1}{\sqrt{3}}\,\overline{u}\,|_{\varphi 1=\pi/6} = \frac{1}{2}\hat{U}_1 \tag{11}$$

and/or in comparison to modulation scheme I

$$\hat{U}_{2,\max,II} = \frac{1}{\sqrt{3}}\hat{U}_{2,\max,I} \approx 0.58\,\hat{U}_{2,\max,I} \quad . \tag{12}$$

Due to the time dependency of $\bar{u}$ the formation of a constant amplitude $\hat{U}_2$ of the output phase voltages requires a variation of the SMC output stage modulation index

$$m_2 = \frac{\hat{U}_2}{\frac{1}{2}\overline{u}} = \frac{4}{\sqrt{3}}\frac{\hat{U}_2}{\hat{U}_1}\cos(\omega_1 t - \pi/6)\ . \qquad (13)$$

There, we have for the absolute turn-on times of the active switching states

$$\begin{aligned}
\tau_{(100),ab} &= \frac{T_p}{\sqrt{3}}\frac{\hat{U}_2}{\hat{U}_1^{\,2}}u_a\cos(\varphi_2+\tfrac{\pi}{6})\\
\tau_{(110),ab} &= \frac{T_p}{\sqrt{3}}\frac{\hat{U}_2}{\hat{U}_1^{\,2}}u_a\sin(\varphi_2)\\
\tau_{(110),bc} &= \frac{T_p}{\sqrt{3}}\frac{\hat{U}_2}{\hat{U}_1^{\,2}}(-u_c)\sin(\varphi_2)\\
\tau_{(100),bc} &= \frac{T_p}{\sqrt{3}}\frac{\hat{U}_2}{\hat{U}_1^{\,2}}(-u_c)\cos(\varphi_2+\tfrac{\pi}{6})
\end{aligned} \qquad (14)$$

where φ_2 denotes the phase of the output voltage space vector $\underline{u_2}^*$ ($|\underline{u_2}^*|=\hat{U}_2$, cf. Fig.10 in [1]) which has to be formed in the average over a pulse half period (for Eq.(14) φ_2=0…π/3 and φ_1=0… π/6 is assumed).

In the following the voltage transfer ratio of the SMC shall be characterized using

$$M_{12} = \frac{\hat{U}_2}{\hat{U}_{2,\max,I}} = \frac{\hat{U}_2}{\frac{\sqrt{3}}{2}\hat{U}_1}\ . \qquad (15)$$

Besides the DC link voltage the switched current takes direct influence on the output stage switching losses. Therefore, according to [3] an output stage bridge leg is advantageously not switched in the vicinity of the maxima of the related phase current; the phase output then remains clamped to the positive and/or negative DC link bus within a π/3-wide interval of the positive and the negative output half period. For Φ_2=0 a symmetric clamping around the maximum of the output phase voltage fundamental (cf. **Fig.4**(b) and (c)) results in minimum switching losses. For increasing current phase displacement Φ_2 the clamping interval has to be shifted accordingly, but has to remain within an angle interval of ±π/3 relative to the phase voltage maximum. Therefore, for $|\Phi_2|>\pi/6$ higher output switching losses as for Φ_2=0 will occur (cf. Figs.5(c),(d) and (g),(h)). For an optimal positioning of the clamping interval the time behavior of the phase current *and* (contrary to inverter systems with constant DC link voltage as considered in [3]) the time dependency of the envelopes of the input line-to-line voltages which are employed in each pulse half period for DC link voltage formation would have to be considered.

Remark: For changing the input stage switching state within the free-wheeling interval of the output stage (cf. Fig.2(b) and Fig.3(b)) for modulation scheme I and II switching losses are limited to the output stage. A partitioning of the switching losses between input and output stage is possible for positive DC link current $i>0$. There, by turning off an input stage power transistor, e.g. S_{bnb} in **Fig.5**, the output stage is forced from an active switching state into (passive) free-wheeling operation and the turn-off losses are taken over by S_{bnb}. At the end of the free-wheeling interval the subsequent line-to-line input voltage is applied to the DC link by turning on S_{cnc} (cf. Fig.5) and the output stage returns into the prior active switching state where again no output stage switching losses do occur. A detailed description of this control concept will be given in a future paper.

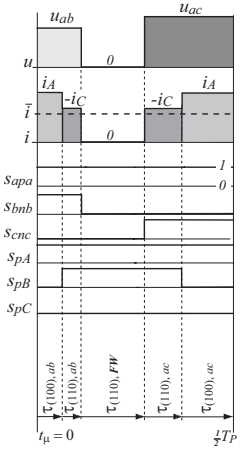

Fig.5: Commutation of the SMC output stage into a passive free-wheeling state (free-wheeling action despite the active switching state control signals remain applied to the output stage power transistors) by turning off a power transistor (S_{bnb}) of the input stage for positive DC link current $i>0$. For conventional modulation (cf. Fig.2), the commutation of the input stage is at zero current and/or switching losses only do occur for the output stage.

3 Comparative Evaluation of Modulation Schemes I and II

The results of a simulation of the stationary operating behavior of a SMC employing the proposed modulation scheme II are compiled in **Fig.6** for

mains frequency	f_1=50Hz	
output frequency	f_2=100Hz	
switching frequency	f_P=25kHz	
load inductance	L=1mH	
input filter capacitance	C=9µF	(star connection).

In order to determine the switching frequency ripple of the filter capacitor voltages independent of the inner mains impedance

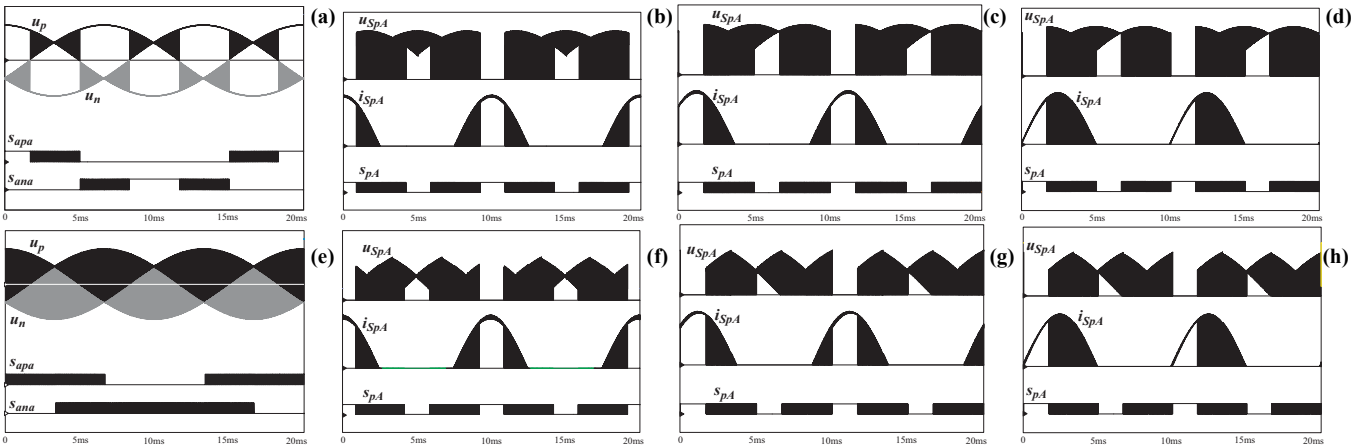

Fig.4: Modulation of the SMC input and output stage for modulation scheme I (cf. **(a)-(d)**) and modulation scheme II (cf. **(e)-(h)**) for different values of the output current phase displacement Φ_2=0 (b),(f); Φ_2=π/4 (c),(g); Φ_2= π/2 (d),(h). Representation of the potential of the positive and negative DC link bus, u_p and u_n, with reference to the mains star point (cf. (a) and (e)) and of the switching functions s_{apa} and s_{ana} (cf. Fig.2 and Fig.3) of input stage bridge leg *a*; furthermore shown: voltage, current and switching function of power transistor S_{pA} of the SMC output stage. The positioning of the clamping intervals of S_{pA} is under consideration of a minimization of the transistor switching losses.

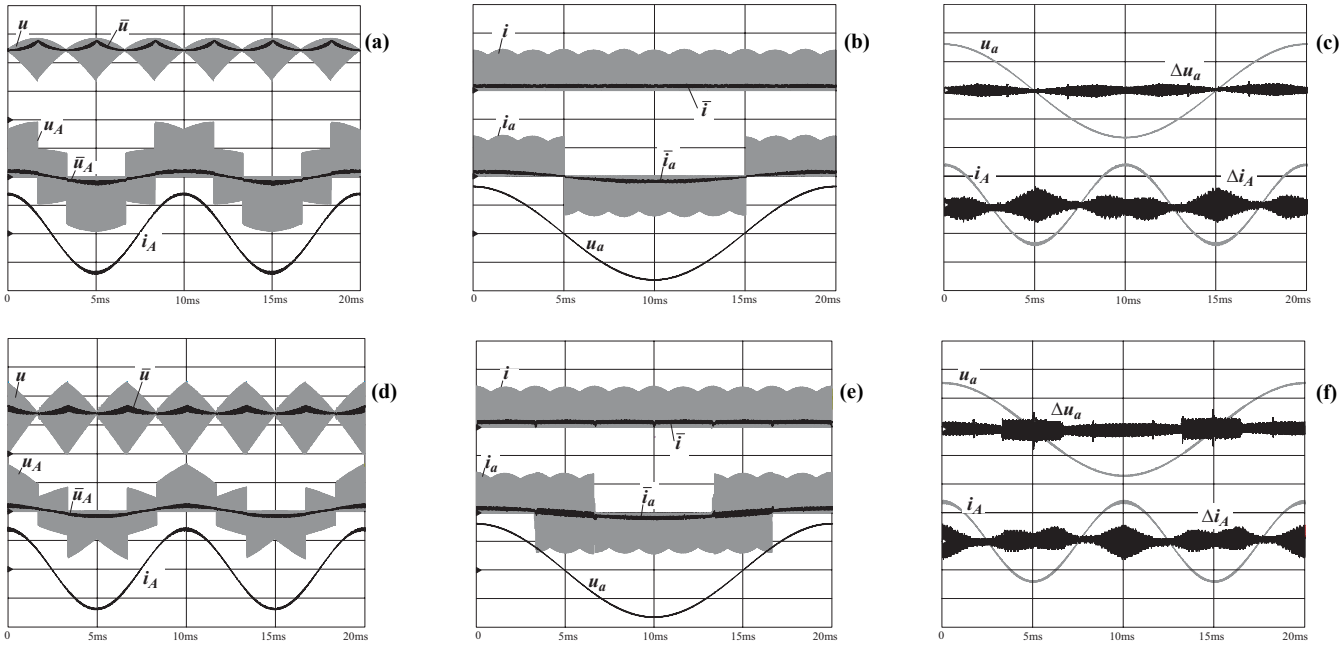

Fig.6: Simulation of the SMC operating behavior for modulation scheme I (cf. (a)-(c)) and modualtion scheme II (cf. (d)-(f)); **(a), (d)** DC link voltage u, local average value $\bar{u}$, output phase voltage u_A (with reference to the inductive load star point), local average value $\bar{u}_A$, output phase current i_A; **(b), (e)** DC link current i, local average value $\bar{i}$, input phase current i_a, local average value $\bar{i}_a$, input phase voltage u_a; **(c), (f)** input phase voltage u_a, ripple component Δu_a, and output phase current i_A and ripple component Δi_A; scales: 200V/div, 15A/div (Δu_a: 20V/div, Δi_A: 1.5A/div); M_{12}=0.1, Φ_2=0.

and/or the dimensioning of an input filter the system is fed by a purely sinusoidal current. There, the current phase displacement and amplitude is adjusted such that a filter capacitor voltage fundamental amplitude of $\hat{U}_1$= 327V (equivalent to $U_{1,RMS}$= 230V) is achieved. Furthermore, a load voltage is impressed at the output side which ensures a load current fundamental amplitude of $\hat{I}_2$=17.75A independent of the selected current phase displacement Φ_2; for M_{12}=1 and Φ_2=0 this is equivalent to P_O=7.5kW. The clamping intervals of the output stage bridge legs are shifted with increasing output current phase displacement Φ_2 as shown in Fig.5 in order to always achieve a maximum reduction of the output stage switching losses.

As shown in Figs.6(a),(b) and **Fig.7** the proposed modulation scheme II reduces the average DC link voltage and therefore the output stage switching losses by a factor of about two as compared to modulation scheme I.

However, for the formation of an output voltage of equal amplitude $\hat{U}_2$ a higher modulation index of the output stage is required as for modulation scheme I. This results in a larger width of the sections of the output currents forming the DC link current and/or in higher conduction losses of the input stage (cf. **Fig.8** and **Fig.9**) and in a higher ripple Δu_1 of the input filter capacitor voltages and/or a higher RMS value $I_{C,RMS}$ of the filter capacitor current (cf. Fig.6(f) and **Fig.10**(a) and **Fig.11**(a)). Furthermore, $\Delta U_{1,RMS}$ and $I_{C,RMS}$ are increased by the occurrence of current pulses of equal magnitude but opposite sign in the vicinity of the input current zero crossings (cf. i_b in Fig.3(b) und i_a in Fig.6(e)).
As shown in Figs.6(c) and (f) and Fig.10(b), modulation schemes I and II result in an approximately equal RMS value $\Delta I_{2,RMS}$ of the output current ripple for given voltage transfer ratio M_{12}. This is again caused by the larger on-time of the active switching states of the output stage and/or by the larger width of the output voltage pulses of modulation scheme II which lead to an equal change of the output phase currents as the voltage pulses of smaller width but higher amplitude occurring for modulation scheme I.

An advantage of modulation scheme II over scheme I is the lower value of the switched voltage which results in a lower amplitude of the common mode component of the output voltage and/or in lower conducted electromagnetic emissions of the converter system (Fig.11(b)).

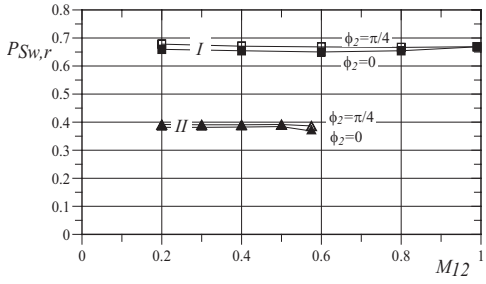

Fig.7: Normalized switching losses $P_{Sw,r}$ of a transistor of the output stage (e.g. of S_{pA}). Assuming a linear dependency of the transistor switching losses on the switched voltage and current, for determining $P_{Sw,r}$ the sum of the transistor voltage and current products at the turn-on and turn-off instants is calculated over the least common multiple T_m of the mains and output period, $\Sigma_{Tm} i_{SpA} u_{SpA}/(4/3\hat{U}_1\hat{I}_2 T_m/T_P)$. The normalization to $4/3\hat{U}_1\hat{I}_2 T_m/T_P$ (T_P=1/f_P) results in a quantity being independent of the absolute value of the switched voltage and current and the considered time period. The factor 4/3 considers that there are in total 8 switching actions of the output stage and/or 8/6 switching actions of a single output stage power transistor within a pulse period T_P.

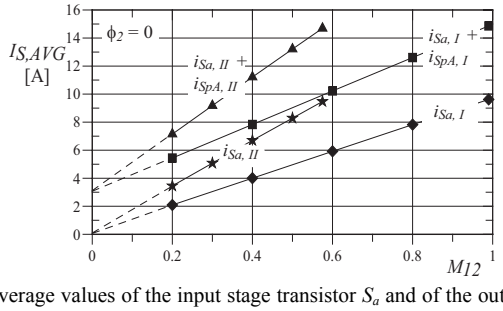

Fig.8: Average values of the input stage transistor S_a and of the output stage transistor S_{pA} in dependency on the voltage transfer ratio M_{12} (cf. Eq.(15)) for Φ_2=0. S_{pa} does not conduct current for Φ_2=0 and shows only a very low current average value for Φ_2=π/4 (cf. Fig.17 in [1]), therefore, i_{Spa} is not shown. Index *I* refers to modulation scheme I, index *II* to modulation scheme II. Simulation parameters as for Fig.6, but f_2=50Hz. Increasing M_{12} results in an increasing width of the output current sections forming the DC link current and therefore in a linear increase of the input stage transistor current average value. Increasing Φ_2 results in lower instantaneous DC link current values and accordingly in lower input stage conduction losses.

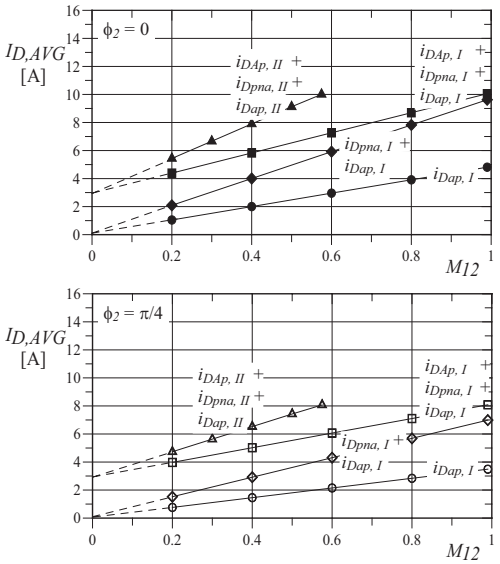

Fig:9: Average values of the power diode currents of the input stage (diodes D_{ap} and D_{pna}) and of the output stage (diode D_{Ap}) in dependency on the voltage transfer ratio M_{12} (cf. Eq.(15)) for Φ_2=0 and Φ_2=π/4. For details of the representation and an explanation of the characteristic of the dependency on M_{12} see caption of Fig.8.

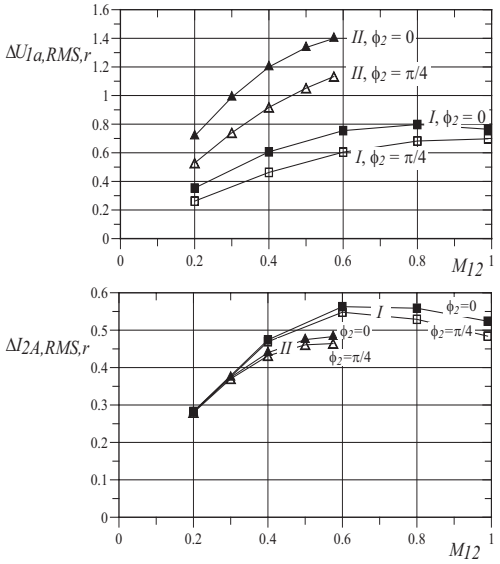

Fig.10: Normalized RMS value of the input filter capacitor voltage ripple and of the output current ripple, $\Delta U_{1a,RMS,r}$ and $\Delta I_{2A,RMS,r}$, for Φ_2=0 and Φ_2=π/4. normalization with reference to $\hat{U}_1 T_P/(8L)$ (cf. [3]) and/or $\hat{I}_2 T_P/(8C)$. For details of the representation see caption of Fig.8.

As a closer analysis shows, the characteristics shown in Figs.7-11 which have been calculated assuming f_1/f_2=1 are also valid in good approximation for a wide variation of the ratio f_1/f_2 of the input and output frequency. This is proven by **Fig.12** e.g. for $I_{Sa,AVG}$, $\Delta U_{1a,RMS,r}$ and $\Delta I_{2A,RMS,r}$.

4 Conclusions

For achieving a low volume of the filter components a matrix converter has to be operated at high switching frequency. Therefore, the switching losses are in general constituting a large share of the total converter losses.

The modulation scheme II proposed in this paper allows to cut the switching losses of a SMC operating in the lower modulation range in half as compared to conventional modulation I for equal RMS value of the output current ripple. The converter conduction losses are only slightly increased. Accordingly, the thermal stress on the power semiconductors is considerably reduced what permits an increase of the output current at low output frequency and/or of the torque of an AC drive at low speed. As a disadvantage a higher ripple of the input filter capacitor voltages has to be accepted.

Alternatively, the reduction of the switching losses can be utilized for an increase of the switching frequency. This allows to maintain

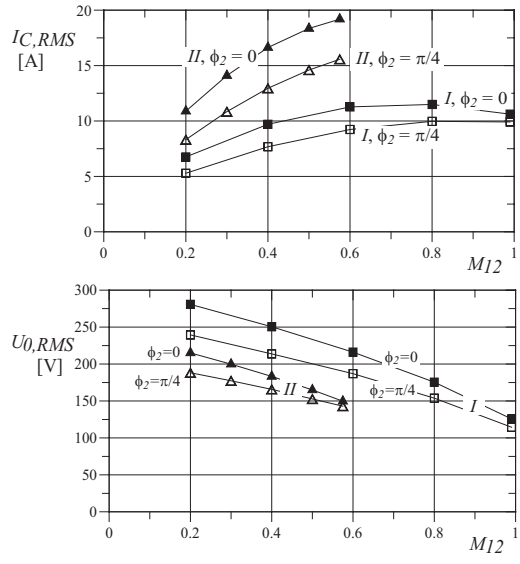

Fig.11: RMS values $I_{C,RMS,r}$ and $U_{0,RMS,r}$ of the filter capacitor current and of the common-mode component of the SMC output voltage in dependency on the voltage transfer ratio M_{12}.

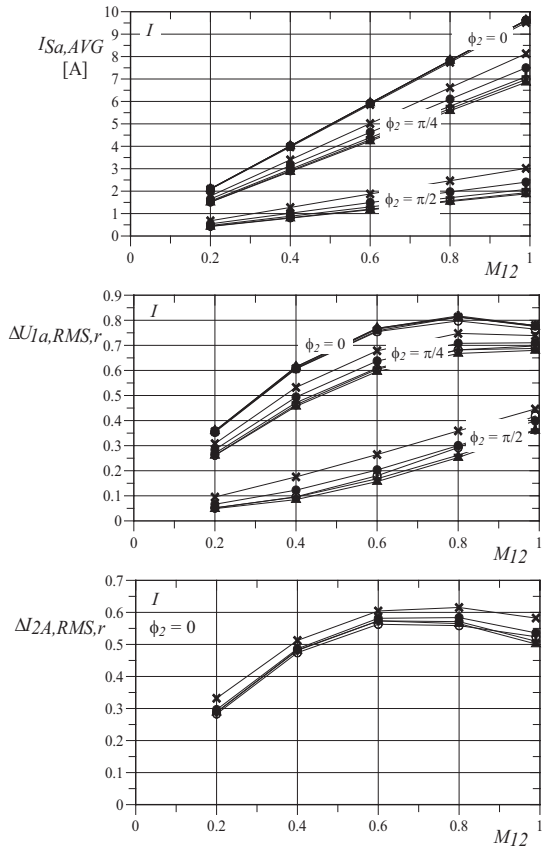

Fig.12: Dependency of input stage transistor current average value $I_{Sa,AVG,r}$, of the normalized RMS value of the input filter capacitor voltage ripple $\Delta U_{1a,RMS,r}$ and of the normalized RMS value of the output current ripple $\Delta I_{2A,RMS,r}$ on M_{12} for different values of the output frequency f_2; ✕: f_2 = 500Hz, ●: f_2 = 250Hz, ✚: f_2 = 100Hz, ○: f_2 = 50Hz, ▲: f_2 = 5Hz; f_1=50Hz, modulation scheme I, normalization as for Figs.8 and 10; remaining parameters as for Fig.8. The integration required for the calculation of the average and RMS values is performed over the least common multiple of the input and output periods T_1=1/f_1 and T_2=1/f_2.

a filter capacitor voltage ripple given for conventional modulation I and features a reduction of the RMS value of the output current ripple by a factor of two.

In a next step the proposed modulation scheme II will be experimentally verified for a 7.5kW prototype of the SMC. There it is important to consider that a large ripple of the filter capacitor voltages results in passive free-wheeling operation in the vicinity of $u \approx 0$ which causes a distortion of the output voltage formation. Therefore, a compensation scheme based on output voltage measurement has to be employed or the modulation has to be changed over to modulation scheme I in order to ensure a high output current quality.

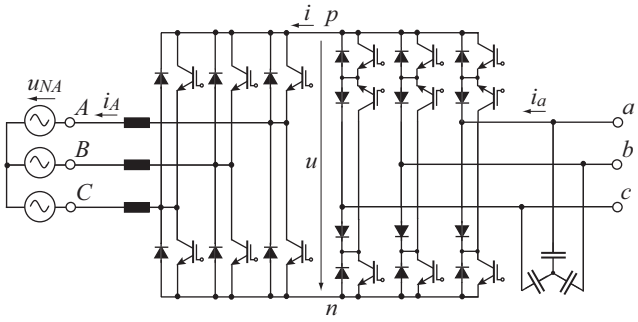

Fig.13: Operation of a SMC in boost mode. The definition of the positive voltage and current directions is assumed equal as for buck-mode operation in Fig.1.

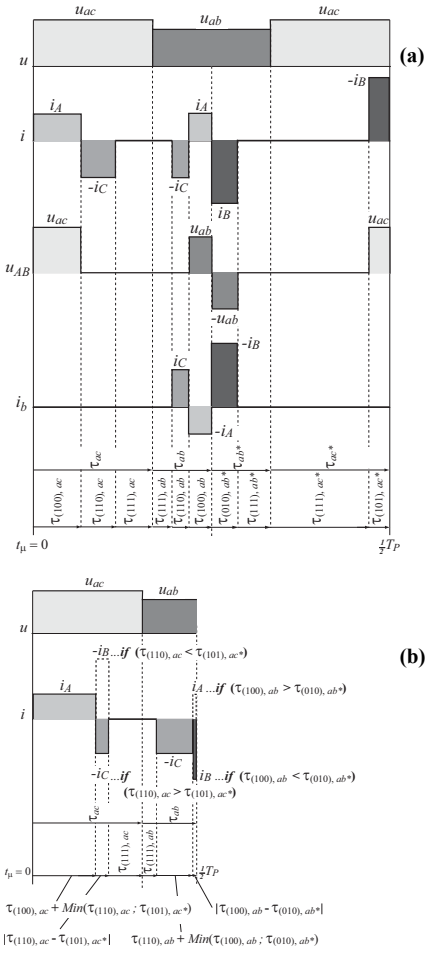

Fig.14: Proposed modulation scheme **(a)** for generating reactive output current (filter capacitor current, cf. Fig.13) for zero active power transfer via the DC link; the switching state sequence of a pulse period T_P (cf. (a)) can be combined in a half pulse period as shown in **(b)**.

In the course of future research also the operation of the SMC in boost mode (cf. **Fig.13**) which has not been treated in the literature so far will be analyzed in detail. There, the main subject is the generation of purely reactive output power at no load, i.e. without active power flow via the DC link ($\Phi_1 = \pm\pi/2$ *and* $\Phi_2 = \pm\pi/2$). This is not possible for modulation scheme I or II (cf. Section V-B in [1]) as the DC link current shows zero local average value within each turn-on interval of a line-to-line input voltage for $\Phi_2 = \pm\pi/2$; Accordingly, no local average value of the filter capacitor current can be formed.

The modification of the modulation concept required for purely reactive power operation is shown in **Fig.14**(b) at the example of modulation scheme I. There, the first half of a pulse half period, $t_\mu = 0 \ldots T_P/2$, is utilized for voltage formation (as given for conventional modulation). Within the second half of the pulse period the filter capacitor currents (e.g. i_b) are formed, where the switching state turn-on times (e.g. $\tau_{(010),ab}^*$ and $\tau_{(101),ac}^*$) are determined such that no local average value of the DC link power $p = u.i$ does result. There, the DC link current in general shows a local average value (cf. **Fig.15**). The maximum value of the reactive output current available for purely reactive power operation ($\Phi_1 = \pm\pi/2$ *and* $\Phi_2 = \pm\pi/2$) which, e.g. could be utilized for a sinusoidal control of the output filter capacitor voltages at no (active) load is shown in **Fig.16**. A detailed discussion and experimental verification of the novel control concept will be given in a paper to be published in near future.

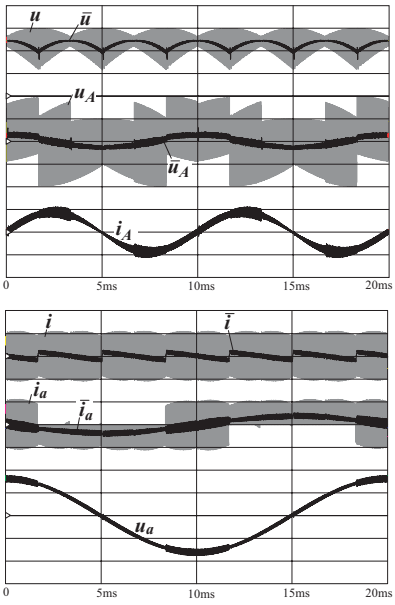

Fig.15: Digital simulation of the operating behavior of the SMC in boost mode for $\Phi_1 = -\pi/2$ *and* $\Phi_2 = +\pi/2$; modulation as shown in Fig.14, parameters as given in Section 3; scales: 200V/div, 20A/div.

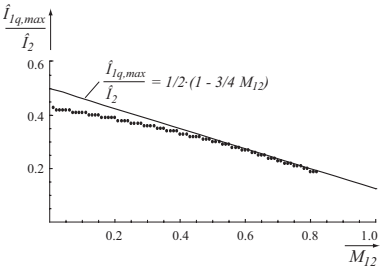

Fig.16: Dependency of the normalized maximum fundamental amplitude of the reactive output phase current, $\hat{I}_{1q,max,r}$, on the voltage transfer ratio M_{12} in case no active power is transferred via the DC link; modulation as shown in Fig.14.

References

[1] **Kolar, J.W., Baumann, M., Schafmeister, F., and Ertl, H.:** *Novel Three-Phase AC-DC-AC Sparse Matrix Converter*, *Part I and II.* Proceedings of the 17th Annual IEEE Applied Power Electronics Conference, Dallas (Texas), USA, March 10 - 14, Vol. 2, pp. 777 - 791 (2002).

[2] **Wei, L., and Lipo, T.A.:** A Novel Matrix Converter Topology with Simple Commutation. Record of the IEEE Industry Applications Society Annual Meeting, Chicago, Sept. 30 – Oct. 4, Vol. 3, pp. 1749-1754 (2001).

[3] **Kolar, J.W., Ertl, H., and Zach, F.C.:** Influence of the Modulation Method on the Conduction and Switching Losses of a PWM Converter System. IEEE Transactions on Industry Applications, Vol. 27, No. 6, pp. 1063-1075 (1991).