PWM Converter Power Density Barriers

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***Abstract* — Power density of power electronic converters in different applications has roughly doubled every 10 years since 1970. Behind this trajectory was the continuous advancement of power semiconductor device technology allowing an increase of converter switching frequencies by a factor of 10 every decade. However, today's cooling concepts, and passive components and wire bond interconnection technologies could be major barriers for a continuation of this trend.**

For identifying and quantifying such technological barriers this paper investigates the volume of the cooling system and of the main passive components for the basic forms of power electronics energy conversion in dependency of the switching frequency and determines switching frequencies minimizing the total volume. The analysis is for 5 kW rated output power, high performance air cooling, advanced power semiconductors, and single systems in all cases. A power density limit of 28 kW/dm^3@300 kHz is calculated for an isolated DC-DC converter considering only transformer, output inductor and heat sink volume. For single-phase AC-DC conversion a general limit of 35 kW/dm^3 results from the DC link capacitor required for buffering the power fluctuating with twice the mains frequency. For a three-phase unity power factor PWM rectifier the limit is 45 kW/dm^3@810 kHz just taking into account EMI filter and cooling system. For the sparse matrix converter the limiting components are the input EMI filter and the common mode output inductor; the power density limit is 71 kW/dm^3@50 kHz when not considering the cooling system.

The calculated power density limits highlight the major importance of broadening the scope of research in power electronics from traditional areas like converter topologies, and modulation and control concepts to cooling systems, high frequency electromagnetics, interconnection technology, multi-functional integration, packaging and multi-domain modeling and simulation to ensure further advancement of the field along the power density trajectory.

***Index Terms* — Figures of Merit, Power density, Cooling system, Passive components.**

I. INTRODUCTION

The continual development of power electronic converters, for a range of applications, is characterized by the requirements for higher efficiency, lower volume, lower weight and lower production costs (cf. Fig. 1). A high efficiency is usually demanded at the nominal operating point, and in particular for redundant systems also at partial loads [1], to ensure a good utilization of the energy resources and a low operating cost. Furthermore, low losses are basic requirement to enable a compact realization, which also allows a flexible deployment of the converter system.

The requirement for a reduced converter volume is driven, particularly, by the information technology applications, where the rapid progress of integrated circuit technology had lead to more compact systems with a higher power consumption [2]. Furthermore, a small volume requirement provides greater design freedom and a lower capital outlay in the building infrastructure [3]. Also, power electronic converters are increasingly becoming embedded in the final application. This allows a reduction in the installation cost and an improvement in electromagnetic compatibility. When fully integrated within the load, the converter's volume is strongly limited by the main dimensions of the load system. Examples of such application are the variable speed drives that are used in a range of the industrial systems and consumer white-goods, as well as the low power level, point-of-load converters and voltage regulator modules (VRM) [4].

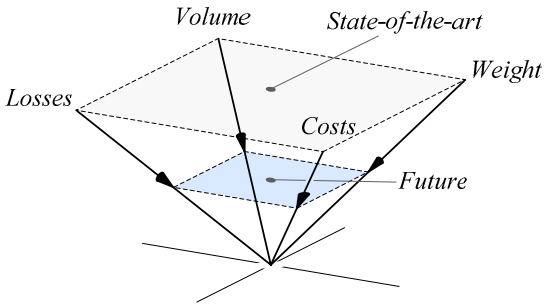


Fig. 1. Development trends in power electronic converters.

A low converter weight typically means that a reduced amount of material is used and for stationary power supplies allows for simple installation, handling and maintenance, which is particularly important for mobile systems, apart from low volume requirement. Modern examples are found in hybrid vehicles [5] and More Electric aircraft [6].

For comparing the technological status and performance of power electronic converters over a wider power range and with other disciplines, Figures of Merit (FOM) are defined by relating the converter volume, weight, cost and power loss to the output power [7]:

- Power Density, P_O/V, [kW/dm^3]
- Specific Power; P_O/G, [kW/kg]
- Relative Costs, $P_O/\$$, [kW/$]
- Relative Losses, P_V/P_O, [%].

(where P_O and P_V denominate the output power and the power losses, and V, G, and $ are the converter volume, weight and costs). The relative loss FOM provides a better measure of the technological advancement for high efficiency systems than just efficiency ($\eta \approx 1\text{-}P_V/P_O$) since an improvement of the efficiency from 95% to 96% appears as a relatively small increase, however it requires a reduction of the losses by around 20%.

To understand what is required for future power electronic developments, the FOM are typically used in application specific road-maps (e.g. US Freedom Car initiative [7] and Technology Reports of the Power Supplies Manufacturer Association (PSMA) [8]). There, power density is most frequently utilized to represent and evaluate the progress of the technology. This is equivalent to the microelectronic industry where the shrinking of the poly-silicon gate's feature size and/or the doubling of the transistor density every 18 (24) month (Moore's Law) is used as a measure of progress.

The trend has been for a large increase in the power density and the dynamic technological development of the power electronic converters over the last few decades covers the complete cross section of applications and converter types. This trend is shown in a diagram by Ohashi [9,10] and is summarized in Fig. 2, where the trend line for industrial systems is differentiated from research only systems (typically, a period of 10 years is needed for the full introduction of a new concept into industry). In [10], a power density of 50 kW/dm^3 was emphasized by a special point (see Fig. 2) and indicated by Takahashi as the future power density (time frame > 20 years) of inverters utilizing SiC power semiconductors [11].

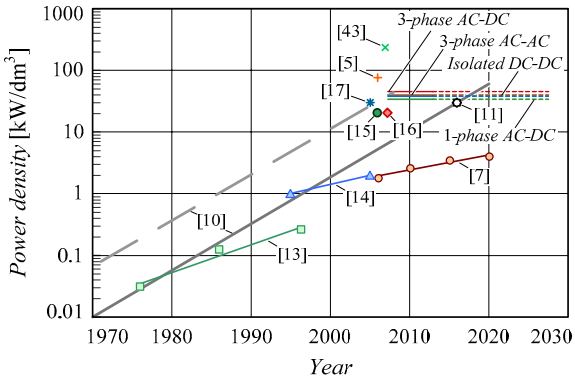


Fig. 2. Power Density Trend of commercial products and research systems [10] and Power Density Barriers as identified in this paper. Without progress in power passives and interconnection technology the barriers would result in the saturation (S-curve shape) of the future power density development of single systems; a further improvement then would have to come from splitting into partial interleaved systems.

The power density of 1 to 2 kW/dm^3, shown in Fig. 2 for the year 2000, has been confirmed by a study by the European Center of Power Electronics (ECPE) for industrial AC drive PWM inverters [12]. However in the literature, for individual applications, a less forward reaching development is described. As an example, [13] shows that for switching power supplies there was an increase in the power density of embedded converters from 0.5W/in^3 (30 W/dm^3) in 1976 to 2W/in^3 in 1986 and it predicts a 4W/in^3 (244 W/dm^3) power density for 1996. Similarly, [14] shows a doubling of the power density of industrial power converters between 1994 and 2004. For automotive converters, [7] states that an increase in power density from the present value of 5 kW/dm^3 to 10 kW/dm^3 is required by 2020. This demands a doubling of the power density over the next 10 years.

These particular values have already been exceeded by converter systems that are used in hybrid vehicles which are available on today's market (e.g. the power control unit of the Toyota RX400, which is constructed from two inverters and a DC-DC converter without isolation). Furthermore, in concept studies for water-cooled motor-integrated inverters for hybrid vehicles (without EMI filter), power densities of 75 kVA/dm^3 are shown [5]. Water-cooled, non-isolated, high frequency DC-DC converters presently achieve 25 kW/dm^3 [15] (in this case it includes a single-stage EMI filter). For a water-cooled, unity power factor, three-phase AC/DC converter, a power density of 20 kW/dm^3 (including a Class B EMI filter) is predicted in [16]. Furthermore, an air-cooled DC-DC is shown in [17] that reaches a power density of 30 kW/dm^3 without an EMI filter.

Accordingly, for the main industrial power electronic applications, a doubling of the power density can be expected in the future. A doubling of power density typically requires an increase in the switching frequency by a factor of approximately 10. This increase in switching frequency can be achieved by using a higher switching frequency in an individual system or, more favorably, by the phase-shifted operation of parallel converters. It is interesting to note that also within the field of microelectronics that there is a long-term trend for IC chips to increase their internal clock frequencies by about a factor 10 each decade (see ITRS Roadmap, Fig. 1(b) in [3]).

An important point to note for the power densities indicated so far is the overall system is frequently not considered and the essential elements, such as the cooling system, EMI filter, filter capacitors, housings and terminals are omitted from the power density calculation. Often, e.g., for power supply modules only the module volume is considered and not the volume needed to transfer the heat to the environment (by air flow or a heat sink) [18]. The same applies to systems with water cooling, where the pump and heat exchanger exhibit a relatively high space requirement [19]. The water effectively only represents a transportation medium, like a heatpipe, but finally the heat must be dissipated by conventional radiators to the environment. Therefore, the published high power density figures are only a localized figure and are not representative for the final system power density.

In summary, a clear overall view of the actual attainable power densities for various converter types, based on today's technology, is missing. However, only the understanding of technological barriers could initiate technological improvements and ensure a further development of the converters along the trend lines shown in Fig. 2.

A power electronic converter is formed from the following main elements:

- Power Semiconductor Modules
- Modulation and Control Circuit / Auxiliaries
- *Power Passives (Filter Components/Transformers)*
- *Cooling System*
- Interconnection / Packaging

The power density, ρ, is defined by the division of the power output by the total volume, where the total volume, excluding custom component shapes and the use of multi-functional subsystems (e.g. for electrical connection, thermal conduction paths or guiding of magnetic fields [20,21]), is typically a factor of two more than the sum of the partial volumes $\sum Vol_i$ [12]

$$\rho = \frac{P_O}{Vol} < \frac{P_O}{\sum Vol_i} . \qquad (1)$$

The cooling system and the EMI filter exert, in general, a substantial influence on the total volume [22, 16]. An increase in the power density is therefore possible, in principle, with an increase of switching frequency or an increase in the operating temperature of the power semiconductors (Fig. 3).

An increase in switching frequency leads, however, to an increase in the switching losses of the power semiconductors and results in a larger heat sink volume. In [23], the losses are defined as intrinsic, i.e. caused by the structure of the power semiconductors and extrinsic, i.e. caused by the outside interconnections and the limits of Si and SiC power semiconductor devices when operated with hard switching are derived. A reduction in the relative switching loss increase with the frequency can be achieved by utilizing soft switching. The switching frequency increase then can be, to a large extent, used to decrease the size of the inductive components and thus to decrease the converter's total volume.

The increase in frequency results in a smaller relative magnetic flux magnitude in the magnet core of a transformer, and this means that the core area can be reduced. However, there is an increase in the skin and proximity losses (which is partly compensated by the lower turn length caused by the smaller core area) with the frequency increase, which finally leads to a thermal limit since a minimum volume is reached in which no more energy can be dissipated from the surface area. Furthermore, there is not a continuous decrease in the volume of the EMI filter with increasing switching frequency (see Sect.IV.D & E, Figs. 29 & 30).

A decrease of the heat sink volume can be achieved by increasing the power device's junction temperature, however, this is limited by the maximum permissible operating temperature of the Si power semiconductors (175…200°C). Furthermore, a reduced operating temperature is usually set by the thermal stability of the most economical packaging materials and by the reduced life span caused by the increased temperature range during temperature cycling. Alternatively, the cooling effort can be reduced for a given junction temperature

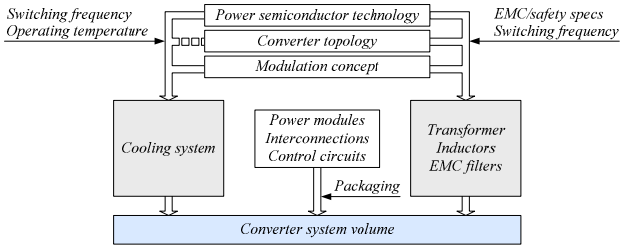


Fig. 3. Dependency of converter volume on the operating parameters.

by decreasing the thermal resistance between the junction and the case using, for example, double-sided cooling of the power semiconductors [24].

So far the increase in the power density has been achieved by a substantial increase in the switching frequency. This has been supported by decreasing the on-resistance of power MOSFETs through Super-Junction structures which made unipolar power transistors, with extremely small switching losses, applicable to higher power level converters.

New SiC or GaN wide band-gap power semiconductors, with substantially higher critical field strength limits compared to Si, will in the future make the realization of unipolar power semiconductors with small on-resistances possible for devices with several kV blocking voltages possible (starting from approx. 4kV a transition to bipolar devices is more favorable). For the main industrial applications for power electronics, this provides the possibility in the future of extremely low switching losses and a relatively free ability to optimize the passive components over several decades of the switching frequency. Furthermore, since these new semiconductors have higher maximum operating junction temperatures, this will lead to a drastically reduced cooling effort. This is possible because the new power semiconductors have a higher thermal conductivity and small layer thicknesses [25], however depends on developments of appropriate packaging materials and soldering techniques.

The availability of power semiconductors with high operating temperatures and extreme switching speeds (where their use will require appropriate planar connection techniques [26] and control circuits [27]) will therefore move the passive components into the foreground since they will become the power density limiting components.

This paper analyzes the way the volume of the main passive components and of the cooling system of converters changes (assuming optimum selection of the converter and filter topology) for changing switching frequency and determines the resulting power density limits $\rho_{lim,i}$

$$\rho < \rho_{\mathrm{lim},i} = \frac{P_O}{Vol_i} \cdot \tag{2}$$

There, a wide range of applications, i.e., the fundamental types of power electronic energy conversion are considered separately and the volumes of the respective main passive components (indicated in the parentheses) are minimized by properly selecting the operating frequency

- Isolated DC-DC Converter
  (Transformer and Output Inductors)
- Single-phase unity power factor AC-DC converter
  (Output Capacitors)
- Three-Phase AC-DC Converter
  (EMI Filter and Input Inductors)
- Three-Phase AC-AC Indirect Matrix Converter
  (EMI Filter und Common-Mode Output Inductors)
- Three-Phase Back-to-Back AC-AC Converter
  (DC link capacitor).

where, with reference to [11], the resulting power density of the matrix converters is of particular interest.

The considerations are, in each case, for an individual system with a power rating of 5 kW in order to ensure validity of the results in the power range of 1 to 10 kW. The possibility for a switching loss neutral increase of the effective operating frequency using the parallel connection of multiple phase-shifted converters or a minimization of the total volume of the converter systems [28] is not considered for reasons of brevity and is the subject of a future publication.

In order to relate the findings to today's semiconductor technology, in selected cases the cooling effort required for the today's best available semiconductor combinations is considered besides the main passive components. From this a maximum power density results at an optimal operating frequency

$$\rho < \rho_{\mathrm{lim},12} = \frac{P_O}{Vol_1 + Vol_2} = \frac{\rho_1 \cdot \rho_2}{\rho_1 + \rho_2} \cdot \tag{3}$$

(where Vol_1 denominates the volume of the main passive components and Vol_2 is the heat sink volume) that clearly identifies today's technological limits and provides a basis for road-mapping activities in the field (ECPE [29], CPES [30], AIST [31]).

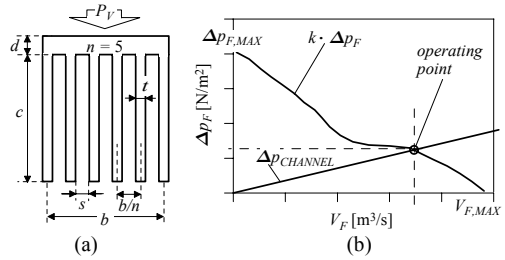
In order to guarantee a minimum heat sink volume and/or high power density in **section II** the choice of fin geometry of the heat sink is adapted in the most optimal way so that the highest thermal energy removal is achieved per unit volume. In such a way, a maximum cooling ability for each unit volume of the cooling system is determined. This cooling ability then is used with all types of converter systems to compute the power density limit $\rho_{lim,12}$. In **sections III** to **V** the basic types of power electronic converters are analyzed, and at the end of each section a short evaluation of the results is given to clarify each case.

This paper concludes with a discussion on the measures needed to increase the power density based on existing technologies. A future looking view is given on the further investigations required for peak power density, specific power and efficiency as well as highlighting the requirement for multi-domain modeling and simulation tools in order to enable the development of highly compact power converters.

II. Thermal Management

A. Heat Sink Optimization for Forced Convection

In order to optimize a heat sink employing forced convection, one has to consider the thermal resistance of the heat sink material, the thermal resistance due to convection, and the temperature increase of the air flowing through the heat sink channels. The following optimization is based on a typical heat sink geometry shown in Fig. 4, where the heat generating power devices are placed on a base plate and a number of fins extending out from the opposite side of the base plate.



(a) (b)

Fig. 4. (a) Geometry of the heat sink with thermal losses P_V [W] covering the area $A_{CHIP} = b \cdot L$, where L is the heat sink length in air flow direction. (b) Fan characteristic showing fan pressure being dependent on the air flow V_F. In order to consider pressure losses at the channel inlet, Δp_F is multiplied with the fin spacing ratio $k = s/(b/n)$ [19].

Generally, the fin geometry provides a pressure drop $\Delta p_{CHANNEL}$ for the air flow through the channels. The air flow is driven by a fan that is characterized by a pressure-flow curve (Fig. 4(b)). The operating point defines the air flow that, based on the fin geometry, is laminar or turbulent. Based on flow and air properties, the convective heat transfer from the fin surface into the air in the channels can be calculated. All these relations can be described employing analytical and empirical equations [32][19], which allows a systematic optimization of the fin geometry for a given fan. Following the detailed procedure described in [19], the total thermal resistance of the heat sink (from heat sink surface to ambient air at the fan inlet) is

$$R_{th,S-a}^{(HS)} = R^*_{th,FIN} + R_{th,conv} + R_{th,\Delta T} \tag{4}$$

with the conductive heat flow through the fins being

$$R^*_{th,FIN} \approx \frac{1}{2\lambda_{HS} L} \cdot \left(1 - 10^{-3} \frac{V_{F,MAX}}{\Delta p_{F,MAX}} \frac{L}{s^2 c^2} \right)^{-1}, \tag{5}$$

the convective heat flow from fin surface into air being

$$R_{th,conv} \approx \left(1.3 \cdot 10^4 \frac{\Delta p_{F,MAX}}{V_{F,MAX}} \frac{s^4}{L^2} \right) \left(1 + 2 \cdot 10^3 \sqrt{\Delta p_{F,MAX}} \cdot \frac{s^2}{L} \right)^{-1}, \tag{6}$$

and a contribution due to the temperature rise of the air heating up along the channel from inlet to outlet given by

$$R_{th,\Delta T} \approx \frac{7.5 \cdot 10^{-4}}{V_{F,MAX}} \cdot \tag{7}$$

Generally, the maximum air flow rate $V_{F,MAX}$, pressure $\Delta p_{F,MAX}$ and power consumption P_{FAN} are all dependent on the fan's rotating speed n [rpm] and diameter D [m] as described in [33] as

$$V_{F,MAX} \left[m^3/s \right] = k_1 \cdot n \cdot D^3 \tag{8}$$

$$\Delta p_{F,MAX} \left[N/m^2 \right] = k_2 \cdot n^2 \cdot D^2 \tag{9}$$

$$P_{FAN} \left[W \right] = k_3 \cdot n^3 \cdot D^5 . \tag{10}$$

Investigating the datasheets of 65 commercially available fans with a wide variations of their geometries [34], we calculated the parameters of (8)-(10) to be within the ranges $k_1 = [6 \cdot 10^{-3} \,..\, 13.5 \cdot 10^{-3}]$, $k_2 = [3.94 \cdot 10^{-4} \,..\, 8.85 \cdot 10^{-4}]$ and $k_3 = [3 \cdot 10^{-6} \,..\, 76.5 \cdot 10^{-6}]$.

For comparison of different heat sink designs concerning power density, we calculate the "cooling system performance index (CSPI)" [19] (see also "volumetric thermal conductivity" [35]) as

$$CSPI \left[\frac{W}{K \cdot dm^3} \right] = \frac{1}{R_{th,S-a}^{(HS)} \left[\frac{K}{W} \right] \cdot Vol_{CS} \left[dm^3 \right]} \tag{11}$$

which can be expressed independently from a specific fan by employing (8)-(10)

$$CSPI^{-1} = R_{th,S-a}^{(HS)} \cdot Vol_{CS} = \frac{\frac{c^2}{2\lambda_{HS}} \left(1 + \frac{c^2}{3 A_{CHIP}} \right)}{1 - \frac{A_1 \cdot A_{CHIP}}{s^2 \cdot \sqrt[3]{\frac{1}{k_3} \cdot P_{FAN}^{\max}} \cdot c^{1/3}}} + \frac{A_3 \cdot \left(1 + \frac{c^2}{3 A_{CHIP}} \right) s^2}{1 + \frac{A_2 \cdot A_{CHIP}}{s^2 \cdot \sqrt[3]{\frac{1}{k_3} \cdot P_{FAN}^{\max}} \cdot c^{1/3}}} + \frac{A_4 \cdot \left(A_{CHIP} + \frac{1}{3} c^2 \right)}{\sqrt[3]{\frac{1}{k_3} \cdot P_{FAN}^{\max}} \cdot c^{1/3}} \tag{12}$$

using the abbreviations $A_1 = 10^{-3} \cdot k_1 / k_2$, $A_2 = 5 \cdot 10^{-4} \cdot k_2^{-0.5}$, $A_3 = 6.5 \cdot k_2^{0.5} / k_1$ and $A_4 = 7.5 \cdot 10^{-4} \cdot k_1^{-1}$. Here, the fan speed n has been substituted by the maximum acceptable power consumption of the fan P_{FAN}^{max} employing (10). The "cooling system" volume Vol_{CS} in (11), (12) is defined as volume of heat sink plus volume of the fan.

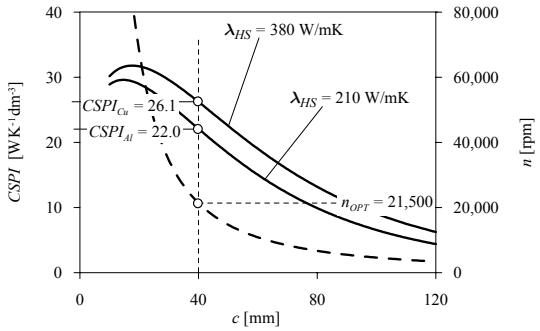


Fig. 5. Optimizing a cooling system employing (12) for heat sink materials aluminum and copper. For a typical 5kW-converter with 95% efficiency, we assume A_{CHIP}=32 cm^2 and $P_{FAN,MAX}$=20 W.

If the channel width s in (12) is set to values maximizing the CSPI, theoretically optimized curves can be plotted as shown in Fig. 5. With a fan diameter c=40mm (equal to fin length, see Fig. 4(a)), a theoretical maximum $CSPI_{Al}$ =22.0 W.K^{-1}.dm^{-3} can be achieved for an aluminum heat sink (with a thermal conductivity of 210 W/Km), and a maximum $CSPI_{Cu}$ =*26.1* W.K^{-1}.dm^{-3} for copper (380 W/Km). The required fan speed would be N_{OPT} = 21,500rpm for both materials. In case of c=20mm, the CSPI-values would be around *30*, but the required fan speed would be 60,000 rpm, significantly increasing noise and reliability problems.

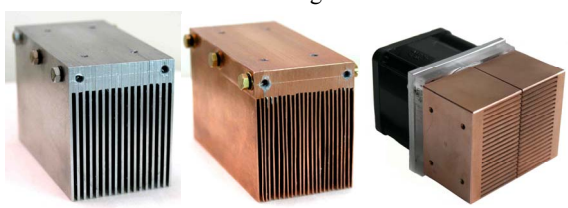
Experimental prototypes of optimized heat sinks for typical 5kW-converters are shown in Fig. 6. The heat sinks of Fig. 6(a) and (b) have been designed according to the theoretical optimum given in Fig. 5. Based on measured R_{th}-values, we obtained $CSPI_{Al}$=17.5 W.K^{-1}.dm^{-3} and $CSPI_{Cu}$=21.6 W.K^{-1}.dm^{-3}. Both CSPI-values are 20% below the theoretical optimum because of manufacturing constraints that do not allow to fully exploit the theoretical optimum [36], and due to employing a fan with n=15,500 rpm [34]. Fig. 6(c) shows a different heat sink design with two opposite base plates which better utilizes the heat flow through the fins. This results in a higher $CSPI$=30.9 W.K^{-1}.dm^{-3}. For a detailed discussion and a comparison with commercially available heat sinks of significantly lower performance, see [19][36].

B. Thermal Limits of the Converter Power Density

Generally, the power density of a converter is defined as

$$\rho_{SYS} = \frac{P_{O,SYS}}{Vol_{SYS}} = \frac{\eta_{SYS}}{1 - \eta_{SYS}} \frac{\Delta T_{MAX} / R_{th}}{Vol_{SYS}} \tag{13}$$

with converter output power $P_{O,SYS}$, converter volume Vol_{SYS}, converter efficiency η_{SYS}, maximum acceptable temperature difference between power semiconductors and ambient ΔT_{MAX}, and thermal resistance R_{th} defining the heat flow from the semiconductors to ambient. For a general discussion we assume



(a) (b) (c)

Fig. 6 . Optimized heat sinks for a SanAce 40x40x28mm/50dB fan [34] and with A_{CHIP}=32cm^2 (a) aluminum, n=16, s=1.5mm, t=1.0mm, b=c=40mm, d=10mm, L=80mm, $R_{th,S-a}$= 0.26K/W; (b) copper, n=23, s=1.3mm, t=0.5mm, b=c=40mm, d=10mm, L=80mm, $R_{th,S-a}$=0.21K/W; (c) copper, n=21, s=1.0mm, t=1.0mm, b=c=40mm, d=5mm, L=27mm, $R_{th,S-a}$= 0.27K/W.

in the following that the thermal resistance between semiconductors and heat sink surface is small compared to the thermal resistance associated with convection at the heat sink surface.

As shown in Fig. 7(a), the natural convection at the outer surface of a cube-shaped converter is proportional to the square of its base length. If forced convection is employed by realizing a part of the converter volume as heat sink plus fan, the effective cooling surface, and, therefore, heat transfer to ambient via forced convection, is proportional to the third order of the base length (Fig. 7(b)). Here, the fin number $n_{FIN} = a_{CUBE}/(s+t)$ is defined by fin thickness t and channel width s. Since the effective cooling surface for employing a heat sink is proportional to the volume, the previously defined 'Cooling System Performance Index' (CSPI), which can be interpreted as 'volumetric thermal conductivity', will be used in the following calculations.

The thermal resistance of natural convection at the surface of a cube-shaped (base length a_{CUBE}) converter is

$$R_{th,n,CUBE} = \left(n_{C,f} \; \alpha \; a_{CUBE}^2 \right)^{-1} \tag{14}$$

with heat transfer coefficient α *[W/m²K]* and number of cooled surfaces $n_{C,f}$. For forced convection, realized by a cooling system integrated in the converter, the according thermal resistance is

$$R_{th,f,CUBE} = \left(k_{CS} \; a_{CUBE}^3 \; 10^3 \; CSPI \right)^{-1}, \tag{15}$$

which can be directly derived from (11) with $k_{CS} = Vol_{CS}/Vol_{SYS}$ describing the volume share of the cooling system. The thermal resistance in (13) is

$$R_{th,CUBE} = R_{th,n,CUBE} \parallel R_{th,f,CUBE} \tag{16}$$

resulting in a general expression for the converter power density of a cube-shaped converter system as

$$d_{SYS,CUBE}\left[\frac{W}{m^3}\right] = \frac{\Delta T_{MAX,S-a}}{\eta_{SYS}^{-1} - 1}\left(n_{C,f} \; \alpha \; a_{CUBE}^{-1} + 10^3 \; CSPI \cdot k_{CS} \right) \tag{17}$$

with a maximum acceptable sink to ambient temperature difference of $\Delta T_{MAX,S-a}$. As shown in Fig. 8, in case of dominating forced convection, the converter power density d_f is, in approximation, independent from the absolute converter size, while in case of pure natural convection d_n decreases inversely proportional to the base length.

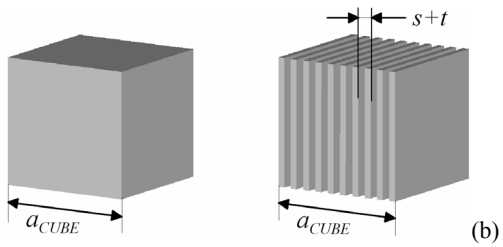


Fig. 7. (a) Surface area of the cube employing natural convection is proportional to the square of the length $A_{conv} \sim a_{CUBE}^2$. (b) 'Internal' surface area consisting of fins is proportional to the third order of the length $A_{conv} \sim a_{CUBE}^2 \cdot a_{CUBE}/(s+t) \sim a_{CUBE}^3$.

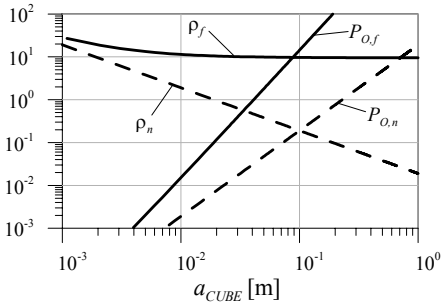


Fig. 8. Converter power density and output power dependent on absolute size of a cube-shaped converter for dominating forced convection (index *f*, solid line) and pure natural convection (index *n*, dashed line). Parameters are η =0.95, $\Delta T_{MAX,S-a}$ =50°C, $n_{C,f}$ =*1*, α =20 W/m²K, *CSPI*= 20 W.K⁻¹.dm⁻³, k_{CS} =0.5.

In case of pure natural convection, small systems will always show higher power densities than large systems. Assembling one large converter from many small sub-converters does not change this fundamental relationship between absolute size and power density because additional outer surface will be needed for cooling all of the internal sub-converters.

How much should the efficiency of a converter be increased if the desired output power is to be increased, but the convective cooling system, converter volume and maximum temperature remain unchanged? Based on (13) and (17), the converter efficiency can be written as

$$\eta_{SYS} = \eta_{SYS}(P_{OUT,SYS}) = \left(1 + \frac{c_X}{P_{OUT,SYS}} \right)^{-1}, \tag{18}$$

with

$$c_X = \alpha \; \Delta T_{MAX} \; a_{CUBE}^2 + 10^3 \, CSPI \cdot a_{CUBE}^3 \tag{19}$$

representing different qualities of the employed cooling system. Fig. 9 shows results for different parameter values $c_{X,(i)}$.

For two shapes representing naturally cooled converters with equal efficiency, equal maximum temperature and equal volume, the ratio of power densities follows as

$$d_{SYS}/d_{SYS,CUBE} = \left(1 + 2\,k\right) \Big/ \left(3\,k^{2/3}\right) \tag{20}$$

under the assumption that all six surfaces are equally cooled by convection. In (20), one shape is a cube, and the deviation of the second shape (base length a, height h) from the cube is characterized by $k = h/a$. As shown in Fig. 10, a cube represents the worst shape in terms of maximum power density if all six surfaces are cooled equally (solid line). Assuming only one single side is cooled by convection, this gives the ratio as

$$d_{SYS}/d_{SYS,CUBE} = k^{(-2/3)} \tag{21}$$

which is shown as dashed line in Fig. 10. In this case, which is more realistic for many converter designs than the assumption of all six sides equally being cooled, there is no local minimum. The more plate-like the shape is, the higher the theoretically possible power density will be.

C. Power Semiconductors

The power density of a cooling system can be written as

$$\rho_{CS} = \frac{P_{O,SYS}}{Vol_{CS}} = \frac{\eta_{SYS}}{1-\eta_{SYS}} \Delta T_{MAX} \cdot CSPI \;\; \cdot \tag{22}$$

Therefore, besides optimization of the CSPI, a further increase in the power density can be achieved by increasing the maximum acceptable junction temperature. Especially when

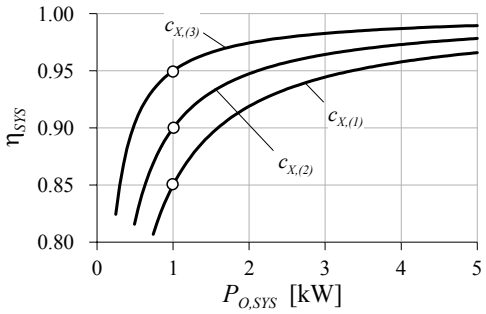


Fig. 9. In case of a given cube-shaped system volume and a given cooling system, the converter efficiency has to be increased in order to increase the possible output power.

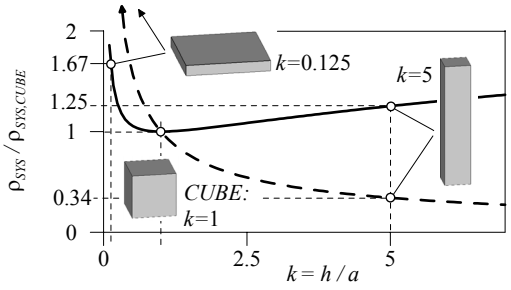


Fig. 10. Simple thermal model of converter systems with different shapes but with equal volume employing pure natural cooling at their surface. Solid line: All surfaces are equally cooled ($n_{CS} = 6$). Dashed line: One surface (square-shaped, length a) is cooled ($n_{CS} = 1$).

employing SiC, which allows junction temperatures well above 150°C, this effect can be exploited [19]. If, at a given ambient temperature $T_{ambient}$ = 45°C, the maximum junction temperature can be raised from 125°C to 175°C by replacing Si-semiconductors with SiC, the power density d_{CS} will rise by a factor 1.625.

Increasing the chip size of a power semiconductor will not only reduce the conduction losses in case of a MOSFET, but another effect, valid for all semiconductors, is the reduction of the thermal resistance from junction to sink since the $R_{th,J\text{-}S}$ is inversely proportional to the chip size.

Assuming equal losses $P_{V,T} = P_{V,D} = 0.5\,P_{V,SYS}$ of diode and transistor in Fig. 11, and furthermore setting $R_{th,J\text{-}S} = R_{th,T,J\text{-}S} = R_{th,D,J\text{-}S}$, the cooling system volume becomes

$$Vol_{CS} = \frac{1}{CSPI}\left(\frac{T_{J,MAX} - T_{ambient}}{P_{OUT,SYS}\left(\eta_{SYS}^{-1} - 1\right)} - \tfrac{1}{2} R_{th,J-S}\right)^{-1} \qquad (23)$$

with $T_{J,MAX}$ as the maximum acceptable value for the junction temperatures $T_{J,T}$ and $T_{J,D}$. This fundamental dependency of Vol_{CS} on $R_{th,J\text{-}S}$ is shown graphically in Fig. 12 for two different junction temperatures. As long as $R_{th,J\text{-}S}$ is not too small compared to $R_{th,S\text{-}a}^{(HS)}$, the cooling system volume can be significantly reduced by reducing the thermal resistance of the semiconductors. This can be simply achieved by employing a number of power semiconductors in parallel. If the thermal resistance of the semiconductors reaches a critical value $R_{th,J\text{-}S,MAX}$, it becomes impossible to operate the system within the given thermal parameters. Fig. 12 shows that increasing the junction temperatures is very effective in reducing the cooling system volume and, therefore, in increasing the power density.

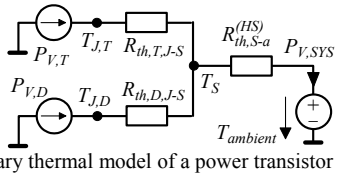


Fig. 11. Stationary thermal model of a power transistor (losses $P_{V,T}$) and a diode (losses $P_{V,D}$) mounted onto the heat sink with temperature T_S. The heat sink employing convection is fully represented by $R_{th,S\text{-}a}^{(HS)}$.

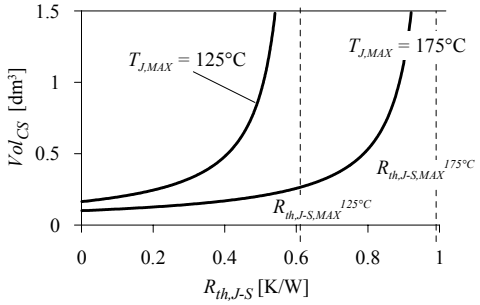


Fig. 12. Graphical representation of (23) assuming the thermal equivalent circuit shown in Fig. 11 with the parameters η_{SYS} =0.95, T_a=45°C, $CSPI$= 20 W.K^{-1}.dm^{-3}, $P_{O,SYS}$ =5 kW.

The choice of the thermal resistance values $R_{th,S\text{-}a}^{(HS)}$ and $R_{th,J\text{-}S}$ define the heat sink temperature T_S. Based on (22), the cooling system volume can be written, with a dependency on the heat sink temperature, as

$$Vol_{CS}(T_S) = \frac{P_{OUT,SYS}\left(\eta_{SYS}^{-1} - 1\right)}{CSPI}\left(T_S - T_{ambient}\right)^{-1}, \qquad (24)$$

which is shown in Fig. 13 for two different values of the system output power. The closer the heat sink temperature is to the ambient, the larger heat sink volume is needed to keep the converter system within its thermal boundaries. With the heat sink temperature close to the maximum acceptable junction temperature, the volume can be minimized. As already discussed before, this can be achieved by minimizing $R_{th,J\text{-}S}$ (Fig. 12).

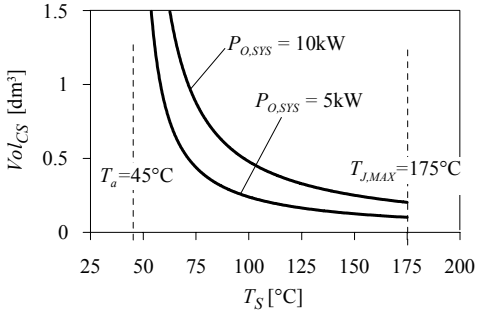


Fig. 13. Graphical representation of (24) with the parameters η_{SYS}=0.95, T_a=45°C, $T_{J,MAX}$=175°C, $CSPI$= 20 W.K^{-1}.dm^{-3}.

III. Magnetic Devices

The magnetic components, such as transformers and inductors, typically occupy a significant share of the converter volume. The volume of the magnetic components is of particular importance in isolated DC-DC converters. In this section the maximum power density of transformers and inductors used in DC-DC converter systems is determined. The considerations are based on a particular DC-DC converter (Fig. 14) used in telecom applications, where a high input voltage is stepped down to 48 V at a power level of 5 kW. The method for calculation of the power density is also valid, with a slight adaptation, for other converters. In the calculations, unless no other numbers are mentioned, the following specifications are assumed:

TABLE 1. SPECIFICATION OF THE CONSIDERED TELECOM SUPPLY.

Input Voltage	400 V (min. 380 V)
Transformer Primary Current	14.7A$_{peak}$
Output Voltage	48 V (max. 54 V)
Output Power	5 kW

First, the power density of the transformer for natural convection and forced air cooling are calculated. In the next step, the power density of the output inductors L_1 and L_2 is determined. Finally, the density which could be achieved by indirect air cooling is presented.

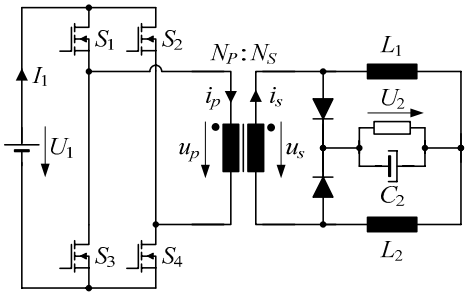


Fig. 14. 5 kW DC-DC converter used as the example to determine the magnetic components power density.

A. Transformer Power Density and Loss Model

The calculation of the transformer power density is based on a two-winding transformer with an nearly sinusoidal voltage U_P and current I_P in the primary and U_S and I_S at the secondary. The number of turns is represented by N_P and N_S and since a converter in the range of several kilowatts, with relatively high winding currents, is considered, it is assumed that only one turn per layer of the winding is realized. This could be either a foil winding or several parallel connected solid wires, which can be transformed in an equivalent foil winding [39].

The thickness of the foil (or diameter of the wires) significantly influences the skin- and proximity-effect losses in the winding. In order to minimize these losses, the optimal thickness must be calculated for each operating frequency, using, for example [39],

$$d_{Opt,v} = \frac{1}{\sqrt[4]{\frac{5N_v^2-1}{15}}} \cdot \frac{\sqrt{2}}{\sqrt{\omega \mu_0 \sigma}} \tag{25}$$

where N_v denotes the number of layers. With the thickness of the foils d_{Optv}, the copper fill factor k_{CU} and the thickness of the bobbin d_{bobbin}, the width of the winding window d (cf. Fig. 15)

$$d = \frac{1}{k_{CU}}\left(N_P d_{Opt,P} + N_S d_{opt,S}\right) + d_{bobbin} \tag{26}$$

and the volume of the winding $V_{Wdg} = b \cdot d \cdot l_W$ is calculated. By applying the optimal thickness of the layers, the AC losses, skin plus proximity-effect, are 4/3 times the DC losses. Thus, the overall winding losses can be calculated by

$$P_{Wdg} = \frac{N_P l_W}{\sigma b d_{Opt,P}} \frac{4}{3} I_P^2 + \frac{N_S l_W}{\sigma b d_{Opt,S}} \frac{4}{3} I_S^2 . \tag{27}$$

With the assumed sinusoidal voltages and currents, a sinusoidal flux density with a peak amplitude of

$$B_P = \frac{\sqrt{2} U_P}{N_P A_{Core} \omega} \tag{28}$$

results and the core losses in the different core sections can be simply calculated with the Steinmetz equation [40]

$$P_{Core} = C_m f^{\alpha} B_P^{\beta} V_{Core,v} . \tag{29}$$

where $V_{Core,v}$ is the volume of the considered section. The overall core volume is given by

$$V_{Core} = (b+a) \cdot c \cdot 2a + 2d \cdot a \cdot c . \tag{30}$$

In the case of a converter with a non-sinusoidal flux density the equations published in [41] should be applied.

From the core and winding losses, the temperature distribution in the transformer is calculated using a thermal model as shown in Fig. 16. It is assumed that the temperature within each layer is approximately uniform and that the heat flows from one layer to the next via the isolation represented by thermal resistance $R_{th,I}$. In the outer layer, the heat is dissipated to the ambient via $R_{th,W\text{-}A}$ and at the inner layer it flows via the bobbin ($R_{th,W\text{-}C}$) to the core. In the core the heat flows from the middle leg to the yokes where it is dissipated to the ambient via $R_{th,C\text{-}A}$. To simplify the calculations it is assumed that the winding losses are uniformly distributed within the winding, which is approximately true since the share of the proximity effect losses on the total losses is relatively small for an optimised layer thickness.

The hottest spots of the transformer are the inner layer of the winding and at the centre of the middle leg where the core is

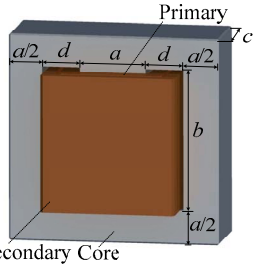


Fig. 15. Transformer (tube type) dimensions with primary and secondary windings.

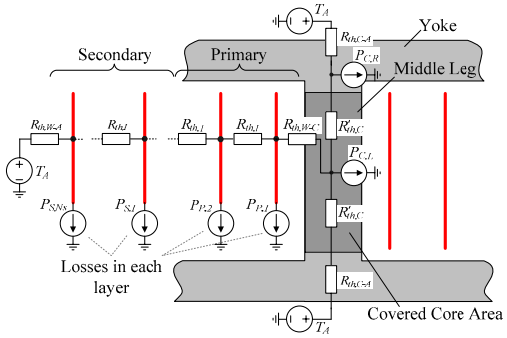


Fig. 16. Thermal equivalent circuit of the transformer with primary and secondary windings.

covered by the winding and the heat can not be dissipated directly to the ambient.

The thermal resistance between the core/winding surface and the ambient is calculated by

$$R_{th,v-A} = \frac{1}{\alpha S_v} \tag{31}$$

where α is the heat transfer coefficient for the surface S_v. This could be calculated by empirical equations for natural convection [42][45] and forced air cooling [45][43].

Based on the previous assumptions, the maximum power density of a transformer for the considered DC-DC telecom converter is calculated for different operating frequencies. The results for a 1 kW transformer with natural convection are shown in Fig. 17, where the space for the pace air flow has been neglected. In Fig. 17, the results for the calculations presented by Gu & Liu [37] are also shown, which have been validated with measurement results.

The results using the presented calculation method and that from [37] correspond very well in the lower frequency range. For higher frequencies the model applied in this paper leads to higher achievable power densities. This is especially true if the aspect ratio of the transformer is unconstrained and in the optimization algorithm also core shapes with a low height can be considered. These lead, in the higher frequency range, to lower overall losses and a larger cooling surface (c.f. Fig 10). Due to the winding arrangement/shape (cf. Fig. 15) the resulting planar cores have a tube-type structure and differ from the conventional known (ELP, etc.) disk-type planar cores, which lead to lower power densities than the tube-type structures. This is especially true if the height of the transformer is limited as presented in [47].

In case the aspect ratio is limited to cubic shapes then similar power densities result as with the approach presented in [37] (cf. Fig. 17).

In Fig. 18, the power density of the transformer for the considered 5 kW telecom power supply with different operating frequencies is shown. As shown, a maximum value of approximately 29 kW/dm^3 at an operating frequency of 400 to 500 kHz could be achieved, which includes a space for the air flow of ≈5mm.

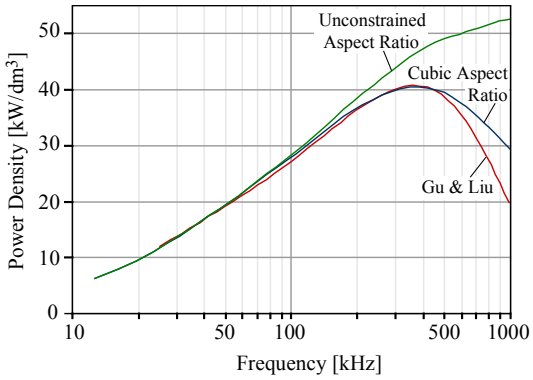


Fig. 17. Comparison of the calculated power density of the presented approach and that of Gu & Liu [37]. For the blue trace the aspect ratio of the transformer is limited to cubic shapes while for the green trace it is unconstrained. Volume of the space for the air flow is neglected.

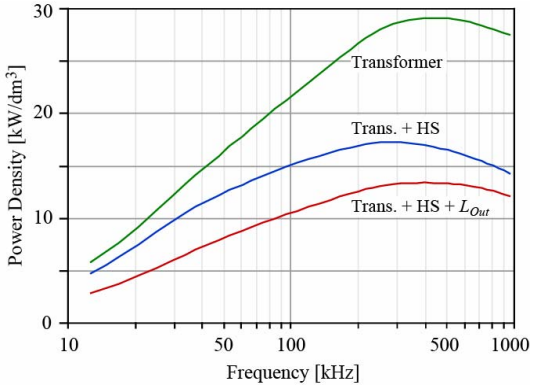


Fig. 18. Power density of the transformer with natural cooling (top line) including the space for the air flow. Volume of the semiconductors' heat sink is added (middle line) and the volume of the output inductors is also added (bottom line).

If the volume of the semiconductors' cooling system, calculated with a CSPI = 30 $W.K^{-1}.dm^{-3}$ (cf. Sect. II.A and (11)), is included the maximum power density decreases to approximately 17 kW/dm^3 at 300 kHz. There, the conduction and ZVS switching losses of the full bridge and the conduction losses of the output rectifier are considered based on measurements of APT50M75 MOSFETs and APT100S20B Schottky Diodes. Since the switching losses increase linearly with frequency the optimal operating frequency decreases.

When the volume of the two output inductors is also considered the power density further decreases to approximately 13 kW/dm^3 at 400 kHz. Since the value of the required output inductance decreases linearly with frequency, the optimal operating frequency then increases.

As a next step, forced air cooling of the magnetics is considered, where the heat transfer coefficient (31) is significantly lower and more heat could be dissipated via the surface. For calculating the effective power density the volume of the fan and of the air channel around the transformer must be considered. The calculation of the fan volume is based on two assumptions:

- the power consumption (10) of the fan is limited to 10 W (cf. (31)).
- the volume flow in the channel, which is defined by the air speed, is approximately 2/3 of the maximum fan volume flow (8).

Based on these assumptions the volume is calculated by

$$Vol_{Fan} = 0.83 \frac{\left(K_3\, b_K^3\, l_K^3\, v^3\, P_{Fan}^3\, K_1\right)^{\frac{9}{4}}}{P_{Fan}^3\, K_1^3}. \qquad (32)$$

The resulting volume of the transformer with fan and air channel is presented in Fig. 19, where a maximum power density of approximately 69 kW/dm^3 could be achieved by the tube type transformer at a switching frequency between 500 kHz and 600 kHz. The disc type design reaches 61 kW/dm^3 at 300 kHz. With the addition of the semiconductors' heat sink the power density decreases to 26 kW/dm^3 and with the addition of the output inductors it further drops to 21 kW/dm^3.

B. Inductor

In the telecom power supply (Fig. 14) being considered a current doubler is used for rectification and filtering. The volume of the two output inductors can be calculated with a similar method as previously presented. In the case of an inductor, the maximum AC flux density in the core is given by

$$B_{Max} = \frac{L\left(I_{L,p} + I_{L,DC}\right)}{N_L A_L} \qquad (33)$$

where $I_{L,p}$ is the peak value of the ripple current and $I_{L,DC}$ the DC component of the inductor current. Due to the DC component of the inductor current, the optimal thickness of the foil is calculated by

$$d_{Opt,v} = \frac{1}{\sqrt[4]{\frac{5N_v^2 - 1}{15}}} \cdot \sqrt[4]{\frac{I_{DC}^2 + I_1^2}{I_1^2}} \cdot \frac{\sqrt{2}}{\sqrt{\omega \mu_0 \sigma}} \qquad (34)$$

where only the fundamental component of the triangular current ripple I_1 is considered.

The value of the required inductance results from the allowed ripple current in the inductors. In the considered converter, it is assumed that the total peak-to-peak current ripple in the output capacitors is limited to 10% of the DC output current. Since the voltage time product decreases with increasing frequency, the value of the required inductance also decreases linearly with frequency. This results in an increasing power density with increasing operating frequency until the increasing losses ultimately causes the power density to decrease (cf. Fig. 20).

During the optimization, the maximum flux density B_{Max} must be kept below the saturation flux density i.e. less than 0.3..0.4 T for ferrites. Especially, at lower operating frequencies, the size of the core/inductor with ferrite material is mainly determined by the saturation flux density and only at higher frequencies by the losses in the core. This could be seen in Fig. 20 where the power density of the inductors (ratio of transferred power to volume) is shown for ferrite materials (N87-EPCOS) and also for an amorphous core (SA1-Metglas/$B_{Max} \approx$ 1T).

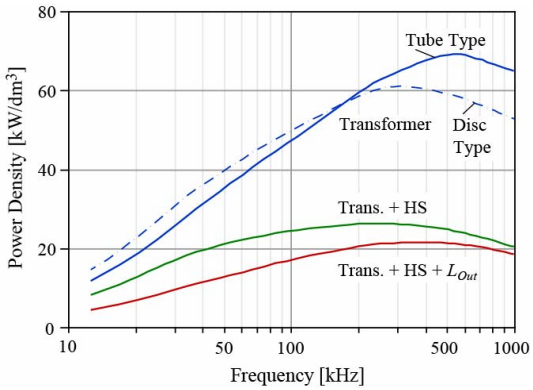


Fig. 19. Power density of the transformer with forced air cooling (top line) including the volume of the transformer's fan. Volume of the semiconductors' heat sink is added (middle line) and the volume of the output inductors is also added (bottom line)

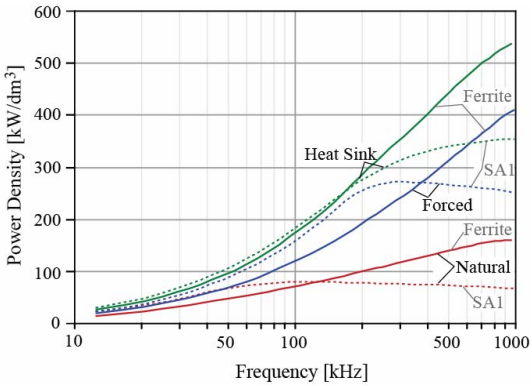


Fig. 20. Output inductor power density for natural, forced and indirect air cooling using ferrite and amorphous cores. The volumes of the fans/heat sinks/boundary layers have also been considered.

C. Magnetic Devices plus Heat Sink

In order to increase the power density further an indirect cooling system, as shown in Fig. 21, is applied. Here the transformer losses are not dissipated via the surface of the transformer but via a Heat Transfer Component (HTC) and an additional heat sink/fan [48].

The losses in the transformer/inductors are calculated as previously presented. The thermal model, however, must be adapted to the new cooling method. If the heat dissipation via the surface is neglected the complete heat must flow in the windings from the outer to the inner layer and in the core from an outer leg to the HTC. Therefore, the hot spots are the outer winding layer and the centre of the outer leg. In order to reduce the temperature drop along the core ($\lambda \approx 4$ K.m^{-1}.W^{-1}) 2 mm thick copper foils are connected in parallel to the thermal resistance of the core. For the results presented here it has been assumed that the thermal conductivity of the HTC is very high ($\lambda \approx 30000$ K.m^{-1}.W^{-1}), i.e. that the HTC is made of an ideal heat pipe, so that the temperature drop along the HTC is negligible.

The volume of the heat sink and the fan for the transformer can be calculated with the CSPI (11), where the thermal resistance of the heat sink is required. In order to achieve a minimal total volume the thermal resistance must be included in the optimization of the transformer.

In Fig. 22, the resulting power density of the transformer including the volume of the HTC, Cu-bars, heat sink and fan is shown in the upper traces. There, a maximal power density of approximately 138 kW/dm^3 for the transformer with N87, including heat sink and fan, is achieved. With the high frequency N49 material even a power density of 150 kW/dm^3 at 800 kHz could be achieved. Since the N49 material out performs N87 material only at very high frequencies the overall system power density is smaller with N49 than with N87. This is caused by the relatively small share of the transformer volume on the overall system volume and the volume of the semiconductor heat sink increasing with switching frequency. With the disc type transformer again a lower power density results (117 kW/dm^3 at 500 kHz).

If the heat sink for the semiconductors is also considered the value decreases to 34 kW/dm^3. For the system including the output inductors a maximal value of 28 kW/dm^3 at 300kHz is achievable.

If these values are compared with values given in the literature, it is important to note that often the volume required for the air flow, and/or the additional fan/heat sink is neglected and only the volume of the transformer is considered.

D. Summary

For an isolated telecom DC/DC converter, the power density of the transformer, semiconductor cooling system and output

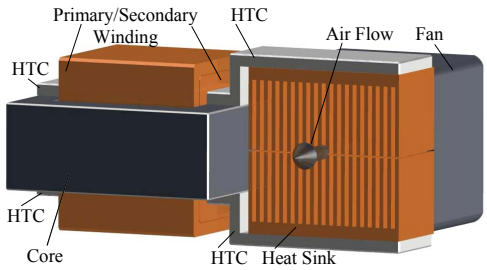


Fig. 21. Transformer with double sided indirect air cooling via a Heat Transfer Component (HTC), a heat sink and a fan.

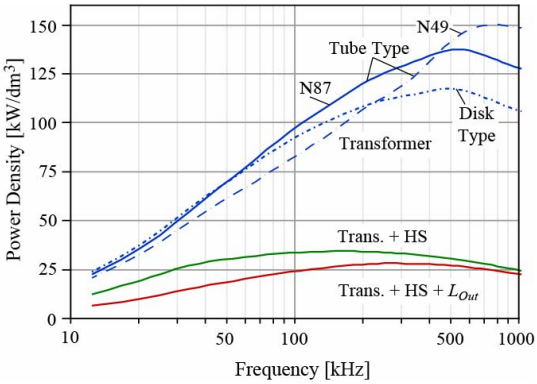


Fig. 22. Power density of the DC-DC converter with indirect air cooling (top line) including the volume of the transformer's heat sink and fan. In the middle line the volume of the heat sink of the semiconductors and in the lower one the volume of the output inductors is accounted.

inductors is very dependent on the employed cooling method. For natural cooling the power density limit is 13 kW/dm^3 and increases to 21 kW/dm^3 for forced air cooling and up to 28 kW/dm^3 for indirect air cooling. It is interesting to note that the optimal switching frequency for maximum power density is relatively low, in the range of 200kHz to 300 kHz, when the cooling system of the semiconductors is included. Compared to these values the power density of the complete DC-DC converter, including power switches, controller and capacitors, is lower by a factor of 2.5 to 3. A complete 1U-5 kW telecom DC-DC converter has been developed at ETH Zurich and a power density of 10 kW/dm^3 has been achieved.

IV. Impact of EMC Filters on Power Density

The EMC filter typically occupies a significant volume of a power converter and therefore has a significant impact on the power density. The EMI filter volume is dependent on the converter topology and switching frequency. In order to illustrate the influence the EMI filter has on power density, two converter topologies, a three-phase AC-DC-AC Sparse Matrix Converter (SMC) and a three-phase unity power factor Vienna Rectifier (VR), are selected for in-depth analysis. The EMC filter design for these two topologies is performed in order to obtain minimum filter volumes, based on typical power filter design practices.

A. Design of EMC Filters

The total EMC filter is comprised of a combination of multiple high performance differential (DM) and common (CM) mode filter stages, which fulfill the conducted emissions (CE) requirements from CISPR 22 for Class B equipment in the frequency range of 150 kHz to 30 MHz [49]. The limits used in the design procedure are actually 6 dB lower than Class B, as displayed in Fig. 23, in order to provide a safety margin for ensuring compliance. The design is based on an optimization routine [50], which calculates the filter components values, based on a series of constraints, that lead to minimum filter volumes.

A series of simplifications are performed in order to reduce the calculation effort. The simplifications are:

(i) the accurate calculation of the harmonic content of the power converter's switched voltages is replaced by simplified envelopes, which are functions of the topology, modulation index and switching frequency, and they do not consider the influence of parasitics and voltage rise and fall times;

(ii) the circuits are considered symmetric regarding the three-phases, so that single-phase equivalents are used;

(iii) the parasitics, inter-component couplings and the effect of the tolerances on the designed filter components are neglected for the attenuation calculation;

(iv) parasitics inside the power converters are neglected, except for the capacitances to ground (PE), which are responsible for CM paths and are lumped into one capacitance Cg which is summed together with any of the capacitances to PE;

(v) the effects of internal power supplies and gate drive circuits are neglected, and;

(vi) the capacitor values and core dimensions are available in a continuous range;

(vii) only natural air cooling is used for the inductors.

The starting point of any EMC filter design is the determination of the frequency spectrum for the DM voltages and currents and the CM voltages. These voltages are compared to the desired limits at the frequency of interest, $f = \omega/2\pi$, which is 150 kHz for switching frequencies lower than 150 kHz or the switching frequency for higher frequencies. This then gives the required attenuation, Att_{req}, at the frequency of interest.

The two power converter topologies are presented in Fig. 24, along with the simplified equivalent circuits used for the filter design calculations, where the LISN circuits are replaced for 50 Ω resistors representing the input sensing resistance of a test receiver. The choice of a two- or three-stage filter is dependent on the required attenuation, the cost and the volume of the filter [51]. It is shown in Fig. 24(a) that a two-stage filter is considered for a SMC and in Fig. 24(b) a three-stage filter is considered for the VR. With the SMC, an output CM choke is included, since the CM voltage at the input terminals of the electric motor must be limited. The output cable and the machine usually present a high capacitance to PE when compared to the capacitance between the converter's semi-conductors and cooling system. Therefore, for simplicity reasons, this is the only capacitance to PE considered in the design of the SMC filter. The first DM capacitors $C_{DM,1}$ are chosen in order to limit the high frequency ripple of the input voltages of the SMC to ±7.5% of the peak input RMS voltage. For the VR, the boost inductors, L_{boost}, are also considered as part of the filters, although their design is based on high performance ferrites and limiting the input peak-to-peak current ripple to 20% of the peak input current.

B. Multi-stage DM Filter Volume Minimization

In order to guarantee that the designed filters are of minimal volume, the desired component values can be derived as functions of two equations, namely the required attenuation at a given frequency and the total volume, which is to be minimized. The main assumptions are:

(i) the inductors are designed for their low frequency RMS current;

(ii) the parasitics of the components do not influence the attenuation at the relevant frequency, and

(iii) the boost inductor is not included in the analysis and its value is defined by current ripple requirements.

In order to simplify the problem, the asymptotic approximation of the attenuation, *Att*, for a LC filter is used

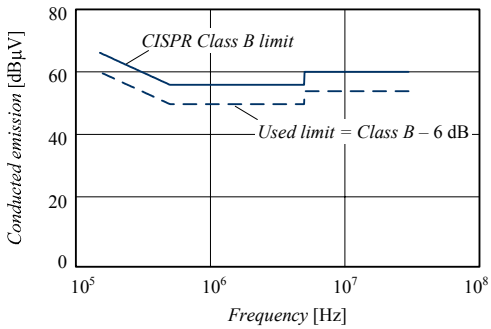


Fig. 23. Conducted emissions limit for CISPR Class B and limit of Class B minus 6 dB used in the design procedure.

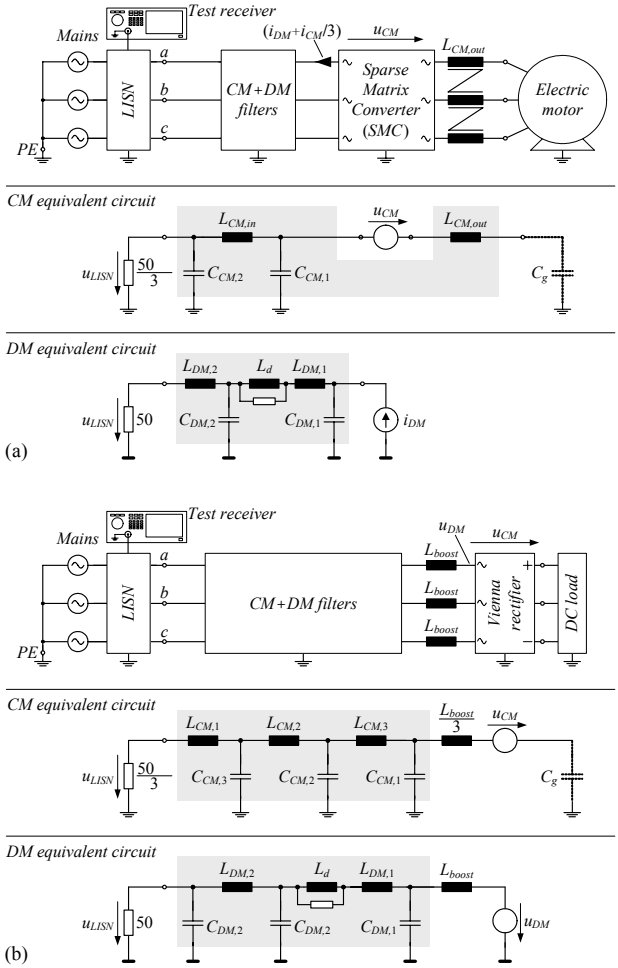


Fig. 24. Converter and filter topologies with simplified equivalent circuits for (a) Sparse Matrix Converter, and; (b) Vienna Rectifier.

[51], which leads to

$$Att(\omega) = \frac{1}{\omega^{2\cdot N} \cdot \prod_{j=1}^{N} L_j \cdot \prod_{j=1}^{N} C_j}. \tag{35}$$

It can be proven that for the smallest total inductance each of the individual inductors must have the same value and the same is valid for the capacitors. Based on that, only two variables are left to minimize the volume.

Let us consider only the case of a single LC stage, which shows the basic principle of minimizing a filter's volume. The required attenuation, Att_{req}, equation can be further simplified to

$$Att_{req} = \frac{k_{att}}{L \cdot C}, \text{ where } k_{att} = \frac{1}{\omega^2} \tag{36}$$

The second equation for the minimization problem is the total volume of the filter, which is the sum of the volume of the inductor with the volume of the capacitor

$$Vol_{filt} = Vol_L + Vol_C . \tag{37}$$

It can be assumed the volume of this type of component is directly related to their stored energy, so that volumetric coefficients for inductors k_L and capacitors k_C are defined as

$$Vol_L = k_L \cdot L \cdot I_{nom}^{\ 2} \text{ and } Vol_C = k_C \cdot C \cdot U_{nom}^{\ 2} . \tag{38}$$

These coefficients can be derived based on data sheet information from capacitors and on a series of inductor designs as shown in Fig. 25. Fig. 25(a) depicts the linearized dependency of volume for different types of mains rated capacitors, while Fig. 25(b) displays the volume of Molypermalloy based inductors designed for mains operation.

It follows that,

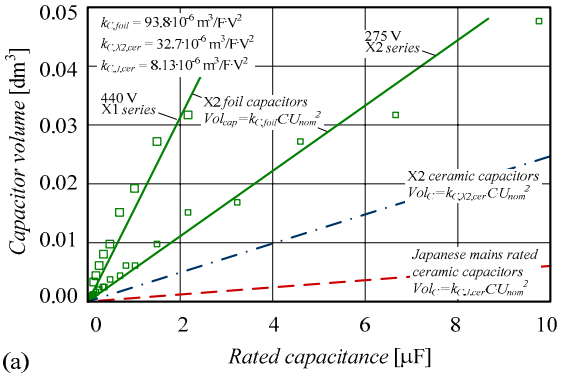
$$Vol_{filt} = k_L \cdot L \cdot I_{nom}^{\ 2} + k_C \cdot C \cdot U_{nom}^{\ 2} . \tag{39}$$

Rearranging (36) in terms of C and inserting it in (39) leads to

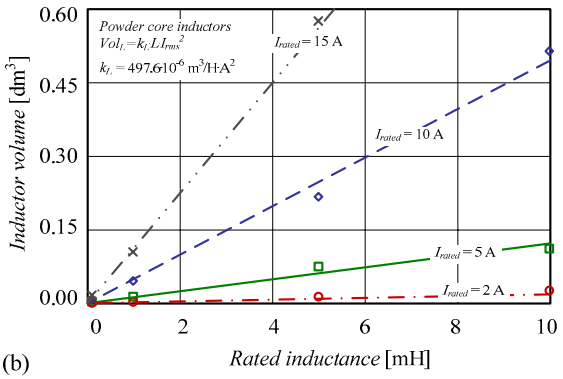
$$Vol_{filt} = k_L \cdot L \cdot I_{nom}^{\ 2} + k_C \cdot \frac{k_{att}}{L \cdot Att_{req}} \cdot U_{nom}^{\ 2} . \tag{40}$$

By differentiating (40) with L the minimum volume point can be found and the values for the components are defined by

$$L = \frac{U_{nom}}{\omega \cdot I_{nom}} \sqrt{\frac{k_C}{k_L \cdot Att_{req}}} , \qquad C = \frac{I_{nom}}{\omega \cdot U_{nom}} \sqrt{\frac{k_L}{k_C \cdot Att_{req}}} . \tag{41}$$



(a)



(b)

Fig. 25. Volume and volumetric coefficients of different filter components. (a) Linearization of capacitors' volume for different mains rated types, X2 foil, X2 ceramics and Japanese mains rated ceramics [52], [53]. (b) Linearized volume of toroidal Molypermalloy inductors as a function of rated inductance, current and value [54].

The same procedure can be extended to multi-stage filters. Thus, minimal volume filters can be designed based on the ratings of the components and their volumetric coefficients.

Requirements related to control issues must also be considered. In order to provide sufficient passive damping that cause minimum losses and avoiding oscillations, also for no-load operation, RL networks are included in the choice of the topologies. These networks are used for damping resonant frequencies introduced by the filter components and the uncertainties in the mains impedance, which could shift given resonances or introduce new resonant circuits with low damping. For simplicity reasons the influence of the RL damping networks in the attenuation is neglected and the inductors L_d are considered to have the same volume as inductors $L_{DM,1}$.

Regarding the DM spectra of emissions, the SMC is considered as a current source i_{DM} (Fig. 24(a)), while the VR is treated as a voltage source u_{DM} (Fig. 24(b)) due to their inherent shaping of the current and voltage waveforms.

C. Multi-stage CM Filter Design

For the design of the CM filters, the converters are considered as voltage sources u_{CM} (Fig. 24), which are dependent on modulation, input and output voltages and switching frequencies. The CM filter of the SMC is split into an output CM inductor and a two-stage CM filter at the input. The aim of the output inductor is to keep the CM RMS voltage at the input terminals of the motor lower than 15 V for any switching frequency and any capacitance to ground, C_g, values. The remaining components are responsible for providing the total required attenuation.

Two types of components are considered for the CM filters: ceramic capacitors which are Y2 rated [53] and CM inductors based on toroidal nanocrystalline cores [55], which are "state-of-the-art" in their class. An earth leakage current limitation of 3.5 mA is used and this bounds the total capacitance per phase to approximately 40 nF at 50 Hz, which is reduced to 30 nF per phase and evenly distributed among the filter stages.

The design of the CM inductor is more involved and a maximum window factor of 0.28 is considered. The design takes into consideration the variation of the complex permeability of the cores as well as the total losses, where the maximum temperature rise is limited to 75 °C.

The cores of the CM inductors are specified as a function of the required area product A_eA_w, which is a function of the switching frequency, rated DM current, CM voltage, number of windings, window factor, maximum current density and maximum flux density at the switching frequency or at the mains frequency (50/60 Hz). A series of CM chokes are designed in order to empirically determine linearized functions that are used for the filter calculations. Based on these designs the maximum current and flux densities are curve fitted as shown in Fig. 26 and these curves are used in an automatic design procedure of the inductors.

The area product presents a quite predictable relation to the volume of an inductor and this is shown in Fig. 27(a) for various core sizes. A relation of the type $k.A_eA_w^{\ 3/4}$ is commonly used, although for this work a power of 0.668 has been used for higher accuracy. Another relationship, which can be approximated, is the maximum impedance at a given frequency and current as function of the area product as shown in Fig. 27(b), where as an example a frequency of 150 kHz and a RMS current of 15 A is used. With these relationships it is possible to estimate the volume of a CM choke as a function of rated current and required impedance at the frequency of interest.

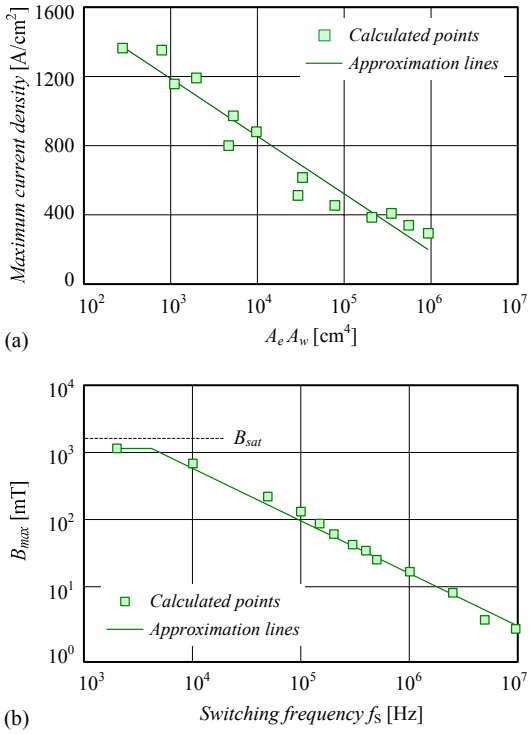


Fig. 26. CM inductor design curves for core material VAC VITROPERM 500F (a) Maximum current density as a function of the area product A_eA_w. (b) Maximum flux density as a function of the switching frequency.

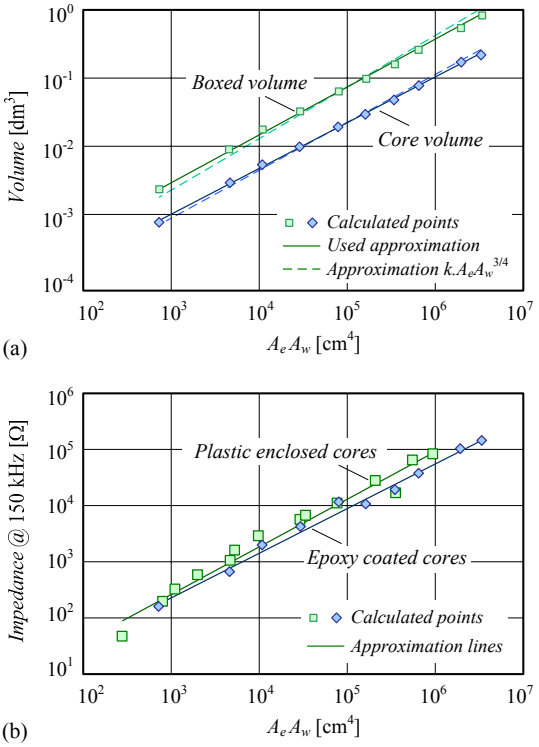


Fig. 27. (a) Dependency of an inductor's boxed and core volume on area product A_eA_w of the used material. (b) Impedance at 150 kHz and 15 A_{RMS} as a function of area product for two types of cores, namely epoxy coated cores and cores with a plastic enclosure [55].

D. Sparse Matrix Converter Power Density Limits

Based on the presented filter design procedures the volume of the various filter components can be derived as function of the converter rating, switching frequency and total capacitance to ground C_g. This is of high importance since optimum switching frequencies can be chosen to minimize the total converter volume. The total volume of the EMC filters for a SMC is displayed in Fig. 28 along with the contributions of the DM and CM filter volumes as well as the volume of the first DM capacitors $C_{DM,1}$ for two different values of capacitance to ground C_g. From these figures it is observed that the DM filters dominate the filters volume for lower switching frequencies and that the CM filter volume is highly dependent on the capacitance to ground. The increased volume of the CM filter at lower frequencies in Fig. 28(b) is a result of the increasing size of the output CM inductor. An increased total volume is seen at 150 kHz due to the CE requirements and the necessity of filtering low order switching frequency harmonics.

Taking the results shown in Fig. 28(b) for $C_g = 10$ nF, it is possible to derive the power density limit curves as a function of the switching frequency. This is presented in Fig. 29 for three different capacitor technologies. Since the power semiconductor losses would reduce the achievable power density for higher switching frequencies, it is seen that a power density limit of

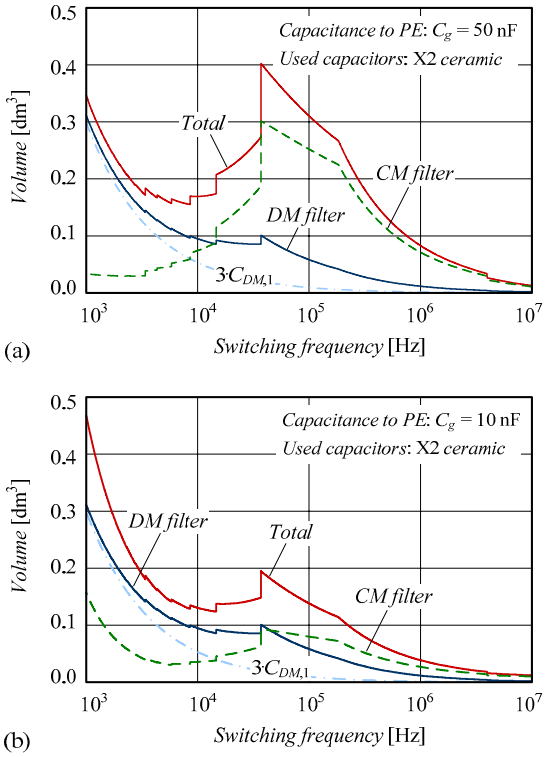


Fig. 28. The total and partial volumes of the EMC filters for a SMC rated for 230 V RMS phase voltage, modulation index M=0.7, mains frequency 50 Hz, output power S_2=5 kVA and X2 rated ceramic capacitors for two different values of capacitance to ground: (a) $C_g = 50$ nF, and; (b) $C_g = 10$ nF.

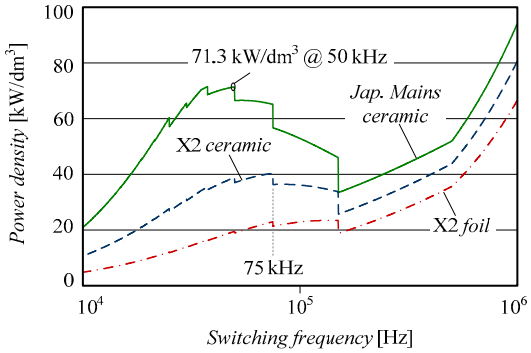
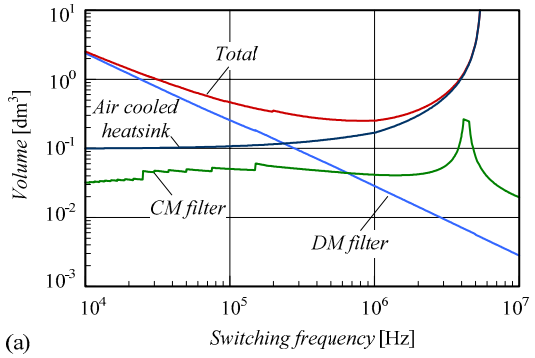


Fig. 29. Power density limits for three different capacitor technologies as a function of the switching frequency considering only the EMC filter for a 5 kVA Sparse Matrix Converter $C_g = 10$ nF.

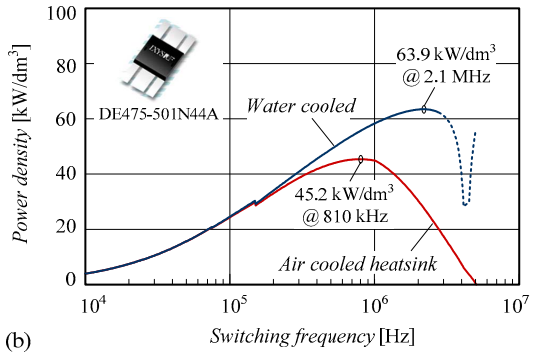
71.3 kW/dm^3 is achieved with ceramic capacitors rated for the Japanese mains at a switching frequency of 50 kHz. This frequency is around 75 kHz for the other capacitor technologies, but at much lower power densities. This shows the importance of the improvement of passive components technology for increasing power density.

E. Vienna Rectifier Power Density Limits

The same procedure for the calculations is made for a 10 kW VR and the results are shown in Fig. 30. The calculations for the volume of the cooling system of the power semiconductors (forced air and water) are included, based on the considerations of Section II [1]. For the forced air cooling system, a $CSPI = 25$ W.K^{-1}.dm^{-3} is used. While for the water cooled system the dimensions as in [56] are utilized. The semiconductor losses are estimated for a IXYS DE475-501N44A RF MOSFET and two paralleled Cree SiC Schottky Diodes (10 A / 600 V) [16] leading to a required thermal resistance from the heat sink to ambient in order to limit the junction temperatures to 125 °C with an ambient temperature of 45 °C. A total capacitance to ground of $C_g = 2$ nF is considered. The DM capacitors are X2 rated ceramics [53]. In Fig. 30(a) it is seen that CM filter and cooling system volumes are the main contributors to the total volume and that a minimum volume is achieved for a switching frequency around 1 MHz for an air cooled system. The achievable power densities, for just the EMI filter and cooling system, are presented in Fig. 30(b), where it is seen that a water cooled system is capable of further increasing the power density for frequencies higher that 1 MHz.



(a)



(b)

Fig. 30. (a) Total and partial volumes of the EMC filters and cooling system for a Vienna Rectifier rated for 230 V RMS phase voltage, 800 V output voltage, output power P_2=10 kW and X2 rated ceramic capacitors for $C_g = 2$ nF. (b) Power density limits for two different cooling strategies as a function of the switching frequency considering filters and cooling system.

V. DC Link Capacitors

For power electronic systems based on a DC voltage link, the DC link capacitors contribute significantly to the converter volume and hence influence the power density of the total system. For example, a 30% capacitor volume has been

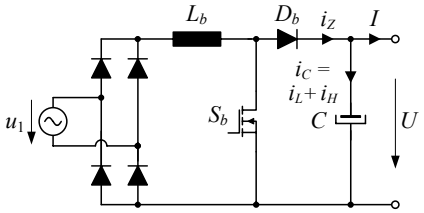


Fig. 31. Single-phase PFC circuit.

mentioned for an ultra-compact active three-phase rectifier [57]. Maximization of the converter's power density, therefore has to also focus on DC link optimization. The tasks of the DC link capacitors (demonstrated, e.g., for a typical single-phase PFC, Fig. 31) are:

(i) to "absorb" the high-frequency switching component i_H of the converter's output current i_Z,

(ii) to equalize the mains power pulsations in case of single-phase systems (component i_L of i_Z showing twice mains frequency), and

(iii) to serve as an energy storage for providing hold-up (e.g., for SMPS) and/or to dynamically absorb a power injection from the load (e.g., in case of an emergency stop of a drive converter, where the magnetic excitation energy of the motor may be fed back to the inverter's DC link) or from the PFC as well as for limiting over voltages ("energy catching").

Hence, the selection of the capacitor must consider its rated current (task (i) and (ii)) as well as the required storage capacitance (being effective for (ii) and (iii)). Typically the choice of capacitor is between electrolytic and foil types.

A. Basic Comparison of Capacitors Types

To demonstrate the basic differences of electrolytic capacitors and foil capacitors, a comparison of the specific charge density q and of the specific energy density w of the two capacitor types shall be performed based on a very simplified calculation. It is assumed that the dielectric material (Al_2O_3 for electrolytic capacitors and, e.g., polypropylene for foil capacitors) shows a specific level of breakdown field strength E^*.

1) Electrolytic Capacitor

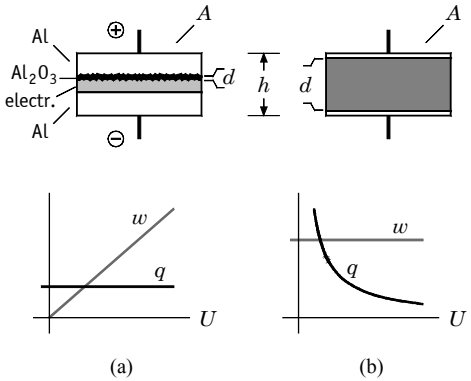
As shown by the structure diagram of Fig. 32(a) the thickness d of the dielectric layer is very small and can be neglected as compared to the total thickness h of the capacitor composite (cathode foil + paper including electrolyte + dielectric layer + anode foil). Hence, the capacitor volume $V_C = A \cdot h$ does not depend on d. Using the basic capacitor relation $C = \varepsilon \cdot A/d$ and substituting d by U/E^* (U ... max. capacitor voltage dependent on E^*) we can calculate the total charge of the capacitor as

$$Q = CU = \varepsilon \frac{A}{d} \cdot d \cdot E^* = \varepsilon E^* \cdot A = \frac{\varepsilon E^*}{h} \cdot V_C \qquad (42)$$

With this, the specific charge density calculates to be $q = Q/V_C = \varepsilon E^*/h = k_Q$. Consequently, based on this simplified model electrolytic capacitors show a charge density that is not dependent on the capacitor's rated voltage $q = const.$, i.e., for practical applications the capacitance-voltage product of electrolytic capacitors directly is linked to the capacitor volume. Then, the calculation of the specific energy density $w = W/V_C$ starting with $W = \frac{1}{2} CU^2$ finally leads to $w = \frac{1}{2} k_Q \cdot U$, i.e., the energy density depends linearly on the rated capacitor voltage $w \propto U$. Fig. 33 shows the specific volumetric energy density for different capacitor values of the same electrolytic type.

2) Foil capacitor

For this capacitor type it is assumed that the thickness h is dominated by the dielectric layer d (cf. Fig. 32(b)). Using the



(a) (b)

Fig. 32. Principle structure of electrolytic capacitors (a) and of foil capacitors (b) and corresponding specific volumetric charge and energy densities in dependency on the rated capacitor voltage *U*.

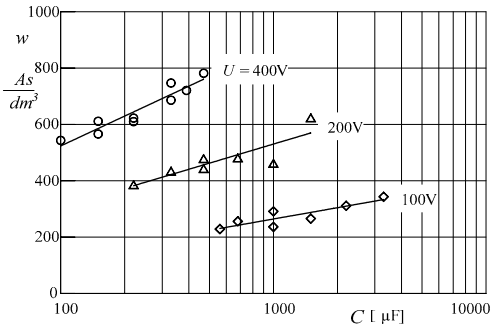


Fig. 33. Dependency of the specific volumetric energy density *w* on the capacity value *C* for different rated capacitor voltages *U* (EPCOS snap-in-type series B41505/B43505).

basic relation of the energy density of the electric field $w = ½ D \cdot E$ (and neglecting the thickness of the conductive foils) it is immediately obvious, that this type of capacitor is characterized by a specific energy density of $w = ½ \varepsilon (E^*)^2$, i.e., $w = const.$. The calculation of the specific charge density q using $W = ½CU^2 = ½QU$ leads to $q = 2w/U$, i.e., the charge density decreases inversely proportional to the rated capacitor voltage $q \propto 1/U$.

B. Electrolytic Capacitor Current Capability

Due to their fairly high current carrying capability and their high specific energy density, electrolytic capacitors are today widely applied in DC voltage links. As a more detailed analysis shows, these capacitors primary have to be dimensioned according to the current carrying capability if special requirements concerning hold-up or over-voltage protection are neglected. Unfortunately, the rated rms current of electrolytic capacitors cannot be easily estimated assuming that the specific

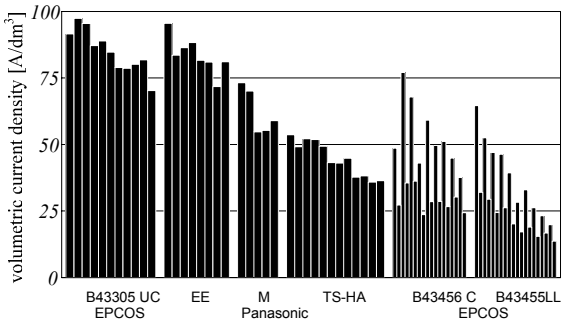


Fig. 34. Comparison of rated specific volumetric current densities s_C of different electrolytic capacitors (rated voltage: 400V). Family types are: leaded (EE, M), snap-in (B43305, TS-HA), and screw-terminal (B43456 C, B43455LL) capacitors; from left to right for each type is increasing capacitance value and size. B43456 C and B43455LL are shown for natural as well as for "base-plate" cooling.

volumetric current density s_C [A/dm³] is approximately constant over a wide range of capacitor types, as is much more the case for the specific charge density (CV-product). The reason for this is that the rated capacitor current I_N for a specific loss resistance R_{ESR} essentially depends on the cooling condition of the component. Consequently, capacitors of a smaller volume (leaded or snap-in types) show a considerably higher specific current capability compared to large-can (screw-terminal) types (cf. Fig. 34).

It has to be mentioned, however, that the rated current values given in many data sheets have to be used with caution. Unfortunately, the manufacturers rarely specify thermal resistances which are essential for a proper design. This is of particular importance since the useful life time of an electrolytic capacitor is strongly influenced by its operating temperature. It further has to be pointed out, that the concept to replace a large-size capacitor by a group of small capacitors connected in parallel (as this would be inspired by Fig. 34 to minimize the DC link volume) is valid only in case that each capacitor has good cooling. This, however, is not true if the components are bundled in the most compact way. In this case, an additional head space has to be considered. A detailed thermal analysis shows that for natural cooling at least a head space volume being approximately equal to the component's volume would be typically required. This emphasizes the importance of extended thermal modeling of the DC link capacitors for the design of modern power converters.

C. Foil Capacitor Issues

As a consequence of the three-phase systems not requiring any low-frequency energy storage in the DC link, the application of foil capacitors seems to be very attractive for raising the converter's power density. For example, a 15 µF/ 1050V foil capacitor of series EPCOS B32678 is specified to a rated current of $I_N = 29$ A (4-pin version). A volume of $V_C = 35x50x57.5mm^3 = 0.1\ dm^3$ leads to a specific current density of almost $s_C = 290A/dm^3$, which is about 3-times higher than very good electrolytic capacitors. Therefore a single foil capacitor would be sufficient to realize a three-phase PFC with an output power of $P_{3PFC} = U \cdot I = U \cdot I_N / 0.73 = 800V \cdot 29A/0.73 = 31.8$ kW (using the eqs. of sect D). This results in a specific capacitor power density of more than 300kW/dm³ (cf. Table 2).

TABLE 2. COMPARISON OF DC LINK AND CONVERTER RATINGS FOR ELECTROLYTIC OR FOIL-TYPE DC LINK CAPACITORS.

		Electrolytic cap. 2 x 390µF/450V	Foil capacitor 1 x 15µF/1050V
Capacitor size		∅3 x 4 cm³	3.5 x 5 x 5.75 cm³
Capacitor volume	V_C	2 x 28 cm³	100 cm³
Cap. rated current	I_N	2.2 A	29 A
Cap. current dens.	s_C	79 A/dm³	290 A/dm³
Output current	I	4 A	40 A
Output voltage	U	800 V	800 V
Output power	P	3.2 kW	32 kW
Cap. power density	p_{PCF}	56 kW/dm³	320 kW/dm³
ESR_H @ 85°	R_{ESR}	2 x 140 = 280 mΩ	≈ 2 mΩ
1/(ωC) @ 100kHz	X_C	2 x 4 = 8 mΩ	≈ 100 mΩ
Cap. losses @ I	P_{loss}	2 x 2.5 W	1.7 W

The very high current capability of foil capacitors is a key advantage for the maximization of the converter's power density, however, their limitations have to be also discussed. Due to the low capacitance value and the high Q-factor (the 15 µF capacitor shows a Q-value of 50 @ 100 kHz!), foil capacitors easily tend to resonant.

D. DC Link Capacitor Current Stress

Omitting the detailed calculation for the sake of brevity, the DC link rms current components of a single phase PFC (Fig. 31) are

$$I_Z = I\sqrt{\frac{16}{M3\pi}} \qquad I_C = I\sqrt{\frac{16}{M3\pi}-1} \tag{43}$$

where I is the ripple free DC output current and M is the modulation index $M=\hat{U}_1/U$. Considering the line-frequency power flow and assuming that the high- and low-frequency components of i_C are not correlated, the currents are given by

$$I_C^{\,2} = I_L^2 + I_H^2 \qquad I_L = \frac{I}{\sqrt{2}} \qquad I_H = I\sqrt{\frac{16}{M3\pi}-\frac{3}{2}}\,. \tag{44}$$

For a typical application where $M \approx 0.8$, this leads to $I_Z = 1.46\,I$, $I_C = 1.06\,I$, $I_L = 0.71\,I$ and $I_H = 0.79\,I$.

For three-phase systems, such as a six-switch inverter operated as three-phase PFC, no line-frequency current I_L will appear, and the current stress of the DC link capacitor, in the ideal case, originates exclusively from the switching currents. Using the relations derived in [58] the DC link rms quantities are given by

$$I_Z = I\sqrt{\frac{20\sqrt{3}}{9M\pi}} \qquad I_C = I_H = I\sqrt{\frac{20\sqrt{3}}{9M\pi}-1}\,, \tag{45}$$

and are valid for ohmic mains behavior ($\cos\varphi = 1$). For PFC-applications, a $M \approx 0.8$ is frequently used, which leads to $I_Z = 1.24\,I$ and $I_C = I_H = 0.73\,I$.

E. Single Phase DC Link Dimensioning

As indicated by (44), the DC link capacitor current i_C of a single phase converter not only contains switching (high) frequency components but is also characterized by a low-frequency (i.e., 100Hz for 50Hz mains frequency) component originating from the pulsating power flow, which is typical for single phase systems. The rated current I_N of electrolytic capacitors is characterized by a frequency dependency due to the fact that the capacitors loss resistance R_{ESR} (mainly influenced by the electrolyte) decreases for increasing frequency. Consequently, the manufacturers usually specify the rated current I_N separately for the low and high frequencies (e.g., f_L=100 Hz, f_H=100 kHz) or, alternatively, by $I_{N,L}$ and a multiplier k_C which gives $I_{N,H} = k_C \cdot I_{N,L}$ (typ. $k_C \approx 1.4\ldots2$). If i_C contains low and high frequency components, the calculation of the capacitors rated losses leads to a limiting curve with an elliptical shape (cf. Fig. 35). Evaluating (44) yields a ratio $k_M = I_H/I_L$ that is constant for a given modulation index (e.g., $k_M \approx 1$ for $M = 0.8$). The intersection of the k_M-line with the ellipse defines the dimensioning point of the capacitor. Generally speaking, if the capacitor is selected based exclusively on its low frequency current, this value $I_L = I/\sqrt{2}$ has to be only slightly increased by a factor of ≈20% (valid for typical capacitors and modulation indices) to get the required rated capacitor current.

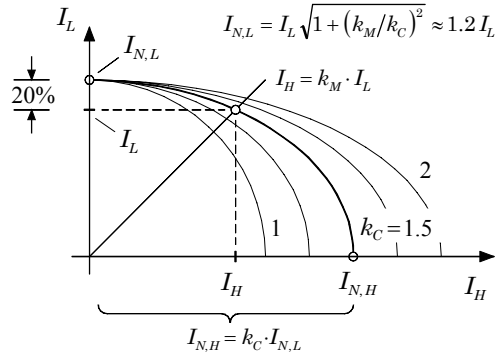


Fig. 35. Capacitor current limiting curve in the case where the capacitor current contains low and high frequency components. For typical single-phase PFC systems, it is sufficient to select a capacitor with a rated current being 1.2-times the low-frequency component (which can be easily determined considering the line-frequency power flow).

F. DC Link Capacitor Power Density Limit – Single Phase System

To provide an estimation of volume inherently required for realizing the DC link, the PFC's through-put power $P_{PFC} = U \cdot I$ (cf. Fig. 31) is related to the capacitor's volume V_C to define a power density $\rho_{PFC} = P_{PFC}/V_C$ for the DC link. Combining the relations derived before ($I_L = I/\sqrt{2}$, $I_{N,L} = 1.2\,I_L$) and using $I_{N,L} = s_C \cdot V_C$ we obtain $\rho_{PFC} = U \cdot s_C/0.85$. Choosing $s_C = 80\text{A/dm}^3$, which is valid for modern compact capacitors in the power range typically used for single-phase converters, and a DC link voltage of U=400V, we obtain a specific power density of $\rho_{PFC} \approx 38\text{kW/dm}^3$.

Considering a slightly more detailed dimensioning example of a 1 kW PFC (U=400V, I=2.5A), a rated capacitor current of $I_{N,L}$ =2.1A is calculated, which can be handled by a, e.g., EPCOS B43305 ultra-compact series (∅30x40mm^2) 390 µF/450 V capacitor, resulting in $\rho_{PFC} = 35\text{ kW/dm}^3$. The pulsating low-frequency component of i_C will lead to a 100Hz voltage ripple of $u_{L,pk} = I/(\omega C) = 10\text{V}$ (≡2.5%), which is usually acceptable for the load-converter. Finally, it has to be noted, that for the application of modern high-current electrolytic capacitors in single-phase converters the component selection is mainly current-oriented and that a capacity-oriented selection is only necessary to comply with the hold-up or over-voltage protection requirements.

G. Specific Capacitor Volume – Three Phase System

A similar calculation is now performed for a three-phase PFC. In the ideal case, the capacitor current of a three-phase PWM converter only contains switching frequency components as calculated in (45) or $I_C = I_H = 0.73I$ ($M \approx 0.8$). The capacitor now has to be selected regarding a current rating of $I_{N,L} = I_H/k_C$. Using again $P_{3PFC} = U \cdot I$ and considering that the DC link of three-phase converters is typically equipped with a series connection of two capacitors (e.g. $U = 800\text{V}$), a DC link capacitor power density limit of $\rho_{3PFC} = U \cdot s_C \cdot k_C / (2 \cdot 0.73)$ assuming $k_C = 1.35$, results in $\rho_{3PFC} = U \cdot s_C/1.08$, which on a first glance seems to be less that the single-phase PFC. Considering, however, that the three-phase system typically has twice the output voltage of its single-phase counterpart, $\rho_{3PFC} = 1.58\,\rho_{PFC}$ is valid, i.e. the three-phase system roughly requires 60% less capacitor volume.

This shall be demonstrated by a brief dimensioning example: A three-phase PFC with $U = 800\text{V}$ has a series connection of two capacitors used in the previous section (2 x 390µF/450V). With a capacitors current rating of 2.2 A and $k_C = 1.35$ results in $I_C = 2.2\text{A} \cdot 1.35 = 3\text{A}$, which leads to $I = 3\text{A}/0.73 = 4\text{A}$. Therefore the PFC's output power is $P = 800\text{V} \cdot 4\text{A} = 3.2\text{ kW}$, i.e. 1.6 kW per capacitor as compared to 1 kW per capacitor for the single-phase system. The proposed dimensioning gives a DC link capacitor power density limit of $\rho_{PFC} = 56\text{ kW/dm}^3$ for the three-phase system (+60%). In other words, if we take the capacitor of a 1 kW single-phase PFC and use two of them connected in series, a 3.2 kW three-phase PFC can be realized. It has to be mentioned, however, that three-phase systems of higher power level usually are equipped with large-can screw-terminal capacitors, which have a lower volumetric current density compared to the capacitor used in this dimensioning example (cf. Fig. 34).

H. Capacitor Sizing for a Back-to-Back Voltage DC link Converter and an Indirect Matrix Converter

The most widely used converter for bidirectional three-phase AC motor drive systems is the back-to-back voltage DC-link converter (BBC) in Fig. 36. The BBC consists of a six-switch active rectifier and a six-switch inverter connected together with a common DC-link capacitor. This configuration allows unity power factor sinusoidal input currents to be drawn from the mains and to supply the load with variable frequency and voltage. The DC-link capacitor provides an energy storage decoupling the inductive input (boost inductors) from the inductive output (load/machine inductance). Due to its volume the DC-link capacitor significantly influences the power density of the overall system. Therefore, in order to maximize the power density of a BBC the DC-link capacitor needs to be minimized as the capacitor volume grows with capacitance value.

In this section the requirements and limitations for the capacitor sizing for a 5 kVA BBC are given. There different criteria for dimensioning the DC link capacitor are:

- Current stresses;
- Maximum voltage ripple for (quasi-)stationary operation;
- Maximum deviation from the nominal DC link voltage after/during transient operation;
- Required energy storage for the demanded ride-through capability.

For the following analysis, only foil capacitors are considered, for the reasons given in subsection C. Foil capacitors are typically dimensioned for a maximum tolerable voltage ripple [59].

The dimensioning for ride-through is based on limiting the maximum DC link voltage drop, ΔU_{DC}, during mains failure for a given hold-up time ΔT at the nominal output power P_2. The minimum capacitance can be calculated as

$$C_{DC,Ride-Through} = \frac{2P_2\Delta T}{\left(U_{DC} - \Delta U_{DC,\max}\right)^2} = 2\,\text{mF} \tag{46}$$

where $U_{DC} = 750$ V, $\Delta U_{DC} = 0.2\ U_{DC}$, $P_2 = 5$ kVA, and $\Delta T = 100$ ms (e.g. five 50 Hz mains periods) are assumed.

However, by applying more advanced control schemes the dimensioning for ride-through capability is not the relevant criterion for capacitor sizing. In case of mains failure the kinetic energy of rotation in the load machine can be used to keep the DC-link voltage above a minimum level, enabling the system to shut-down securely even with capacitor values that are much smaller than calculated in (46).

The maximum voltage deviation from the nominal DC link voltage occurs during transient operation for a power reversal from regeneration to motoring or vice versa. In the following the transient from full regeneration to full motoring is considered for dimensioning. For the analysis the following assumptions are made:

- The power reversal is modelled by replacing the output stage (inverter) including the load machine (e.g. PMSM) with a step-power load (Fig. 37) that is directly connected to the load side of the DC link capacitor;
- Compared to the mains frequency the transient is short;
- The boost inductors are sized so that the peak-to-peak current ripple is 20% of the nominal peak input phase current $\hat{I}_1$ for a standard space vector modulation scheme;
- The control is assumed to operate ideally, guaranteeing always unity power factor at the input. Consequently, the mains phase displacement angle Φ_1 equals 0°;
- The DC link capacitor size is selected such that the maximum voltage deviation ΔU_{DC} during transient operation is limited to 5% to 10% of the nominal DC link voltage (i.e. for $U_{DC} = 750$ V, $\Delta U_{DC} = 50$ V);
- The converter efficiency is not considered and assumed to be 100%.

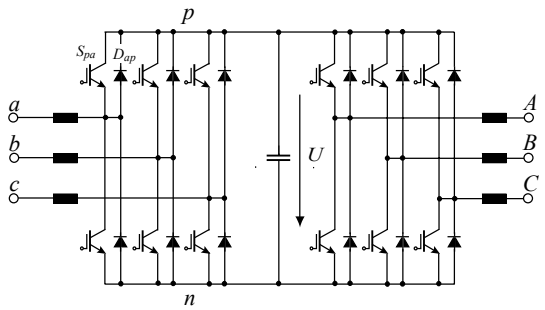


Fig. 36. Back-to-back Converter where the inductors at the output represent the machine inductance.

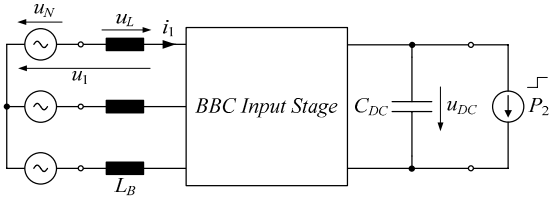


Fig. 37. BBC equivalent model.

These assumptions allow the size of the DC link capacitor to be determined as a function of the mains voltage the nominal DC link voltage U_{DC}, the size of the boost inductors L_B, the nominal output power P_2, and the allowable voltage drop ΔU_{DC}.

Fig. 38 depicts a simplified space vector diagram for the transient operation from full regeneration to full motoring, when the mains voltage phase angle $\varphi_1 = \omega_1 t$ is zero. This means that the d-axis is in-line with input phase a ($u_a = \hat{U}_N \cos(\varphi_1)$). Starting at $t = 0$ when the power reversal is initiated the input current amplitude equals

$$\hat{I}_{1,0} = -i_{1d}\left(t = 0\right) = \frac{2P_2}{3\hat{U}_N} > 0 \tag{47}$$

with a phase displacement angle between the converter input current i_1 and the mains voltage of $\Phi_1 = 180°$ corresponding to regeneration ($i_{1d} < 0$). Simultaneously with the power reversal the DC-link capacitor starts discharging (Fig. 39). The discharging of the DC link capacitor is reinforced by the fact that at the instant when the load step occurs the current direction in the boost inductors has not yet changed. As the digital control is assumed to be ideal, with a delay t_d of one switching period from the beginning of the power reversal, the maximum voltage

$$\hat{U}_{1,\max} = \frac{\sqrt{3}}{3} U_{DC} \tag{48}$$

is applied at the converter input to reverse the current in the boost inductors as fast as possible. A further consequence of the ideal control is that the q-current component at the input can be assumed to be always zero ($i_{1q} \approx 0$). The resulting current change in the d-axis is then

$$\frac{di_{1d}}{dt} = \frac{u_{L_B,\max}(t)}{L_B} = \frac{\hat{U}_N}{L_B} + \frac{\sqrt{3}}{3L_B} u_{DC}\left(t\right) \tag{49}$$

and this equals the current change in input phase a for the given case. As the allowable DC-link voltage change ΔU_{DC} is per definition small compared to the nominal DC link voltage U_{DC}, the following approximation is valid

$$\Delta U_{DC} \ll U_{DC} \quad \Rightarrow \quad u_{DC}\left(t\right) \approx U_{DC} \tag{50}$$

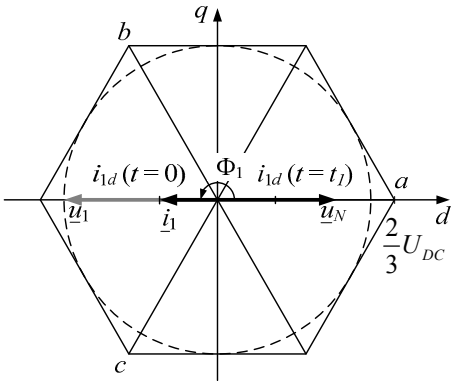


Fig. 38. Space vector representation showing the reversal of the input current i_1.

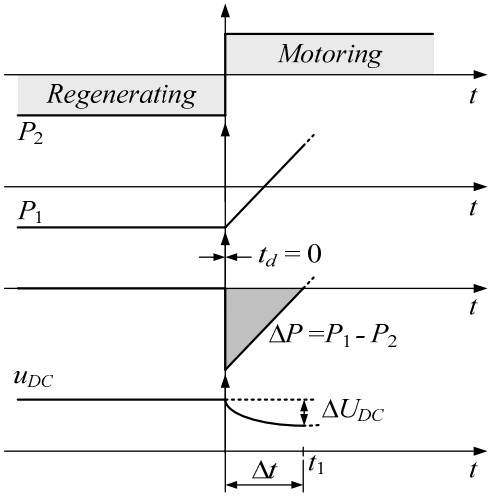


Fig. 39. Output power P_2, input power P_1 and power difference between input and output stages during the transition from regenerating to motoring that leads to a DC link voltage drop ΔU_{DC} for $t_d = 0$.

With (49) and (50), $i_{1d}(t)$ can then be expressed as

$$i_{1d}(t) \approx \begin{cases} -\hat{I}_{1,0} & 0 \le t < t_d \\ -\hat{I}_{1,0} + \dfrac{3\hat{U}_N + \sqrt{3}U_{DC}}{3L_B}(t - t_d) & t \ge t_d \end{cases} . \quad (51)$$

The DC voltage decreases as long as $i_{1d}(t)$ is less than $\hat{I}_{1,0}$. When

$$i_{1d}(t) = \hat{I}_{1,0} \quad (52)$$

the converter input power, given by

$$p_1(t) = \frac{3}{2}U_{Nd}(t) i_{1d}(t) = \frac{3}{2}\hat{U}_N i_{1d}(t) \quad (53)$$

equals the converter output power (similar current amplitude but opposite direction compared to the initial regenerative operation). Consequently, the DC link voltage stops decreasing. The time Δt required for the current reversal can be calculated using (47) and (52) to give

$$\Delta t = \frac{4L_B P_2}{\hat{U}_N\left(\sqrt{3}U_{DC} + 3\hat{U}_N\right)} . \quad (54)$$

In order to calculate the voltage drop, the change in energy of the DC link capacitor needs to be determined from

$$C_{DC}\frac{U_{DC}^2 - u_{DC}^2(t_1)}{2} = C_{DC}\frac{2U_{DC}\Delta U_{DC} - \Delta U_{DC}^2}{2} = -\int_0^{t_1}\Delta p(t)\,dt . \quad (55)$$

By using (50) and (53), (55) can be written as

$$C_{DC}U_{DC}\Delta U_{DC} \approx -\int_0^{t_1}\left(\frac{3}{2}\hat{U}_N i_{1d}(t) - P_2\right)dt \quad (56)$$

Accordingly, minimum required DC link capacitance can be determined from

$$C_{DC,\min} = \frac{2P_2\left[2L_B P_2 + \hat{U}_N t_d\left(\sqrt{3}U_{DC} + 3\hat{U}_N\right)\right]}{U_{DC}\Delta U_{DC}\hat{U}_N\left(\sqrt{3}U_{DC} + 3\hat{U}_N\right)} . \quad (57)$$

If the BBC is operated with unbalanced mains, the 2nd harmonic (with reference to mains frequency) in the DC link current is not zero. Therefore, the capacitor voltage shows a 2nd harmonic component. This leads to a varying power flow similar to the single-phase PFC.

The boost inductors are dimensioned to limit the worst-case peak-to-peak current ripple to 20% of the input current amplitude. Evaluated for a 5 kVA BBC with a nominal DC link voltage of $U_{DC} = 750$ V, the boost inductors are given by

$$L_B = 56\frac{1}{f_s}\ \text{mH} \qquad [f_s] = \text{kHz} \quad (58)$$

According to (57) the link capacitance depends linearly on the boost inductor value. As the boost inductor value decreases with increasing frequency also the DC link capacitor decreases with frequency. Fig. 40 shows how the DC link capacitance and boost inductance vary with switching frequency for a BBC with a nominal output power $P_2 = 5$ kVA, a DC link voltage of $U_{DC} = 750$ V and a maximum DC link voltage drop of $\Delta U_{DC} = 50$ V.

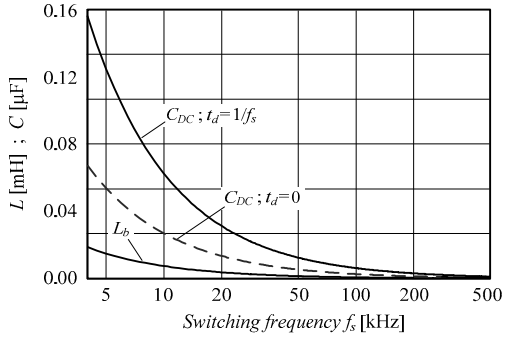


Fig. 40. Required DC link capacitance and boost inductance values as a function of switching frequency and digital delay time (t_d).

Regarding power density the question arises about the sizing of capacitors in converter systems such as Matrix Converters (MCs), which do not require energy storage elements in the power circuit apart from filtering components. The Indirect Matrix Converter (IMC), depicted in Fig. 41, is chosen as the representing topology for MCs as it can virtually be treated as a BBC without a DC link capacitor.

In contrast to the DC link capacitor of a BBC the input capacitors of the IMC cannot simply be considered as energy storage elements at the converter input but form, together with the filter inductors, the last stage of the input EMI filter. These capacitors are selected such that the steady-state peak-to-peak

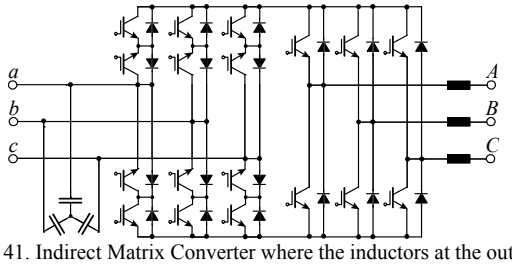


Fig. 41. Indirect Matrix Converter where the inductors at the output represent the machine inductance.

voltage ripple across the capacitors is 10% to 20% of the nominal input voltage. The upper capacitance value is limited by the maximum allowable reactive power drawn from the mains. As the input capacitors of the IMC are connected to the mains, they need to be X2-rated, compared to the DC link capacitors of the BBC.

A typical design for a 5 kVA IMC with a switching frequency of 20 kHz requires a per phase input capacitance in the range of 8 µF and a per phase filter inductance of 100 µH to 150 µH. To analyse the worst-case voltage change across the input capacitors for an identical power reversal as performed for the BBC a single-phase equivalent shown in Fig. 42 is derived, omitting the filter damping. The parameters of the equivalent circuit are as follows: $C_f = 8$ µF, $L_f = 150$ µH (filter inductance including the mains inductance), $U_N = 280$ V, $I_{L0} = -8.9$ A, and $I_2 = 11.8$ A. The current source generates a rectangular waveform with the amplitude I_2, modelling the switching of the converter. U_1, I_{L0}, and I_2 are defined by the worst-case condition for nominal RMS phase input voltage $U_N = 230$ V. Fig. 43 shows the simulation results for the initial voltage drop across the input capacitors for two different switching frequencies keeping the passive components the same. The influence of the load machine is not taken into account. As it can be seen the relative voltage drop is much higher than for the BBC. If the relative voltage drop is made equal for both the BBC and IMC this would lead to unacceptable capacitance values for the IMC due to the reactive power limitations. The comparatively large initial voltage drop, compared to the BBC, across the input capacitors for the IMC caused by the power reversal does not prevent the IMC from correct operation.

In a final step the volume-capacitance dependency for the BBC and IMC are evaluated using foil capacitors. For this purpose, EPCOS series B32676 (750 VDC) capacitors are chosen as a reference for the BBC DC link capacitors, and Evox Rifa series PHE840M as an example of the X2 capacitors (275 VAC) for the IMC. As depicted in Fig. 44, both capacitor series have a similar capacitance-volume dependency. A 5 kVA BBC with a DC link voltage of 750 V, operated at 20 kHz requires, based on (57), a minimum DC link capacitance of approximately 23 µF. While a 5 kVA, 20 kHz IMC would typically need three 8 µF capacitors (24 µF) at the converter input. From Fig. 44, this leads to both converters having a similar capacitor volume of approximately 0.12 dm^3.

The conclusions are as follows:

- For the BBC the DC link capacitor (and boost inductors) size can be reduced by increasing the switching frequency, leading to a higher power density.
- For the IMC, the input capacitor value could be reduced by increasing the switching frequency (see also Fig. 29) only if the voltage ripple is considered (Fig. 38). However, to dimension the capacitors not only the voltage ripple but also the voltage change across the input capacitors caused by a power reversal and the EMI requirements must be considered. Therefore an increase in the switching frequency may not necessarily allow for a reduction in the capacitor value.
- For both converter topologies there are physical limits, i.e. manageable power reversal rate defining the limits for power density.
- In a real design the whole converter including the EMI filter and the load has to be included in the analysis.

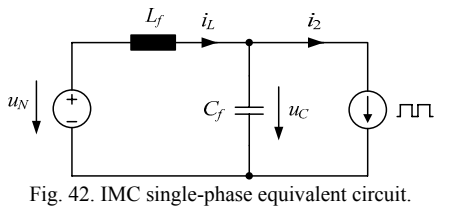


Fig. 42. IMC single-phase equivalent circuit.

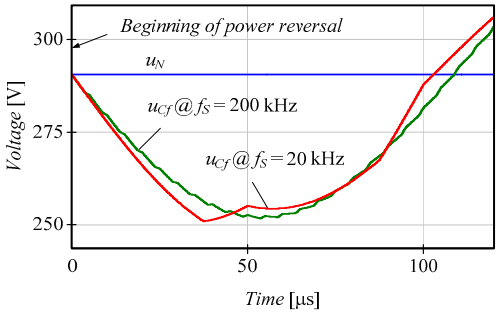


Fig. 43. Initial voltage drop across the input capacitors of an IMC during a power reversal from generating to motoring shown for two switching frequencies keeping the passive components the same.

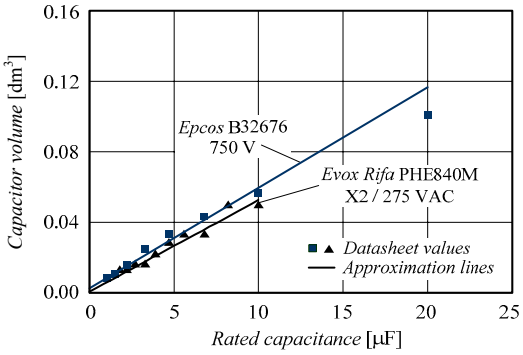


Fig. 44. Capacitor volume vs. capacitance.

VI. Summary

In this paper the power density barriers, based on today's technology, caused by main passive components and air cooling for the fundamental types of power converters are given. To clearly document the technological limits, individual systems with an output power of 5 kW have been considered in each case. These results are therefore valid for the power range of 1 to 10 kW. The practically attainable power density of a realizable converter is less than the indicated limit values since finite volume occupied by the semiconductor modules, gate drivers, printed circuit boards used for the connection of the power components, measuring and control circuits and auxiliary power supplies must also be included. There, an optimization can also take place through spatial integration, i.e. via adjustment of the components shape [21], to which, however, the component manufacturers have so far paid very little attention.

The calculations show that for air cooling of a converter (with ambient temperature of 45°C, a heat sink temperature of 90°C and semiconductor losses of 3% being removed by the heat sink), considering just the cooling system the power density limit is 29 kW/dm^3 (assuming CSPI = 20 W.K^{-1}.dm^{-3}). For an ambient temperature of 65°C this value lowers to 16kW/dm^3.

To enable the overall air-cooled system's power density to reach the level required by 2020, according to [9], requires a major increase in efficiency or an increase in the heat sink temperature or junction temperature. An increase of the heat sink temperature requires, for a given junction temperature, an appropriate decrease in the thermal resistance between junction and heat sink, through the use of higher thermal conductivity interface materials or by optimum heat distribution and/or the use of larger chip surfaces. However, this causes a reduced utilization of the power semiconductor and/or an increase of the realization costs [60]. Alternatively, higher junction temperatures can be used by selecting wide band-gap power

semiconductors to replace the Si power semiconductors. An increase of the thermal conductivity of the heat sink (e.g. by changing from aluminum to copper) has a small influence since the remaining thermal resistance from the heat sink to the air is relatively high.

It is to be remembered that a high power density of the overall system (high global power density) can not be achieved through the use of water cooling or through active cooling using a Peltier element [61] or through temperature reduction by means of compressed air (Ranque Hilsch Vortex tube [62]) [19]. These thermal systems only provide for an increase in the local power density. This localized power density improvement is especially appropriate when the water cooling system is already available, such as with hybrid vehicles, where a water circulation system already exists for the cooling of other main components such as the internal combustion engine.

To enable a further increase in the future power density, a gain is to be made by thermally coupling the magnetic components and capacitors to the heat sink. This significantly increases the surface area that is available for the dissipation of the heat to the environment. The heat dissipation capability then does not scale with the surface area but with the overall volume (see Fig. 7). To enable favorable thermal coupling the use of conventional heatpipes [21] or anisotropic highly thermally conductive materials (solid heatpipes [48]) may find application. Also through the use of a laminated structure in the magnetic core of inductor or transformer it is possible to dissipate the heat from inside the volume [63].

These concepts are therefore of interest since it is expected that substantial progress will be made in material technology regarding the increase of the thermal conductivity (and the improvement of thermal isolation properties). This becomes clear by a comparison of the electrical conductivity of materials, which ranges over 20 decades, whereas for the thermal conductivity, at present, only 4 decades are occupied [64].

The increase in power density of power electronic systems was made possible, so far, by the increase in switching frequency (and decrease in the volume of passive components), particularly through the improvement of the switching characteristics of the power semiconductors.

As an approximation, an increase in power density by a factor of two requires a tenfold increase in the switching frequency. As example, a three-phase, 10 kW, unity power factor rectifier has a power density of 3.5kW/dm^3 [65] for a switching frequency of 48 kHz and a power density of 8.5 kW/dm^3 for a 400 kHz switching frequency [57].

To further increase the power density with an increase in switching frequency, a proportional decrease in the switching times is necessary to maintain a constant efficiency. Switching times as small as 10 ns are then needed for high power and a limiting factor becomes the acceptable level of switch over-voltage caused by the parasitic wiring inductances (current fall rates of > 5 kA/µs could be typical) and/or the losses resulting from the parasitic semiconductor internal and external parasitic capacitances [23]. Furthermore, voltage switching edges with greater than 100 kV/µs demand special dv/dt ruggedness for the gate drive circuits.

Possibilities to decrease the semiconductor internal capacitances are analyzed in [66]. In addition, to obtain higher switching frequencies it is necessary to make the transition to planar connection techniques [26] and 3D integration [67]. This is already used today in the field of microelectronics and in low power rated power supplies [68]. The tuning of the coefficient of thermal expansion (CTE) of the individual materials is of crucial importance here. A further challenge is caused by the large output capacitance of the Super-Junction MOSFETs at low drain to source voltages. This high capacitance leads to substantial pulse pattern distortion at high switching frequencies.

In the future, especially for the mid power range, the frequency increase will occur by using several parallel connected subsystems with phase-shifted carriers and/or interleaving is expect to become an enabling technology. The concept already finds applications today in the low power (VRM [69]) and high power range. As major advantage the frequency increase by interleaving is switching loss neutral in the first approximation, since, for example, in a two phase system each individual system has half the current but with opposite phase at the same switching frequency. This results in a substantial decrease of the input and output ripple [70] and therefore allows for a decrease of the filtering requirement. Furthermore, there is a more even distribution of the power dissipation within the volume, with which “homogeneous power” [71] in the sense of space and time can be referred to. Such a high power density converter system is documented in [15], where a water-cooled, isolated DC-DC converter (12 parallel systems) with a power density of 25 kW/dm^3 (and single-stage LC EMI filter) is described. The specified advantages bring with it an increase in the overall complexity of the system, which, however, with the use of digital signal processing is well controllable. The advancements in digital technology then can be directly applied to power electronics.

With the effective increase of the switching frequency, arrangements to suppress the parasitic non-idealities of the leaded filter elements [67][72] are required. In this context, the electromagnetic integration of inductive and capacitive components [67] represent a very interesting concept, however for power levels within the range of several kW this is not significantly limited by the lack of materials with high permeability and dielectric constants that can be processed in planar layers [28].

Finally, it is noted that this work represents only a first step in the characterization of the technological levels of power electronic systems through the use of FOMs and/or an analysis of the technology gaps and the possible new concepts for reaching high power densities.

Small power level systems can achieve high operating frequencies and extreme power densities using only today's technology. For example, in [69] a 100 MHz VRM with a power density of 3.78 kW/in^3 (230 kW/dm^3 without housing) is presented. In the course of further research it is therefore important to examine, among other things, to what extent the power density is suitable for characterizing converter systems at very different power levels, and for which power levels are specific FOM values to be agreed upon. A benefit through the use of scaling effects, i.e. by using the more favorable relationship between volumes and heat-emitting surface of low power systems (Fig. 8), should not appear as technological progress.

The same also applies to the relative losses of high power systems, since due to the scaling laws these have a smaller value that results in an increase in the efficiency. Due to increasing requirements concerning energy saving, the relative losses are expected to be of major important as a FOM at the converter and the entire power supply chain, e.g. between the mains and point-of-load. In particular, it has to be analyzed what compromise, with regards to efficiency, will result in a maximization of the power density. First considerations show that power density and maximum efficiency lie relatively close together. This is understandable, since the power density is, in the long run, thermally limited with the minimization of the volume, and thus only a relatively small energy loss can be dissipated.

Apart from the continuous power transfer, in future the

"peak power density" (PPD) characteristic must be considered as a FOM especially for hybrid vehicles [7] and More Electric aircraft, where pulse-type manipulation of actuators is important. For example, interestingly, a high short-time overload requirement results in equal volume of a 50 kHz three-phase unity power factor PWM rectifier and a passive 12-pulse-rectifier. Accordingly, significantly higher switching frequencies than required for higher continuous power density are needed. On the other hand, the passive solution exhibits a doubling of the weight compared to the active solution and therefore leads to a potentially higher fuel consumption. Accordingly, for mobile applications, also the specific power is seen to be as an important FOM apart from the power density.

Finally, it is to be pointed out that, if the power density of power electronic converters in the future follows the past trend of increasing by a factor of two each decade (reduction of the linear dimensions by a factor 1.25), and/or the power electronics field on a long-term basis is to dynamically develop itself, it will require an expansion in the research focus from the classical range of power semiconductors, topologies, modulation and control to cooling concepts, high frequency losses of magnet components, materials, interconnection techniques and packaging. Not only should the best possible materials be utilized but also multi-functional materials (i.e. not only considering their main characteristic but also their secondary characteristic such as thermal conduction of magnetic materials [21]), as well as the three-dimensional integration of the converter systems.

The design of highly compact systems must also be supported with multi-domain analysis tools, which apart from the simulation of the circuit must also provide insight into the thermal, electromagnetic [73] and thermo-mechanical properties of the active and passive power components. Only such a global optimization, that includes the full range and influences of the individual material properties [28] as well as the extreme temperature gradients and cycling, will guarantee high reliability and result in a substantial improvement of the power converter's performance indexes.

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