Impact of Power Density Maximization on Efficiency of DC-DC Converter Systems

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***Abstract*—The demand for decreasing costs and volume leads to a constantly increasing power density of industrial converter systems. In order to improve the power density further different aspects, like thermal management and electromagnetic effects must be considered in conjunction with the electrical design. Therefore, a comprehensive optimization procedure based on analytical models for minimizing volume of dc-dc converter systems has been developed at the Power Electronic Systems Laboratory of the ETH Zurich.**

Based on this procedure three converter topologies – a phase shift converter with current doubler and with capacitive output filter and a series-parallel resonant converter – are optimized with respect to power density for a telecom supply (400 V/48 V).

There, the characteristic of the power density, the efficiency and the volume distribution between the components as function of frequency is discussed. For the operating points with maximal power density also the loss distribution is presented. Furthermore, the sensitivity of the optimum with respect to junction temperature, cooling and core material is investigated.

The highest power density is achieved by the series-parallel resonant converter. For a 5 kW supply a density of approximately 12 kW/ltr. and a switching frequency of ca. 130 kHz results.

I. Introduction

The power density of power electronic converters has roughly doubled every 10 years since 1970. Propelling this trajectory has been the increase of converter switching frequencies, by a factor of 10 every decade, due to the continuous advancement of power semiconductor device technology. This increase in power density has been especially important in the design of telecom power supplies which have to operate in a limited space and have maximum weight requirements.

In the near future, the short term operating costs of telecom power supplies will outweigh their capital cost. Along with the high operating cost, due to rising energy prices, the negative environmental effects of increasing energy consumption will demand power supplies with the highest possible efficiency. Therefore, an optimization of power supplies with respect to power density and efficiency for future "Green Data Centers" [1], which enables cost and cooling effort reduction, is required. The main question that arises is: "To what extent does a power density optimization influence the efficiency of the converter system"? In order to address this question an optimization of the converter design is required.

Modern power supply design must consider the thermal issues (thermal interfaces, heat distribution and fluid dynamics) and electromagnetic effects (parasitic elements, electromagnetic coupling, HF-losses and EMI filtering) in conjunction with the electrical design since all these areas significantly influence the size and the efficiency of the system. Therefore, an automatic optimization procedure is applied in this paper to maximize efficiency and/or power density. With this procedure the efficiency, the power density and their mutual influence on two, widely used, telecom power supplies concepts, i.e. a resonant converter and a phase shift converter with capacitive/inductive output filtering, are investigated.

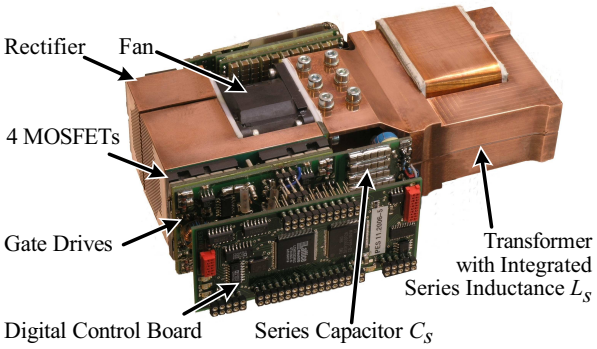


Figure 1. Prototype of an optimized series-parallel resonant converter for telecom applications with a power density of 10 kW/ltr. and the specification given in table I.

The optimization procedure is based on analytic approaches with sufficient accuracy but limited calculation effort instead of general FEM/CFD simulations in order to limit the calculation time. Consequently, analytical models and equations, which include the magnetic devices, ZVS/ZCS switching losses, and HF-losses in the integrated transformer, have been derived and validated for the two converter types. Moreover, the thermal models for the transformer/inductor with integrated cooling system and models for the volume of the required cooling system including the fan have been developed [2], [3]. The optimization procedure also includes methods for calculating

TABLE I
Specifications of the telecom power supplies considered in the optimization presented in this paper.

Input voltage	400 V
Input current	13.0 A
Output voltage	54 V
V_{Ripple} at Output	300 mV_{pp}
Output current	92.6 A
Output power	5 kW
Maximum ambient temp.	45 °C

the volume of the resonant and output capacitors.

Based on this procedure, the power supplies are optimized with respect to the power density for the parameters given in table I. There, the characteristic of the power density, the efficiency and the volume distribution between the components as function of frequency is discussed. For the operating points with maximal power density also the loss distribution is presented. Furthermore, the sensitivity of the optimum with respect to junction temperature, cooling and core material is investigated.

Before the optimization procedure is presented in **Section III** the current and voltage waveforms of the three topologies and the main differences are explained in **Section II**. In **Section IV** the models applied in the optimization procedure are briefly described. Thereafter, the results of the optimization and the comparison of the topologies are presented in **Section V** and the two converter concepts are compared with respect to the maximal achievable power density and efficiency.

II. Converter Topologies

In order to find the limits of the achievable power density and efficiency with an optimization procedure, first the topologies must be identified which show the best potential for volume minimization while maintaining high efficiency. In literature many different topologies have been proposed for telecom applications [4] - [11], which could be basically divided into hard switched, soft switched and resonant converters. Due to the high switching losses, the hard switched topologies do not allow to reduce the volume of the passive components by increasing the switching frequency and simultaneously having a high efficiency.

In the area of soft switched converters the phase shift converter with current doubler or with capacitive output filter [12] (cf. Fig. 2) are promising representatives, which show low switching losses/high efficiency, a simple control, a low number of components and the potential for high power density. Therefore, this concept and a series-parallel resonant converter are optimized in this paper. The series-parallel resonant converter with capacitive or LC output filter as shown in Fig. 4 is a promising converter structure since it combines the advantages of the series resonant converter and the parallel resonant converter. On the one hand the resonant current decreases with the decrease of the load and the converter can be regulated at no load and on the other hand good part-load efficiency can be achieved [13], [14]. Furthermore, the converter is naturally short circuit proof.

A. Phase Shift Converter

In Fig. 2 a phase shift converter with the two considered rectifier structures – a current doubler (CDR) and a center tapped transformer with capacitive output filter (CTC) – are shown. The primary side of these converters and also the control of the switches is the same for both rectifier topologies. However, the current waveforms (cf. Fig. 3) and the related switching and conduction losses, as well as the transformer design are significantly influenced by the rectifier stage.

TABLE II
Main difference between the three considered topologies. For the current doubler output the turns ratio is half the turns ratio of the phase shift full bridge with capacitive output.

	Phase Shift		Resonant
	Current-D.	Cap.-Filter	Cap.-Filter
Turns Ratio	2.75:1	5.5:1:1	7:1:1
Rectifier Volt.	V_{IN}/2.75	2×V_{OUT}	2×V_{OUT}
I_{Off} Leg B	medium	high	low/medium
I_{Off} Leg A	medium	low	zero
Series Inductance	low	medium	high
Reactive Energy	low	medium	zero/low

With a current doubler on the secondary side, a transformer with two standard windings can be applied. There, the turns ratio is $N_P/(2N_S)$ – in the considered case 2.75:1 – what leads to a high secondary voltage, which must be blocked by the rectifier diodes (here: worst case 400 V/2.75≈145 V). The average current in the output inductors is half of the output current, what is roughly also true for the secondary winding of the transformer. During states 1 & 3 (cf. Fig. 3) the current in the secondary winding is equal to the output inductor current, which rises from $I_{1,CDR}$ to $I_{Off,CDR,B}$, which is turned off by a MOSFET of the leg B. During states 2 & 4 the current is determined by the leakage inductance of the transformer. There, the current is decreasing relatively slowly down to $I_{Off,CDR,A}$, since the voltage across the leakage inductance is approximately equal to the forward voltage drop of the conducting power transistors. The value of the leakage inductance and the current at the switching instant must not be too small in order to guarantee ZVS conditions for all four switches. For determining the power density/efficiency limit only the operating point with nominal output power is considered. Part load efficiency is neglected, since the aim is to determine the upper achievable limits. Consequently, a relatively low leakage inductance value (here $\approx 2\mu H$) is sufficient for charging/discharging the parasitic output capacitors of the MOSFETs. This inductance is realized by spatial separation of the transformer windings.

In case the full bridge is combined with a center tapped transformer and a capacitive output filter the series induc-

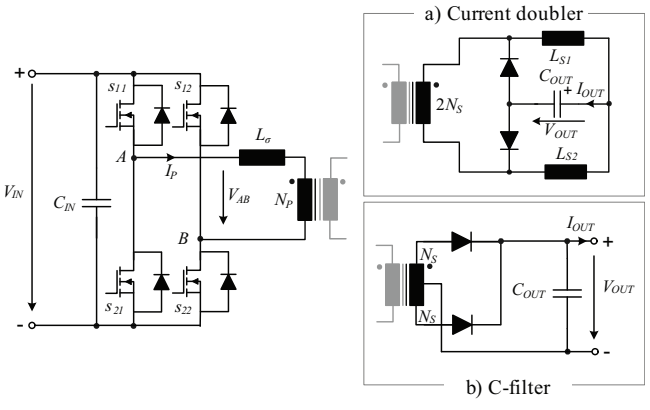


Figure 2. Schematic of the phase-shift converter with (a) current doubler and (b) capacitive output

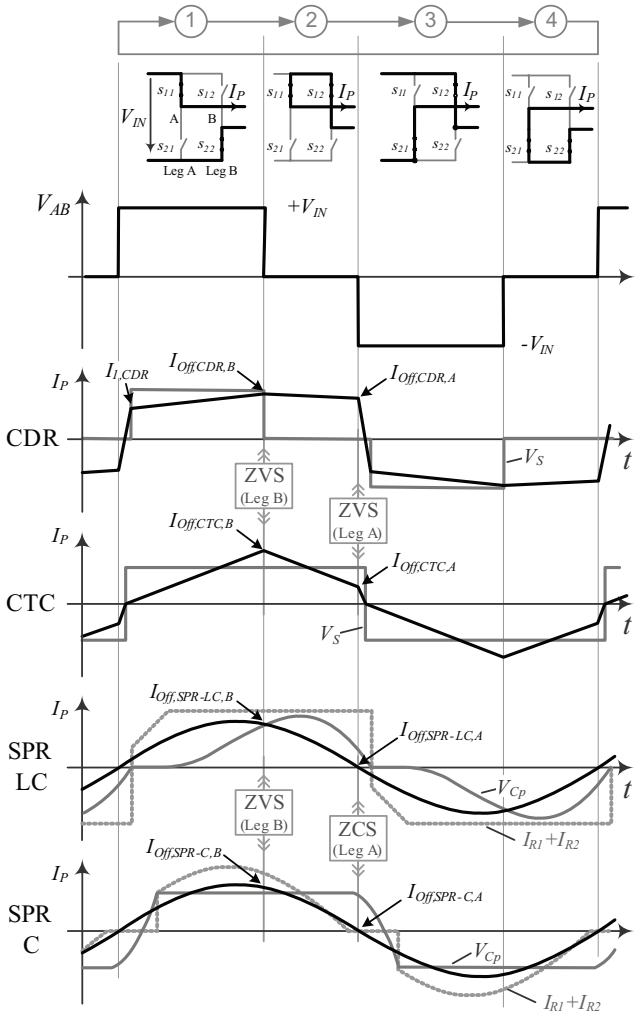


Figure 3. Switching states and primary currents of the phase-shift converter with (a) current doubler (CDR), (b) capacitive output (CTC) and series-parallel resonant converter (SPR) with (c) LC-filter and (d) C-Filter. There, a smaller duty cycle has been used than in nominal, in order to improve the readability of the figure.

tance, which is integrated as leakage inductance L_σ into the transformer, must be larger in order to limit the rise of the current I_P (cf. Fig. 3), since two voltage sources are directly connected via the transformer. During the states 1 & 3 the voltage across L_σ is $V_{IN} - {}^{N_P}/_{N_S} \cdot V_{OUT}$ and the current rises up to $I_{Off,CTC,B}$, which must be turned off by a MOSFET of the leg B. In states 2 & 4 the voltage $-{}^{N_P}/_{N_S} \cdot V_{OUT}$ lies across L_σ and the current decreases down to $I_{Off,CTC,A}$, which is turned off by a MOSFET of the leg A. At the beginning of the following state 3 or 1, the current in the leakage inductance first must be decreased down to zero before it could rise again. During this period the energy stored in the leakage inductance is fed back to the DC link, what results in a reactive power flow. This reactive power flow is required for obtaining ZVS condition in the leg A. With the CDR analogue behavior could be observed, but the energy is lower since the inductance is smaller.

The required turns ratio of the CTC-transformer is N_P:N_S:N_S – in the considered case 5.5:1:1 (assumed max. duty cycle < 0.85, cf. table V) – resulting in $2\times V_{OUT}$ across the rectifier diodes during the blocking state.

B. Series-Parallel Resonant Converter

For the series-parallel resonant converter two different rectifier circuits are considered – a center tapped transformer with LC-output filter and one with capacitive filter as shown in Fig. 4. There, the output filter topology influences the behavior of the dc-dc converter significantly, since the LC-filter acts more like a current source at the output and the capacitive filter as voltage source. The current and voltage waveforms are shown in Fig. 3, where besides the resonant current I_P also the voltage across the parallel capacitor V_{C_P} and the current $I_{R1} + I_{R2}$ in the rectifier diodes is shown.

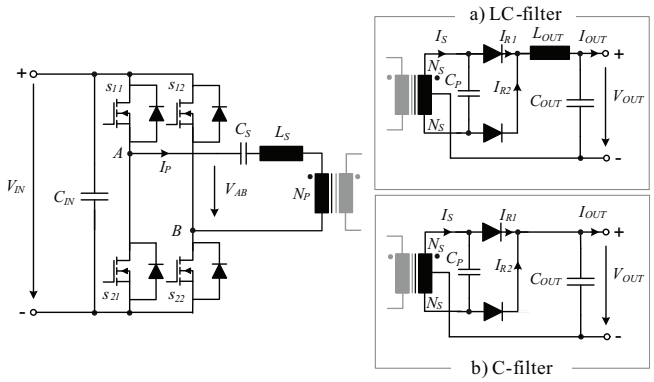


Figure 4. Schematic of the series-parallel resonant converter with a) LC-filter and b) capacitive output

In case of the LC output filter the continuous (CCV) and the discontinuous (DCV) capacitor voltage mode must be distinguished [15]. Since the DCV-mode usually occurs at heavy load conditions, in Fig. 3 the waveforms for this mode are shown. There, the voltage waveform of the parallel capacitor V_{C_P} is clamped by the output current to zero for a certain period of time, which leads to a discontinuous parallel capacitor voltage V_{C_P} showing a large deviation from the purely sinusoidal shape. At the time when V_{C_P} falls to zero the resonant current I_S is smaller than I_{OUT}. As long as I_S is smaller the capacitor voltage V_{C_P} is clamped to zero by the negative difference between I_S and I_{OUT} [-(I_S - I_{OUT})] which flows through the rectifier diodes. From the angle on when I_S is larger than I_{OUT} the positive difference between the currents (I_S - I_{OUT}) charges the capacitor C_P.

Due to the sinusoidal resonant current and the output inductor L_{OUT} the current in the rectifier diodes starts more smoothly resulting in a lower diode turn on stress. In the secondary winding, however, flows a constant DC current plus AC component causing higher transformer losses.

With the capacitive output filter the current in the rectifier steps from zero to the value of the output current. This could result in higher diode forward recovery losses depending on the diode semiconductor technology and in an increased EMI noise level. The transformer secondary RMS current, however, is lower what results in lower losses and a compacter transformer design.

TABLE III
Component values of the LC and the capacitive output filter shown in Fig. 4 for an output voltage ripple of $300\,\mathrm{mV}_{pp}$.

LC-Filter		Capacitive Filter	
C	$30\,\mu$F	C	$470\,\mu$F
-		R_{ESR}	$50\,\mu\Omega$
L	$5\,\mu$H	-	
$I_{C,Ripple,RMS}$	4.6 A	$I_{C,Ripple,RMS}$	52 A

Based on the required output voltage ripple of maximum $300\,\mathrm{mV}_{pp}$ and a maximum inductor ripple current of $\pm 7.5\,\%$ for the LC-filter, the component values for the two topologies can be determined (cf. table III). The ripple current in the filter capacitor in the topology with capacitive filter is much higher than the one for the LC-filter. Applying electrolytic capacitors this high ripple current results in a large filter volume due to the relatively high ESR/low current carrying capability of electrolytic capacitors. This is shown in the second line of row "LC-Filter Size" in table IV. The first line represents the volume of the capacitor if just the capacitance value is considered and the ripple current is neglected. With the ripple current the capacitor volume increases more than by a factor of ten. Both values are based on the cuboid volume of cylindrical electrolytic capacitors.

TABLE IV
Comparison of LC and capacitive output filter with electrolytic or ceramic capacitors. For electrolytic capacitors two volumes are given: The first value gives the volume if just the capacitance value is realized - neglecting the ripple current I_{AC} and the current carrying capability of the capacitors. With the second value also the ripple current is accounted for. The inductor of the LC-filter has a volume of $40.9\,\mathrm{cm}^3$. for the ceramic capacitors also two volumes are considered: The volume "SMD-Device" is the pure volume of the ceramic capacitor and the volume "Mounted" also accounts for the volume of the PCB where the capacitors are mounted. There, a double sided, 1.5 mm thick board is assumed.

	Electrolytic		Ceramic	
	Cylindrical	Cuboid	SMD-Device	Mounted
$\mu\mathrm{F/cm}^3$	170	134	111	90
I_{AC}/cm^3	0.25 A	0.19 A	41.6 A	35.1 A
LC-Filter Size	μF only: **0.22** + **40.9** (L)		**0.32** + **40.9** (Inductor)	
in [cm^3]	I_{AC}: **24.2** + **40.9** (L)		(Max. I_{AC} <11.3 A)	
C-Filter Size	μF only: **3.7**, $I_{AC} < 1.5\,A$		**5.4**	
in [cm^3]	I_{AC}: **273** $\Rightarrow$ C=36 mF		(Max. $I_{AC} < 233$ A)	

If the capacitance is realized by ceramic capacitors the volume decreases down to $0.32\,\mathrm{cm}^3$ including ripple current considerations. In both cases the volume of the inductor ($40.9\,\mathrm{cm}^3$) is based on very compact commercially available inductors e.g. [16], [17]. Due to the large inductor volume the size of the LC-filter is relatively large and would consume approximately 10 % (including interconnection) of the volume if a power density of 10 kW/ltr. is assumed.

With a capacitive filter and ceramic capacitors the volume of the filter elements decreases down to $5.4\,\mathrm{cm}^3$ including the volume of the PCB for mounting and the maximum thermally possible ripple current increases to 233 A. A capacitive filter with electrolytic capacitors would result in a filter volume of $273\,\mathrm{cm}^3$ and a capacitance value of 36 mF if the ripple current is considered. Taking just the required capacitance value into account this volume decreases to $3.7\,\mathrm{cm}^3$.

Since with the capacitive output filter the volume of the filter is much smaller and the current in the secondary winding is lower, in the following only the resonant converter with capacitive output filter is considered in the optimization performed with the optimization procedure presented in the following section.

III. Optimization Procedure

After the topologies with the best potential for a high power density and a high efficiency have been identified, the components values must be chosen, so that the system volume becomes minimal and/or the efficiency maximal. Since the volume of the single components, which are mainly limited by the respective maximum operation temperature, interdepend to some extent on each other, the optimization of the overall volume/efficiency is a quite involved task with many degrees of freedom.

Therefore, an automatic optimization procedure is applied for determining the optimal component values of the telecom supply.

In Fig. 5 a possible flow chart of such a procedure is given, where the specification of the design parameters like the input and output voltage, the output power, temperature limits, material characteristic, etc. is the starting point of the procedure. These parameters as well as starting values for the

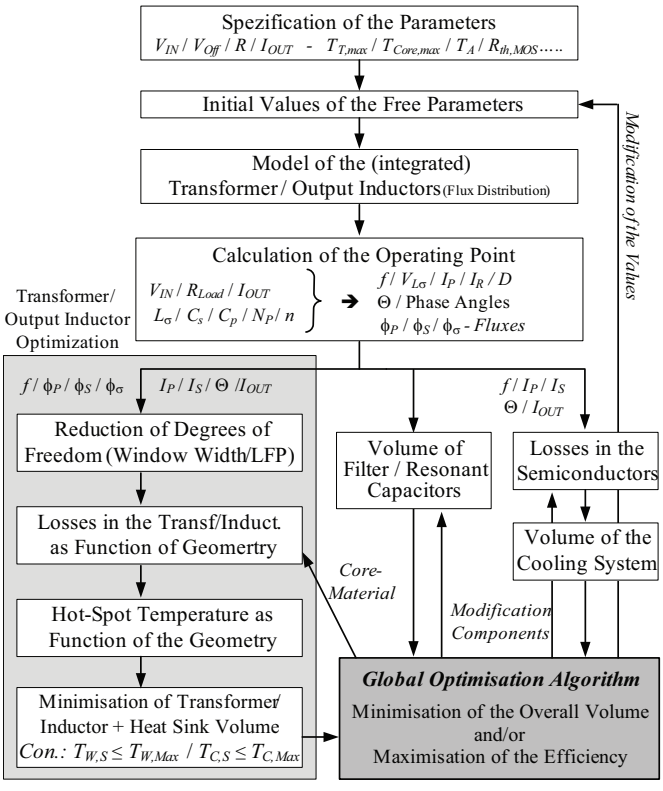


Figure 5. Automatic procedure for optimizing the volume/efficiency of a series-parallel resonant converter while keeping the device temperatures below given limits.

free parameters like N_P, N_S or C_S, C_P, L_S/L_{OUT} must be specified by the user.

Based on the values for the series/leakage respectively the output inductance and the turn numbers the magnetic components are modeled. In case of the phase shift converter the models mainly consist of analytic expressions for the flux distribution and the optimal thickness/diameter of the foil/wires for the windings [18]. For the resonant converter a reluctance model of the transformer with integrated series inductance is calculated. This model is combined with the converter model for calculating the flux distribution in the core [15], [19].

The converter model for the phase shift converters is based on analytic expressions with which the currents and the voltages as well as the duty cycle and the constraints for ZVS conditions are calculated. For the resonant converter first, the operating point of the dc-dc converter is estimated by an approximated fundamental frequency analysis [20]. With the estimated values the solution space for the analytic converter model [19] is restricted and the calculation time is reduced. The converter model is based on a set of equations which are derived with the extended fundamental frequency analysis [21] and solved numerically. The solution are the operating frequency, the voltages and currents as well as the flux distribution of the integrated transformer including phase information.

With the currents in the converter the switching and conduction losses of the MOSFETs and the rectifier diodes are determined. These losses, the ambient temperature and the maximum junction temperatures of the semiconductor devices are used for calculating the volume of the semiconductor heat sink including the fan based on the $CSPI$ (Cooling System Performance Index), which is defined by

$$CSPI\left[\tfrac{\mathrm{W}}{\mathrm{K\ ltr.}}\right] = \frac{G_{th,S\text{–}A}\left[\tfrac{\mathrm{W}}{\mathrm{K}}\right]}{Vol_{HS,Magn.}\,[\mathrm{ltr.}]} \tag{1}$$

and has been introduced in [3] ($G_{th,S\text{–}A}$ is the thermal conductivity of the heat sink). There, it is important to check the resulting volume of the cooling system, since with the scaling factor $CSPI$ quite small volume for the heat sink/fan can result, which are difficult to manufacture. A possible solution is to combine heat sinks which are on comparable temperature levels, so that one larger fan could be used for both heat sinks.

Besides the losses in the semiconductors also the volume and the losses in the resonant tank capacitors and/or the output capacitors are calculated with the voltages/currents. There, the losses in the capacitors must be limited to the maximum admissible values.

The volume and the shape of the transformer/inductor core and the two windings is determined in a second, inner optimization procedure (light gray shaded in Fig. 5). There, the volume of the transformer/inductor is minimized while keeping the temperatures below the allowed limits. For this purpose, first the geometrical degrees of freedom are reduced to 3 by determining the core window width using the optimal winding thickness and the turns number [20]. In case of transformers with integrated leakage inductance also the width of the leakage path (LFP) is fixed by setting the flux density in the leakage path to the same value as in the middle leg conducting the main flux.

Thereafter, the core and winding losses are calculated as function of the three remaining geometrical variables (a, b, d cf. Fig. 7(a)). With the losses and the thermal model of the transformer/inductor the temperature distribution in the core and the winding also could be calculated as function of the variables a, b and d. The peak temperatures in the windings and the core are together with the maximum allowed temperatures the constraints for the following minimization of the volume including the volume of cooling system for the magnetic device (cf. Fig. 7(b)). Furthermore, the variables $a - e$, defining the transformer/inductor geometry, can be restricted in order to preserve certain limitations resulting from the manufacturing process.

In the inner optimization loop it is also possible to maximize the efficiency of the transformer/inductor, if an upper limit for the volume is given.

Together with the volumes of the capacitors/heat sink the minimized transformer/inductor volumes are passed to the global optimization algorithm. This algorithm systematically varies the values of the free parameters until a minimal system volume or a maximal efficiency is obtained. This procedure is relatively fast/simple for the phase shift converters since the number of interdependencies is small, but in case of the resonant converter the models are complex and the calculation/computation effort is huge.

IV. Models

In the subsequent paragraphs the different models of the optimization procedure are explained shortly. First, the analytical converter model is derived, then the equations for the semiconductor losses and the model for the resonant tank capacitor volumes. Finally, the loss equation and the thermal model of the transformer are presented.

A. Analytical Converter Model

With the analytical converter models the currents and the voltages as well as the operating point (duty cycle, frequency, phase shift, etc.) for the phase shift full bridge with current doubler or center tapped transformer and the series-parallel resonant converter with capacitive output filter are calculated.

In case of the series-parallel resonant converter (cf. Fig. 4(b)) the models are partly based on the extended fundamental frequency analysis (E-FFA) proposed in [15], [19], [21], where the currents and voltages are represented by their fundamentals as shown in Fig. 6. In the model also the control method described in [15] with ZVS condition in one leg and ZCS condition in the other leg as well as control by frequency and duty cycle is considered in the equations. This control method reduces the switching losses significantly.

For the resonant converter with purely capacitive output filter the E-FFA has been improved so that not only the fundamental component is considered but also the third harmonic,

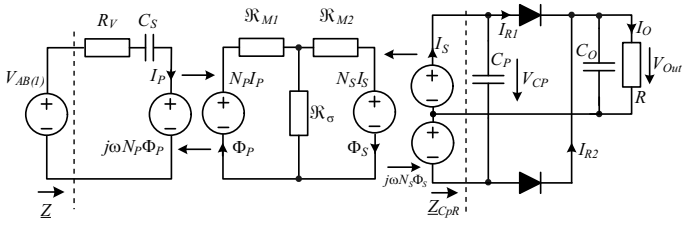


Figure 6. Equivalent circuit of the series-parallel resonant converter with capacitive output filter.

since it influences the behavior of the converter significantly. Thus, both the primary resonant current I_P and the secondary resonant current I_S are sinusoidal with a superimposed third harmonic component. Furthermore, it is assumed that the output voltage is constant and that the components are ideal. The major procedure of the analysis is to determine the impedance Z_{CpR} of the parallel connection of C_P and the rectifier at first. With this impedance the input impedance Z of the resonant circuit, seen by the H-bridge / voltage source V_{AB} (cf. figure 6), could be calculated. In the impedance Z also the reluctance model of the transformer is included.

In the next step two equations for each harmonic can be set up. The first one describes the relation between the phase shift of the primary current I_P and the fundamental component of the H-bridge voltage $V_{AB(1)}$, which is determined on the one hand by the duty cycle D and on the other hand by the impedance Z. The second expression relates the input impedance of the resonant tank to the amplitude of the resonant current. These equations are derived in [19] and are solved numerically in the optimization procedure.

B. Semiconductor Losses

For calculating the volume of the heat sink for the semiconductors with (1) the maximum operating temperature and the thermal resistance between junction and heat sink of the semiconductors are required. These values can be derived from the data sheets of the applied semiconductors. Furthermore, the losses in the 4 MOSFETs including antiparallel diode and the 2 rectifier diodes must be calculated. Based on the currents calculated with the converter models the RMS currents in the MOSFETs and the resulting conduction losses can be calculated. There, it is assumed that always one MOSFET per leg is turned on, so that the current does not flow via the antiparallel diode but in reverse direction through the MOSFET.

For the rectifier diodes an approximately constant forward voltage drop is assumed, so that the conduction losses can be calculated with the average currents. The switching losses of the diodes are neglected since it is assumed that Schottky diodes are used.

Due to the ZVS condition the switching losses can not be calculated based on data sheet information. Instead measurements, which have been performed with the applied APT50M75 MOSFETs from Microsemi (former Advanced Power Semiconductors) [20], are used in the optimization procedure. Based on these measurements the losses per MOSFET can be determined by

$$P_{ZVS}[\mathrm{W}] = \left(1.9^{e-7} I_{Off}^2[\mathrm{A}] - 3.8^{e-6} I_{Off}[\mathrm{A}] + 1.4^{e-5}\right) f[\mathrm{Hz}]$$

in case the current turned off by the MOSFET is

$$I_{Off} \geq 15\,\mathrm{A}$$

and they are negligible if the current I_{Off} is below 15 A.

With the applied control method one leg of the resonant converter would switch at ZCS condition. However, if the ZCS leg, which should switch at the zero crossing of the resonant current, is switched slightly before the zero crossing, the MOSFET has to turn off a small current. Because of the fast switching and the large output capacitance of the MOSFET this current does not cause relevant turn off losses. In case the turned off current is large enough, so that it charges the MOSFET capacitances during the interlocking delay [15], the opposite MOSFET is turning on at zero voltage. Consequently, the switching losses in the ZCS leg are negligible [20].

With the explained approaches the semiconductor losses can be calculated and the heat sink temperature and volume (cf. (1)) can be determined so that the maximal junction temperature is not exceeded. For the efficiency calculation also the losses in the gate drive circuits, which can be calculated with the gate-charge/capacitance and which increase linearly with frequency, must be considered.

C. Resonant Tank Capacitors

The capacitors of the resonant tank and the capacitive output filter are carrying high frequent currents with a relatively high amplitude. In order to limit the losses and the temperature rise dielectrics with a low loss factor $\tan\delta$ are required. There are basically two good choices: either foil capacitors with polypropylene or ceramic capacitors with COG/NPO material. Since the resulting volume with foil capacitors is significantly larger than for ceramics as could be derived from data sheets, the latter are chosen for the considered telecom power supply.

For calculating the volume required for realizing the series and parallel capacitor a commercial 3.9 nF/800 V COG ceramic capacitor in a 1210 SMD housing from Novacap [22] has been chosen as reference component, since it offers the highest capacitance per volume ratings at AC voltages with a high frequency and amplitude. Based on this capacitor the resulting volume could be calculated by scaling. There, also the volume for mounting the components on a double sided PCB is considered in the optimization procedure.

In case of the filter capacitor a 2.2 μF/100 V X7R ceramic capacitor in a 1210 housing manufactured by muRata [23] is used as reference element. The capacitance value is calculated with the currents based on the maximum allowed ripple voltage of 300 mV_{pp} at the output.

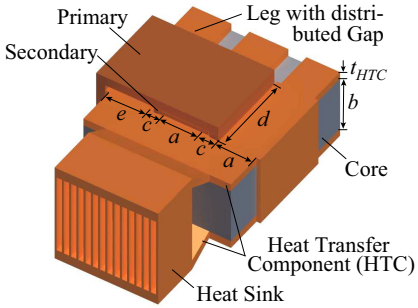
With the currents also the losses in the capacitors can be determined with the loss factor. These are compared with the maximal allowed values, which can be derived by the loss limit of 0.35 W per 1210 housing at 40 °C ambient temperature and 125 °C maximal dielectric temperature. There, also the decrease of the capacitance with temperature and DC voltage is considered in the optimization procedure.

D. Transformer Model

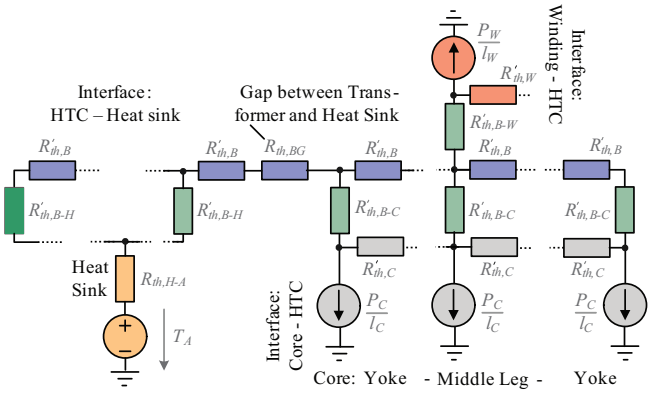
In the optimization procedure shown in Fig. 5 also the shape of the transformer is optimized for minimal volume in the inner loop while the hot spot temperatures are kept below the limits. For this inner optimization loop the volume, the losses and the temperature distribution in the transformer are needed as function of the geometry. The geometry could be described by 5 variables as shown in Fig. 7(a), where the construction of the transformer and the definition of the variables are given. There, it is assumed that copper foil is used for realizing the primary and secondary winding, since the thermal resistance between the winding layers is lower. Furthermore, per layer only one turn is realized.

In Fig. 7(a) a transformer with integrated leakage inductance is shown [24], where the secondary winding encloses the middle leg and the primary winding the middle and one outer leg, which conducts the leakage flux. This type of transformer is used in the resonant converter and in the phase shift converter with capacitive output filter. In case of the phase shift converter with CDR a transformer where both windings just enclose the middle leg is assumed. There, the required series inductance is integrated by spatial separation of the windings.

In order to maximize the power density of the transformer an advanced cooling method as described in [2] has been applied. With this method the losses in the windings and the core are transferred via a heat transfer component (HTC) to an additional heat sink for the transformer.



(a) Transformer with integrated cooling



(b) Thermal model of transformer with HTC

Figure 7. (a) Geometry of transformer with integrated series inductance and heat transfer component (HTC) / heat sink for cooling. Parameters a, b and d are the degrees of freedom in the optimization. (b) Distributed thermal model of the cooling system shown above with the heat sink on the left hand side, a gap between heat sink bridged by the HTC and transformer and the transformer with winding on the right hand side.

For calculating the temperature rise the losses in the windings and the core are required. There, the winding losses are calculated by a 1D approach, which includes skin- and proximity effect losses, and the thickness of the foil is optimized as described in [18]. The core losses are calculated by the approach presented in [25], which is based on Steinmetz parameter [26] and on the rate of magnetization (dB/dt).

With the losses the temperature distribution in the transformer could be calculated based on the thermal model shown in Fig. 7. This model describes the heat flow from the winding/core via the thermal interfaces and HTC to the heat sink/ambient by distributed thermal resistances (R_{th} per length). The calculation of the temperature profile is based on transmission line equations, what is described in detail and validated in [2].

For improving the heat flow within the windings made of foil and also from the winding to the HTC a thermally conductive insulating material is used [27]. Moreover, thermal grease between the core and the HTC and a cover pressing the winding on the HTC are used. This cover is not shown in Fig. 1 and Fig. 7(a).

After the volume has been minimized it is passed to the global optimization algorithm, where it is used for calculating the system volume and for varying the parameters systematically.

V. Calculation Results

Based in the presented procedure shown in Fig. 5 the three considered topologies have been optimized for a telecom supply with the specification given in table I. The results presented below are based on the following components/limitations if not stated differently:

- Core material: N87 from Epcos ($T_{Max} \leq 115\,°C$)
- Windings: Foil windings ($T_{Max} \leq 125\,°C$)
- Center tapped secondary winding
- MOSFETs: APT50M75 from Microsemi (former APT)
- Rectifier diode: APT100S20 from Microsemi
- Capacitors C_S and C_P: Reference 3.9 nF 800 V COG series from Novacap
- Cooling system performance index: 23 (for transformer and semiconductor heat sink)
- Maximal junction temperature $T_{j,max} \leq 140\,°C$

A further requirement is the overall height of the supply which should be below 1 U (≈44 mm). That significantly influences the design of the transformer/inductors (especially the height b - cf. Fig. 7(a)) as well as the cooling system.

In Fig. 8 the characteristic of the power density and the efficiency as function of frequency are shown. The maximal achievable power density is 19.1 kW/ltr. for the resonant converter and 15 kW/ltr. / 11.7 kW/ltr. for the phase shift converter with capacitive output filter/current doubler (1 kW/ltr. = 16.4 W/inch^3). There, only the net volume of the components including PCBs/housings is considered. The volume between

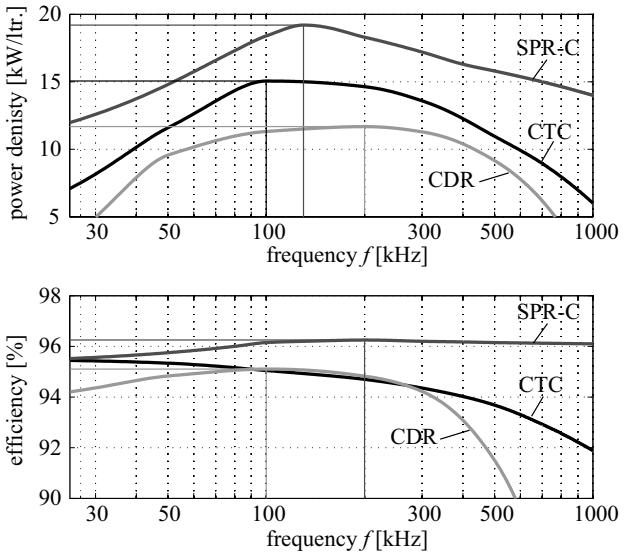


Figure 8. a) Power density and b) efficiency of the phase shift converter with capacitive filter (CTC) and current doubler (CDR) and series-parallel resonant converter with C-Filter (SPR-C) in dependency of switching frequency.

the components required for mounting/insulation and due to not fitting housings (e.g. cube type and cylindrical shapes) is not considered, since it depends significantly on the 3D arrangement of the components and the design of the supply. This volume adds significantly to the total converter volume, so that the resulting power density is lower than calculated here. In case of the resonant converter shown in Fig. 1 the calculated power density is 15 kW/ltr. and the power density of the final system is 10 kW/ltr. If a similar scaling factor is assumed for the three optimized converter topologies, 12.7 kW/ltr. (SPR-C), 10 kW/ltr. (CTC) and 7.8 kW/ltr. (CDR) would result for the power density.

The efficiencies at the operating point with maximal power density are 96.2 % for the resonant converter and 95 % / 94.8 % for the CTC / CDR as shown in Fig. 8(b). At the operating point with minimal losses an efficiency of 96.3 % at a switching frequency of approximately 220 kHz could be reached with the resonant converter. There, the switching frequency is higher than at the operating point for maximal power density, since the losses of the passive components reach a minimum at this frequency. Due to the increased volume for the semiconductor heat sink this operating point results only in a power density of 17.1 kW/ltr.

In case of the phase shift converter with capacitive output filter the maximal efficiency is achieved at the lowest considered operating frequency of 25 kHz. There, the CTC reaches 95.4 %. The maximal efficiency for the CDR is 95.1 %, which is achieved at 100 kHz.

In Fig. 9 the distributions of the volumes on the magnetic devices (transformer and inductor), the capacitors (resonant tank and output), the heat sink for the semiconductors and the remaining components like housings, control board or gate drive for the three topologies are shown. There, it could be seen that with rising switching frequency the volume of the semiconductors' heat sink is increasing due to rising switching

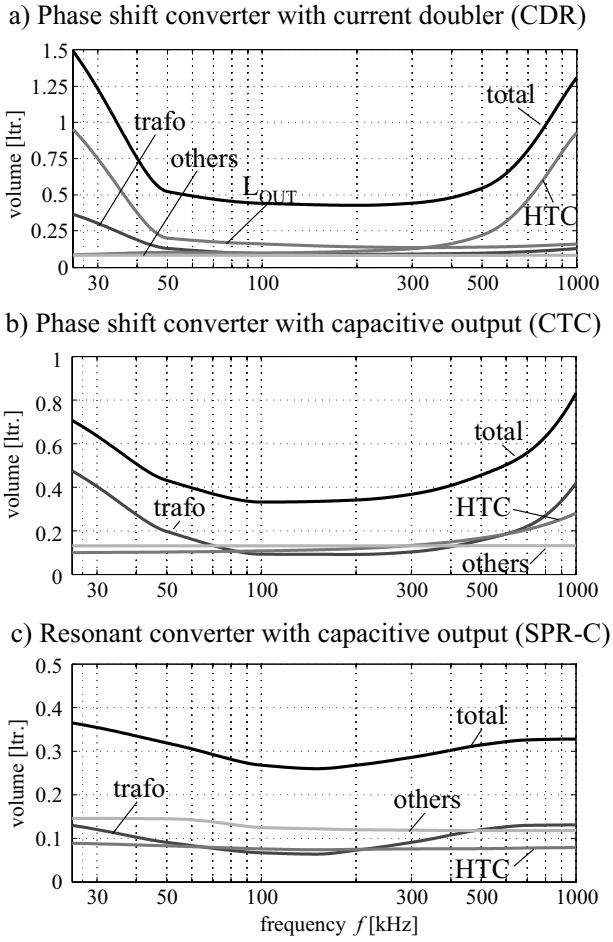


Figure 9. Volume vs. frequency for the phase shift converter with a) current doubler (CDR), b) capacitive filter (CTC) and c) series-parallel resonant converter with C-Filter (SPR-C), split in transformer, heat sink and components volume including output capacitor.

losses. The shape of the volume distribution as function of frequency is strongly determined by the passive components,

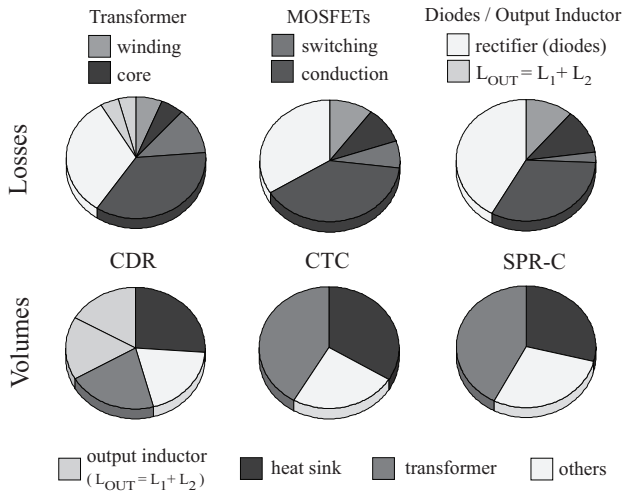


Figure 10. Distribution of the losses and volumes of the phase shift converter with capacitive filter (CTC) / current doubler (CDR) and series-parallel resonant converter with C-Filter (SPR-C).

TABLE V
Resulting specification of the optimized 5 kW telecom supplies. There, the losses in the two inductors of the CDR are 2×10.9 W, the AC flux density is 77 mT and the inductance is 6.7 μH. (In brackets: simulated values including more parasitic elements than considered in the analytic model.)

	Phase Shift		Resonant
	Current-D.	Cap.-Filter	Cap.-Filter
Power Density	11.7 kW/ltr.	14.7 kW/ltr.	19.1 kW/ltr.
Operating Point			
• Frequency	200 kHz	100 kHz	135(129) kHz
• Duty Cycle	0.81(0.86)	0.82(0.88)	0.78(0.83)
• Efficiency	94.8 %	95 %	96.2 %
Transformer			
• Winding Losses	16 W	24.6 W	21.9 W
• Core Losses	13.8 W	23.7 W	23.5 W
• Turns Ratio	11:4	11:2	14:2
• Winding Temp.	125 °C	124 °C	125 °C
• Core Temp.	107 °C	115 °C	115 °C
• Flux Density	175 mT	240 mT	300 mT
Semiconductors			
• $P_{V,SW,MOSFET}$	31.2 W	17.8 W	5 W
• $P_{V,Cond,MOSFET}$	93.7 W	96.8 W	64 W
• Rectifier Losses	83.3 W	83.3 W	83.3 W
• Heat Sink Temp.	125.1 °C	125 °C	130.8 °C

which define a frequency range from app. 100 kHz. . .300 kHz of high power density. Outside this range the volume of the magnetic devices and at higher frequencies also the volume of the semiconductor heat sink rises significantly, what limits the achievable power density.

A more detailed distribution of the volume and also of the losses of the three considered topologies is given in Fig. 10. There, the volume and the losses of the magnetic devices, the capacitors, the semiconductors/heat sink and the remaining components for the operating point with maximal power density is presented. Further details are shown in table V.

The relatively low optimal operating frequency for maximal power density results, since the whole system is considered in the optimization. In case only the transformer for a fixed input voltage/current level would be considered the optimal operating frequencies for maximal power density of the transformer would be (significantly) higher.

A. Power Density Barriers

In the preceding paragraph the power density values for available components/technologies have been presented. Now, the influence of different parameters on the achievable power density is investigated. In table VI the achievable power density and efficiency for the phase shift converter with capacitive output filter is shown for different parameter variations. First, it is assumed that the maximal allowed junction temperature is increased from 150 °C to 200 °C (e.g. by applying SiC switches and appropriate packaging) – the remaining parameters are not modified. By this means the volume of the semiconductor heat sink significantly decreases, so that a power density of 17.1 kW/ltr. (before 14.7 kW/ltr.) could be achieved. There, it is important to note that with the heat sink also the size of the area for mounting the semiconductors is shrinking. Consequently, the thermal resistance between the semiconductors and the heat sink increases, so that the gain in power density is very limited. This effect has not been considered in table VI.

TABLE VI
Influence of device parameters/max. allowed temperatures on maximal achievable power density for the phase shift converter with capacitive output filter. The maximum remains at a switching frequency of app. 100 kHz, except for case 5 where all improvements are considered at the same time. There the optimal switching frequency rises to approximately 200 kHz.

	Parameter	Old Value	New value	New Density/Eff.
1	Junction Temperature	150 °C	200 °C	17.1 $\frac{\text{kW}}{\text{ltr.}}$ 95 %
3	$R_{th,MOSFET}$ $R_{th,Rectifier}$	0.22 $\frac{\text{K}}{\text{mW}}$ 0.2 $\frac{K}{mW}$	0.11 $\frac{\text{K}}{\text{mW}}$ 0.1 $\frac{K}{mW}$	16.1 $\frac{\text{kW}}{\text{ltr.}}$ 95 %
2	Winding / Core Temp.	125 °C 115 °C	150 °C	16.8 $\frac{\text{kW}}{\text{ltr.}}$ 94.9 %
4	$P_{Switching}$	P_{SW}	$\frac{1}{2}P_{SW}$	15.9 $\frac{\text{kW}}{\text{ltr.}}$ / 95.2 %
5	$V_{F,Rectifier}$	0.9 V	0.45 V	17 $\frac{\text{kW}}{\text{ltr.}}$ / 95.8 %
6	1+2+3+4+5	-	-	21.6 $\frac{\text{kW}}{\text{ltr.}}$ / 96.3 %

In the second row of table VI it has been assumed that the thermal resistance between the chip and the heat sink is decreased. Again, this measure allows to shrink the volume of the semiconductor heat sink, since its temperature could be increased. There, the power density rises up to 16.1 kW/ltr. By increasing the operating temperature of the transformer a value of 16.8 kW/ltr. could be reached. There, the rising copper losses due to the rising resistivity limit the gain of power density.

Another option would be to decrease the switching losses by 50 %. Due to the ZVS condition this measure only results in small increase of the power density to 15.9 kW/ltr. A bigger step could be achieved by reducing the forward voltage drop of the rectifier diodes by a factor of two, what results in a smaller volume of the heat sink. This would lead to a power density of 17 kW/ltr. and an efficiency of 95.8 %. A reduction of the conduction losses of the rectifier could be achieved by synchronous rectification. The $R_{DS,on}$ of the applied MOSFETs, however, must be very low – in the considered case ≈8 mΩ@125 °C for cutting the losses in half. Since the rectifier diodes and their heat sink are already quite small, a synchronous rectifier would not help to improve the power density but only the efficiency.

In case all measures are combined a power density of 21.6 kW/ltr. and an efficiency of 96.3 % can be achieved. Similar improvements can be expected for the other systems in case the same measures are taken.

Summing up, this leads to two possible ways to improve the power density:

- For components users / supply manufacturers
  - Improve the thermal coupling between the semiconductors and the heat sink (e.g. by low temperature soldering) and

  - apply advanced cooling methods for the passive components [2].
- For device manufacturers
  - Further reduce the conduction losses of the power semiconductors,
  - reduce the magnetic materials HF losses,
  - decrease the thermal resistance between chip and housing/base plate,
  - increase operating temperatures.

VI. Conclusion

In this paper three topologies for telecom supplies – a phase shift converter with capacitive output filter and with current doubler and a series-parallel resonant converter with capacitive output filter – have been optimized with respect to power density. There, maximal 12 kW/ltr. (19 kW/ltr. pure component volume) are obtained for the series-parallel resonant converter (SPR). The optimal operating frequency with respect to the power density is approximately 135 kHz. For the phase shift converter 10 kW/ltr. result for a capacitive output filter (CTC) and 7.8 kW/ltr. for a current doubler (CDR). Again, the optimal operating frequencies are relatively low – approximately 100 kHz for the CTC and 200 kHZ for the CDR. There, the efficiencies are 96.2 % for the SPR, 95 % for the CTC and 94.8 % for the CDR. These values slightly improve ($\approx 0.8\,\%$) if the converter is optimized for efficiency, but there the power density decreases significantly.

The presented optimizations have been performed for operation at nominal output power – part load efficiency, soft switching range, costs or EMI issues, etc. have been neglected. In case also these constraints are also considered the achievable power density will decrease to approximately 6-8 kW/ltr. for the resonant converter. In combination with a PFC converter with a power density of also 6-8 kW/ltr. a system power density of 3-4 kW/ltr. for an air cooled supply would result.

For increasing the power density especially the thermal management is decisive. A direct cooling of the magnetic components as presented in [2] or improving the thermal resistance between the chip and the heat sink by low temperature solders, which could replace the thermal grease, are effective measures to reduce the system volume. Semiconductors with reduced losses or improved core materials are other possibilities to increase the power density and efficiency. These approaches, however, can only be followed by device/material manufacturers and are not directly accessible to supply manufacturers.

The largest gain results from optimizing the system parameters for the given specifications. The question which topology should be applied is important but does not influence the achievable power density as much as the optimization.

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