Accurate Measurement of the Switching Losses of Ultra High Switching Speed CoolMOS Power Transistor / SiC Diode Combination Employed in Unity Power Factor PWM Rectifier Systems

Gerold LAIMER
+41-1-632-7447
laimer@lem.ee.ethz.ch

Johann W. KOLAR
+41-1-632-2834
kolar@lem.ee.ethz.ch

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
ETH-Zentrum/ETL/H22
CH-8092 Zurich/SWITZERLAND

Abstract. The topic of this paper is a detailed analysis of the switching behavior of a CoolMOS / SiC diode combination applied in a 3.5kW single-phase unity power PWM rectifier system. The focus is on the development of guidelines to accurate measure the switching behavior and the turn-on and turn-off power losses at high switching speeds. Further subjects are the improved design of the power circuit, and the comparison of two high bandwidth current measurement methods applied in the power circuit.

1 INTRODUCTION

Modern boost-type single-phase telecom power supply modules are designed for a rated output power of typically $P_{O,max}$ = 800V · 4.4A = 3.5kW with a power density of approx. 3kW/dm^3. In future power supply systems an increasing power density of up to 10kW/dm^3 is intended. The passive components like inductors and capacitors normally require a large amount of space. Therefore a reduction in size of the passive components is achieved by increasing the switching frequency of the system in order to reach the desired power density.

Associated with the ultra high switching speed is a transient turn-off overvoltage, due to high di/dt-rates of currents passing through parasitic wiring inductances of the power circuit layout. Also, contributing to the high du/dt-rates are high current peaks caused by the charging of parasitic capacitances (i.e. coupling capacity of inductors). Besides this, the ultra high switching frequency increases the power transistor turn-on and the turn-off losses.

The combination of Infineon CoolMOS power transistor with its low resistance in the on-state and the Silicon Carbide Schottky diode (SiC), which has no reverse recovery current, are well suited for this application. Therefore an extremely high switching speed can be achieved, typically in the range of a few nanoseconds.

An accurate analysis of the switching behavior of the power circuit, and an estimation of the switching losses with sufficient precision, requires advanced measurement instruments. Particular, the different propagation delay of the voltage and the current waveforms has to be taken into account. Yet another important point is the utilization of a differential voltage probe with a very high common mode rejection ratio.

In this paper a boost-type single-phase power circuit (**Fig.1**) has been chosen for the characterization of the switching behavior and the determination of the switching losses.

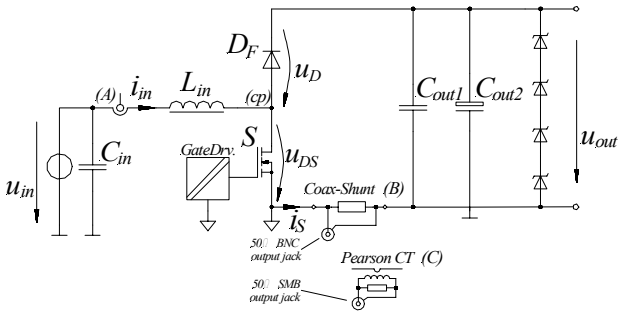


Fig.1: Basic structure of the power circuit of a single-phase boost-type unity power factor rectifier. The output voltage is limited to a maximum value of $u_{out} = 400V$ by four zener diodes connected in series. Each of the zener diodes has a breakdown voltage of 100V with a maximum admissible power dissipation of 1W. The input voltage is in the range of $u_{in} = [5V...40V]$.

Part	Type
S	Infineon SPW47N60C2
D_F	Infineon SDB06S60
Cin, Cout1	Arcotronics MKP C.4A 600V/2.2µF
Cout2	EPCOS 450V/470µF snap in
Lin	38µH helical wound choke with Core material SIEFERRIT N87
(A)	LEM LA-55P
(B)	T&M Research SDN-414-10 Resistance value: 100mΩ
(C)	Pearson: Model 2877 Sensitivity: 1.0V/A $i \cdot t$ Capability: 400µAs

Tab.1: List of components, which have been selected for the test arrangement of the power circuit.

In **section 2** the equipment for high bandwidth voltage and current measurement is shown. The electrical and time behavior of the equipment is listed in tabular form. A comparison of the performance of a coaxial-shunt (T&M

Research) and AC current monitor (Pearson) is given. Also the advantages and disadvantages of the two current measurement methods are discussed. Furthermore, a comparison between voltage and current probes of two different manufacturers is given. The calibration process for accurate voltage and current measurement will be shown. **Section 3** shows the considerations concerning the gate drive unit and the mechanical construction of the power circuit. **Section 4** shows the switching behavior of the boost-type power circuit depicted in **Fig.1**. Also the measured result of the turn-on and turn-off switching losses will be discussed. The influence on the measured results of the propagation delay of different channels is presented. **Section 5** discusses the advantages and disadvantages of surge current measurement setups. Improved design features of the power circuit and the input inductor will be given. In addition the influence of higher switching speeds on switching losses and associated EMI problems (increasing filtering effort) will be discussed.

2 EQUIPMENT FOR HIGH BANDWIDTH VOLTAGE AND CURRENT MEASUREMENT

The primary limitations of oscilloscope systems are insufficient range of input voltage, limited bandwidth and different channel signal propagation delay. The voltages to be measured go up to a few hundred volts. A high voltage passive probe or a voltage differential probe has to be used to divide the voltage down to the input voltage range of the oscilloscope (with a typically attenuation of 10:1 or 100:1). Furthermore, the voltage probes are heavily stressed with voltage slew rates of up to 40kV/µs.

To obtain an accurate measurement it is therefore necessary to use high performance voltage and current measurement instruments. Both the voltage differential and the current channels should have upper-bandwidth capabilities beyond the highest frequency contained in the signals being measured. An approximation of the minimum bandwidth a voltage or current probe should have is explained in the following:

When an input signal feeds the series connection of voltage probe and vertical amplifier, as in **Fig.2**, the rise time of the result is

$$t_{rise,composite} = \sqrt{t_{r,signal}^2 + t_{r,probe}^2 + t_{r,amp}^2} \ . \qquad (1)$$

This equation relates the rise time of a complete system $t_{rise,composite}$, to the rise time of each of its parts. When cascading systems together, their impulse response convolve. The properties of the convolution operation therefore determine how the complete system behaves. Whenever stages are connected in series the square of the composite rise time is equal to the sum of the particular squared rise times **[3]**.

Conversion between bandwidth and rise time may be made according to the principle that, for each signal type (Single-Pole Pulse, Two-Pole Critically Damped Pulse, Gaussian Pulse), the product of bandwidth and rise time is constant.

For example, the product of 3-dB bandwidth and 10-90% rise time for a gaussian impulse response is

$$F_{3dB} t_{10-90} \cong 1/3 \ . \qquad (2)$$

The 3-dB bandwidth (the scope manufacturer commonly quotes performance in terms of system bandwidth) can be converted to a 10-90% rise time by

$$t_{10-90} \cong 0.35 / F_{(-3dB)} \ . \qquad (3)$$

Dividing 0.35 by the expected rise time of the fastest voltage waveform to be measured will give a good estimation of the maximum bandwidth of the waveform. The instrumentation should exceed this bandwidth by a factor of three.

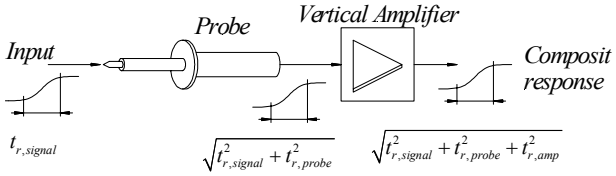


Fig.2: Composite rise time of the series connection of voltage probe and oscilloscope. The bandwidth of the probe and the oscilloscope vertical amplifier should exceed the bandwidth of the signal to be measured by a factor of three.

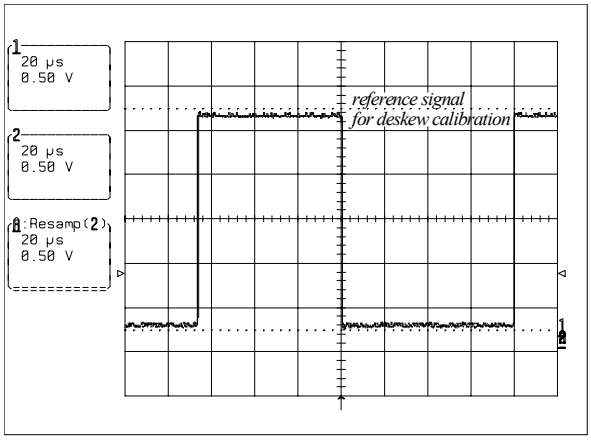
Accurate measurement of instantaneous power loss in switching power transistors and power diodes requires sophisticated instruments to acquire waveform data, as well as signal processing software to analyze the waveforms. There are different approaches to do the power loss measurement.

One approach is to use a Digital Storage Oscilloscope (DSO) with math waveform processing tools that can acquire and simultaneously display the power loss. The DSO does this by multiplying the data points of the voltage across and the data points of the current through the device under test to yield a waveform that represents power.

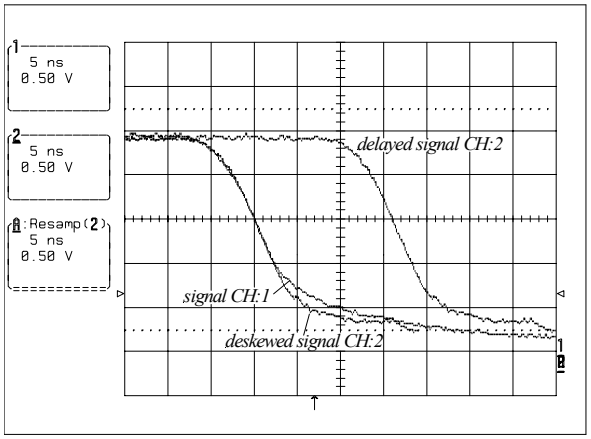
To accurately perform the required waveform math, both the voltage and the current waveforms need to be sampled instantaneously by the DSO. Due to the differences in the voltage and current signal path lengths, and delays introduced by the probes, the current and voltage waveforms can be time-skewed relative to each other. The multiplication of data pairs that are not time-coincident leads to an incorrect power waveform.

Therefore it is mandatory to compensate the time differences between channels. To determine the amount of time delay between channels, one must calibrate the system before doing the measurement. In **Fig.3** the procedure to correct the time-skew in the current and the voltage waveforms is shown.

The current and the voltage probe are connected to the same high slew rate pulse reference signal. The measured waveforms show a delay with respect to each other which can be compensated by the deskew capability of the oscilloscope. In this particular setup, the time delay between current and voltage waveforms is about 15.2ns, which is mainly caused by the voltage differential amplifier.



a)



b)

Fig.3: Both the current and the voltage probe are connected to a pulsed reference signal **a)**. The measurement indicates that the voltage in channel 2 is delayed by about 15.2ns with respect to the current signal in channel 1 **b)**. The correction of the time skew difference between the current and voltage channels can be adjusted by the scopes deskew capability.

2.1 Voltage Probes

The major criterions for the voltage probes are common mode rejection ratio (CMRR), and the frequency bandwidth. A specification of the CMRR of different probes is given in **Tab.2**.

In order to obtain a qualitative behavior of the voltage differential probes they were stressed with a common mode voltage switched from 0V to 300V, with a slew-rate of approximately 10V/ns.

The common mode stress of the voltage differential probes TEK P5205 and LeCroy ADP305 showed a signal with a peak-to-peak voltage amplitute of ±100V!

The same measurement has been carried out with the passive voltage differential probe DXC100A used with the DA1855A differential amplifier.

There, the peak-to-peak amplitude of the measured signal was in the range of ±15V.

If a current transformer is utilized for the current sensing (which provides a galvanic insulated current signal), a single-ended passive high voltage probe can be used, with the advantage of a higher bandwidth limit.

Specs	**P5205 (Tektronix)**	**ADP305 (LeCroy)**	**DXC100A/D1855A (LeCroy)**
BW(-3dB)	100MHz	100MHz	250MHZ
Rise time	-	-	<3.5ns
CMRR	50dB @ 1Mhz	50dB @ 100kHz	100dB @ 100kHz
Rin/Cin	4M/7pF	8M/6pF	1M/10.5pF
CM range	1000V RMS	1000V RMS	500VDC + pk AC

Tab.2: List of oscilloscope voltage probes used for the measurements. The clamp on differential voltage probe P5205 (Tek) and the ADP305 (LeCroy) do not meet the requirements in terms of CMRR and rise time. Only the differential voltage probe DXC100A in conjunction with the D1855A differential amplifier meets the requirements.

2.2 Current Probes

The oscilloscopes current probes (clamp-on probes, probes with external amplifier) were not utilized for the current measurements because of the limited bandwidth, and the mechanical construction that is necessary to insert the probe into the current path of interest. This increases the wiring inductance of the power circuit.

The current probes are mentioned at this point for the sake of completeness.

Specs	**CP015 (LeCroy)**	**TCP202 (Tektronix)**	**P6312/AM503B (Tektronix)**
BW(-3dB)	50MHz	50MHz	100MHZ
Rise time	<7ns	<7ns	<3.5ns
prop. delay	-	17ns	17ns
Imax	15A	15A	20A
Ipeak	50A (<10µs)	50A	50A
Insertion Impedance	0.5Ω @5MHz	0.1Ω @5MHz	0.2Ω @50MHz 1Ω @100MHz

Tab.3: Oscilloscope current probes. The CP015 and TCP202 are clamp-on current probes without external power supply. The P6312 current probe in conjunction with the probe amplifier AM503B is the state of the art current probe for measurement applications from DC to MHZ.

2.3 Oscilloscopes

Besides the sufficient bandwidth the oscilloscope has to provide a deskew capability to compensate time-delays in the acquired voltage and current waveforms relative to each other.

Specs	**WavePro 950 (LeCroy)**	**TDS7104 (Tektronix)**
BW(-3dB)	1GHz	1GHz
Sample-rate @1Channel	16GS/s	10GS/s
Deskew capability	±2µs	±25ns

Tab.4: Oscilloscope utilized for the measurements of the switching behavior and the switching losses.

2.4 Current Viewing Resistor - Coaxial Shunt

A current viewing resistor (CVR) has a number of advantages that are presented in this section.

The insertion into the current path of interest poses no mechanical problems. The CVR provides a direct image of the current through the resister, and the sensor is capable of determining very high surge currents. A standard BNC connector provides a direct connection to a scope by via a 50Ω coaxial cable.

A particular feature is the extremely flat frequency response from DC to 2GHz. Therefore the sensor is ideally suited for surge current measurement applications. Furthermore, the sensor has no offset and no auxiliary power supply is needed.

One disadvantage of the sensor is that it does not provide a galvanic isolation that excludes the concurrent utilization of a voltage probe attached to a different voltage level (a differential voltage probe with a lower bandwidth compared to a single-ended voltage probe has to be used instead).

Another disadvantage of the CVR is the limited pulse energy capacity, which is defined by

$$E_{\max} = R_{Shunt} \int_{\tau_P} i^2 dt \,. \qquad (4)$$

An energy input into the shunt must not exceed the maximum value $E_{\max}$.

2.4 Pearson AC current monitor

The Pearson current monitor is a premium high bandwidth AC current transformer with a signal rise time of up to $t_r = 2ns$.

The lower bandwidth limit is basically determined by three parameters which are the number of secondary windings, the value of the burden, and the cross sectional area of the magnetic core.

The upper bandwidth limit is essentially dependent on parasitic effects (coupling capacity, core losses) and is in the range of up to 200MHz.

The sensitivity of the current sensor is a function of the number of secondary windings and the value of the burden. An important parameter of a current transformer is the $\int idt$ capability. If this value exceeds, the core material of the transformer runs into saturation.

Another advantage of the current transformer is the galvanic isolation of the sensed signal and the high current limit. Surge currents (in case of a short circuit) are not able to damage the sensor.

A disadvantage of the current transformer is the inability to sense DC currents.

3 GATE DRIVE UNIT AND MECHANICAL CONSTRUCTION OF THE TEST CIRCUIT

To get the desired performance of the system, several important points have to be considered. In particular, the layout of the power circuit, the mechanical design of the input inductor, and the galvanic isolation of the gate drive unit.

The switching speed of the CoolMOS can be defined with the value of the gate series resistor. An arbitrary adjustment of the turn-on and turn-off speed of the power transistor is accomplished by using different values for the turn-on and turn-off gate resistor in conjunction with a diode. The values of the gate resistors were determined experimentally during the measurements. To find an appropriate value for the gate resistors one has to consider the higher excitation of high frequency ringing between parasitic elements in the power circuit at a higher switching speed (EMI problems increase). Therefore a compromise has to be found between the reduction of switching losses, and the increased high frequency ringing that accompanies increased switching speed. Turn-off overvoltage is not an issue (a proper layout of the power circuit assumed).

A detailed analysis of the switching behavior is shown in section 4.1.

3.1 Gate Drive Unit

The gate drive unit is stressed with very high du/dt-rates (up to 40kV/µs). A galvanic isolation of the gate drive electronic from the control electronic, which is sensitive to noise currents, has to be made in order to avoid failures. The control signal and the power to the gate drive are separated.

The power supply for the gate drive is built with a DC/DC converter (250kHz switching frequency). A very important point is to keep the coupling capacity between the primary and secondary winding as low as possible in order to avoid charge current peaks due to high du/dt-rates across the coupling capacity.

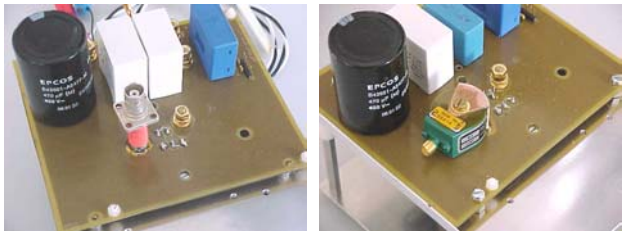
The galvanic isolated transmission of the gate signals has been achieved by using optical plastic fibers with a wavelength of 650nm.

3.2 Mechanical construction

A utilization of oscilloscope current probes in the measurement is not recommended because of two major reasons, explained in the following:

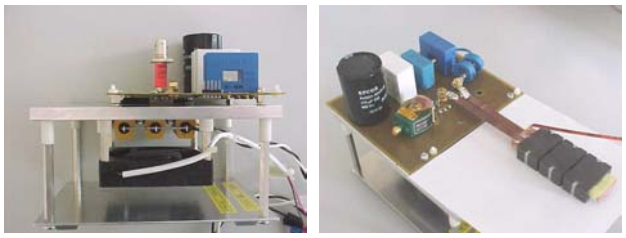
The mechanical design of the power circuit has to be adapted in a way that the oscilloscope current probe can be inserted in the current path. This structural alteration leads to considerably worse measurement results in comparison to a mechanical design without an inserted current probe. The second reason is the limited bandwidth and rise time of oscilloscope current probes (cf. **Tab.3**) in comparison to a passive AC current transformer or a coaxial-shunt.

More accurate measurement results will be obtained by the utilization of a coaxial-shunt or a Pearson current monitor with small geometric dimensions. The picture in **Fig.4**(a),(b) and **Fig.5**(a),(b) shows the realized design of the power circuit. There, the current sensors are integrated in the mechanical assembly of the power circuit.



a) b)

Fig.4: Mechanical construction of the power circuit. The board of the test circuit is constructed with a three-layer stack of ordinary epoxy FR4 material coated with 35µm copper. The silver plated brass of the coaxial-shunt is soldered on top of the ground plane (mid-layer) to keep the wiring inductance low **a)**. The Pearson current transformer is located in the same position as in the construction with the coaxial-shunt. The current path from the input inductor through the Pearson probe is provided by a rod of copper 3mm in diameter, and the return path of the current into the ground plane is made with a 60° segment of a copper plate with 0.5mm thickness (comparable with a mudguard) **b)**.



a) b)

Fig.5: The CoolMOS power transistor and the SiC diode are mounted on the top of an aluminum carrier plate. On the bottom of the plate a number of power resistors are attached to heat up the silicon components in order to test them at a high junction temperature **a)**. In **b)** the assembly of the input inductor is visible.

It has to be pointed out that the wiring of the power circuit has a major influence on the switching behavior and therefore the printed circuit board design of the power circuit used for the testing has to correspond with the layout used for the final system.

Furthermore, the input inductor should be designed with a minimum parasitic capacitance to keep the charge current passing through the parasitic capacitor low.

(If the parasitic capacitance of the input inductor is assumed to be 100pF a change-rate in the drain source voltage of 40V/ns has a charge current into the parasitic capacitance of 4A as a direct consequence!)

4 Measurement of Switching Behavior and Switching Losses

For measuring the switching behavior and the switching losses of the CoolMOS power transistor / SiC diode combination, the assembly shown in **Fig.1** was used. There, between the input voltage and the connection point (cp) (anode of D_F and the drain terminal of the power transistor S), an inductor is inserted giving the circuit a boost-type structure. The positive output voltage $u_{out} = 400V$ is limited by using four zener diodes connected in series (1W/100V each) instead of using a voltage source. With this arrangement no galvanic connection to a power source has to be made and therefore further parasitic elements can be avoided in the test environment.

Due to the low repetition rate of the pulse sequence, the wattage rating of the zener diodes is sufficient to dissipate the transferred energy.

The amount of energy transferred from the input to the output at maximum input current is given by

$$W_{Lin} = 0.5 \cdot L \cdot \hat{i}_{in}^2 = 0.5 \cdot 38\mu H \cdot (25A)^2 \simeq 12mWs \,. \quad (5)$$

When the power transistor is in the on state we have a current flow from the input capacitor C_{in} via the input inductor L_{in} and the power transistor S to ground. During this period the input current i_{in} rises to an adjustable value where the power transistor S is turned off for the duration of approximately 0.8µs. Subsequently the power transistor is turned on again for the duration of approximately 0.8µs.

This low repetition pulse sequence (several Hz) is shown in **Fig.6**.

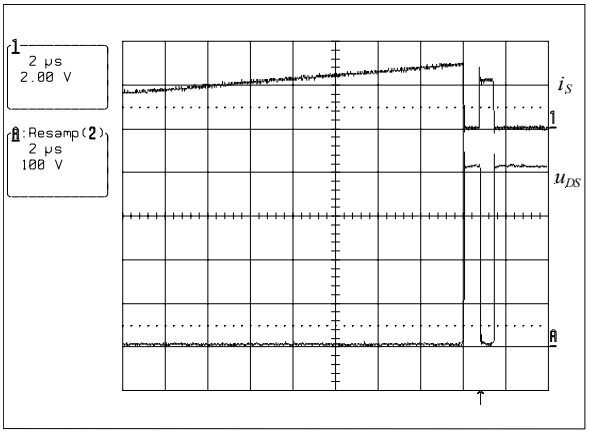


Fig.6: On-off-on-off pulse sequence for the evaluation of the switching behavior and the switching losses of the power circuit.

4.1 Switching Behavior

All subsequent measurements have been carried out with the gate resistors $R_{G,on} = 8.2\Omega$, $R_{G,off} = 6\Omega$ at an output voltage of $u_{out} = 400V$ if not otherwise noted. The junction temperature of the power semiconductors was equal to the ambient temperature of $\vartheta_{ambient} = 20°C$.

The instrument utilized for the measurements was a DSO **LeCroy WavePro 950** (1GHz, 4GS/s), a voltage differential probe **DXC100A** used with a **D1855A** differential amplifier.

The current waveforms have been acquired by means of a coaxial-shunt (SDN-414-10, 100mΩ, 2GHz) from T&M Research and/or the Pearson AC current monitor (model 2877).

The results of the turn-on and turn-off measurements are depicted in **Fig.7**(a),(b) for a transistor current of $i_s = 30A$ at the first turn-off instance.

The resulting transient turn-off voltage shows a maximum value of $u_{DS,\max} = 460V$ (cf. **Fig.7**(a)) which is mainly caused by the forward recovery voltage of the diode D_F and the inductive voltage drop across the wiring inductance (L_{wiring} from diode and ESL of the output capacitor).

Increasing or decreasing the value of the switched current has no influence on the turn-off overvoltage in case of a low inductance power circuit layout. Therefore an overvoltage protection circuit (snubber circuit) can be avoided.

The resulting turn-off voltage slope has a value of 40V/ns. At the beginning of the switching instance, a rapid current drop in i_s of about 4A can be seen, because of the charging of the parasitic capacity C_{DF} (cf. **Fig.8**). This charge current bypasses the current sensor via the output capacitor, and therefore this current flow cannot be seen in the current sensor.

An estimation of the value of this parasitic capacitor can be given by means of the constant transistor drain-source voltage slope du_{DS}/dt and the constant current drop of i_s :

$$C_{DF} \cong \frac{\Delta i_s}{du_{DS}/dt} = \frac{4A \cdot 15ns}{400V} = 150pF \ . \qquad (6)$$

The current through the input inductor can be assumed as constant at the switching instance.

After the power transistor recaptures the blocking capability, the current through the power transistor rapidly decreases with a slope of 1A/ns and subsequently increases in the Diode D_F .

The turn-on switching behavior, depicted in **Fig.7**b), shows a voltage drop in the transistor drain-source voltage u_{DS} of about 100V due to the high di/dt-rate of the current passing through the wiring inductance of the diode D_F and the ESL of the output capacitor.

The output voltage of the capacitor (inner capacitor voltage) is assumed to be constant at the switching instance. When the power transistor begins to conduct the current passing through the transistor increases with a slope of 2.5A/ns. An estimation of the wiring inductance can be given with

$$L_{wiring} = \frac{\Delta u_{DS}}{di/dt} = \frac{100V \cdot 10ns}{25A} = 40nH \ . \qquad (7)$$

At the first turn-off instance the current through the input inductor has a value of $i_{in} = 30A$. During the following period (S is open) the inductor current decreases linearly by an amount of

$$\Delta i_{in} = \frac{u_{out} - u_{in}}{L_{in}} t_{off} = \frac{400V - 40V}{38\mu H} 800ns = 7.6A \ . \qquad (8)$$

Therefore, the initial value of the input inductor current for the subsequent on-period is 22.7A.

At the beginning of the linearly decreasing drain-source voltage u_{DS} (**Fig.7**(b)), the current through the sensor shows a value of approximately 22A, which is caused by the charging of the parasitic capacitors C_{DF} and C_{DS} (the power transistor is not yet fully conducting).

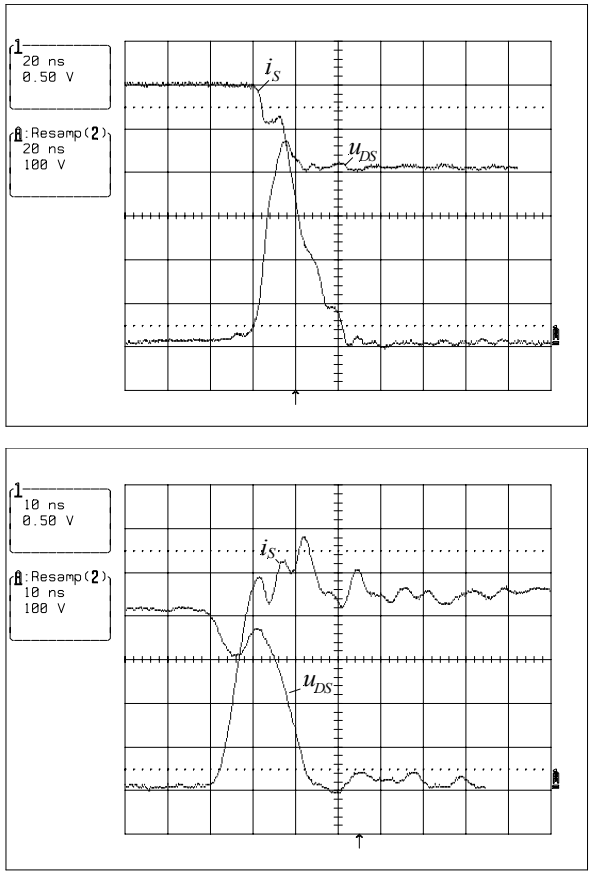


Fig.7: Turn-off behavior of the CoolMOS power transistor. The drain-source voltage shows a voltage slope of 40V/ns and a current slope passing through the transistor of 1A/ns **a)**. The voltage drop in the drain source voltage at the turn-on instance is caused by the high di/dt-rate through parasitic wiring inductance. During the interval where the drain source voltage decreases linearly the parasitic capacitance C_{Lin} of the input inductor is charged.

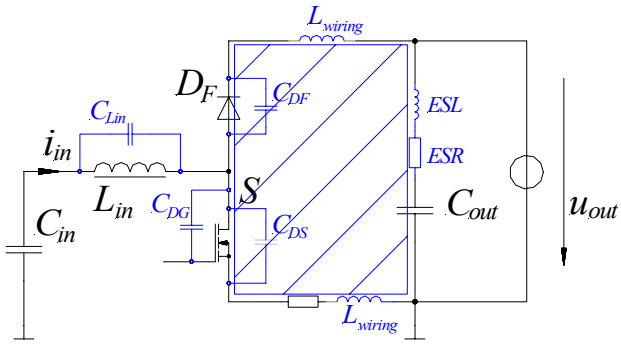


Fig.8: During the on period (S is closed) the current into the input inductor increases. After turning off the CoolMOS (S open) the current i_{in} through the input inductor commutes to the current path through the SiC Diode D_F into the output capacitor C_{out} . The altered current path (visualized by the hatched area) during the switching operation acts like a parasitic inductance. The watermarked capacitors are the parasitic capacitors of the corresponding elements.

During the following time period (linear decreasing u_{DS}) a current is superimposed to the above mentioned charge current of the parasitic capacitors C_{DF} and C_{DS}.

This superimposed current is a charge current of the input inductors parasitic capacitance C_{Lin}, and is initiated by the high du/dt-rate of the drain-source voltage.

An estimation of the value of this parasitic element can be given by:

$$C_{Lin} = \frac{\Delta i_S}{du_{DS}/dt} = \frac{3A \cdot 12ns}{360V} = 100pF \,. \qquad (9)$$

It has to be pointed out that the charge current of the input inductors parasitic capacitance is also contributing to the power losses. Therefore, it is highly recommended to design the input inductor with a minimum of parasitic capacitance.

Also a high frequency ringing is superimposed to the sensed current with an oscillation frequency of about 170MHz. The oscillation is excited on every turn-on instance.

Fig.8 shows the parasitic elements forming the oscillation circuit. These are the parasitic capacitors C_{DF} and C_{DS}, the wiring inductances of the diode and of the CoolMOS (combined in L_{wiring}), as well as the ESL of the output capacitor. Only the resistance of the CVR and the ESR of the output capacitor are contributing to the damping of the high frequency ringing.

4.2 Switching Losses

The measurement results of the turn-on and the turn-off energy losses (depicted in **Fig.9**(a),(b)), considerably depend on the amount of time-skew between voltage and current waveforms. A time-skew of ±2ns leads to a different measurement result of ±10% related to the measurement result obtained with corrected channel delays.

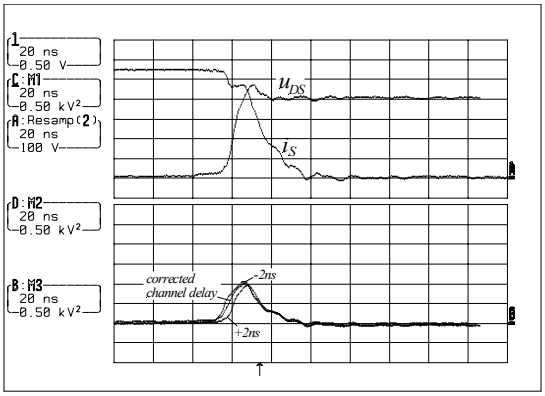
Oscilloscope current probes have a specified delay of about 17ns (cf. **Tab.3**). A coaxial-cable (i.e. RG-58) has a signal delay of 5.03ns/m.

One can see immediately that a compensation of the time-skew of the voltage and the current waveforms is a determining factor providing an accurate measurement of the power losses.

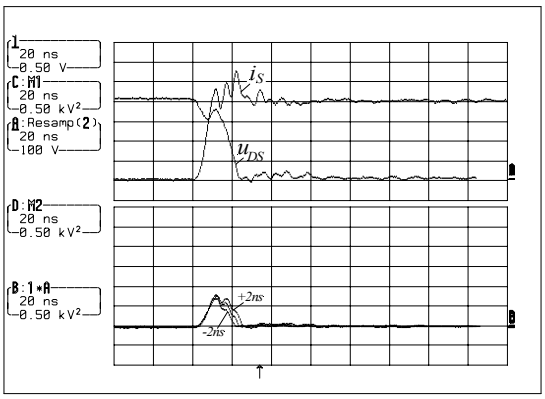
A time-integration of the turn-off power waveform (**Fig.9**(a)) denotes the turn-off energy.

In the particular case (@ 400V / 27A), with a corrected channel delay, the turn-off energy is $W_{turn-off} = 180\mu Ws$, and the turn-on energy loss (@ 400V/20A) is $W_{turn-on} = 75\mu Ws$.

It has to be mentioned that the focus in this paper is to point out guidelines for a practical application of the setup to accurate measure the switching losses. It is not a subject to provide exact values of the turn-on and turn-off power losses for this particular setup.



a)



b)

Fig.9: Analysis of the turn-off **a)** and turn-on **b)** switching behavior of the CoolMOS power transistor. The measurements have been carried out at an output voltage of 400V and a junction temperature of 20°C.

4.3 Comparison of the Coaxial-Shunt and the Pearson Current Monitor

In **Fig.10** a comparative measurement of the turn-on switch-current i_S between the coaxial-shunt and the Pearson current monitor is shown. It can be seen directly that both current waveforms are coincident. Therefore, both current sensors are adequate for the measurement of the power losses in high speed switching applications.

It has to be pointed out that for still higher di/dt-rates the Pearson current monitor runs into its bandwidth limit.

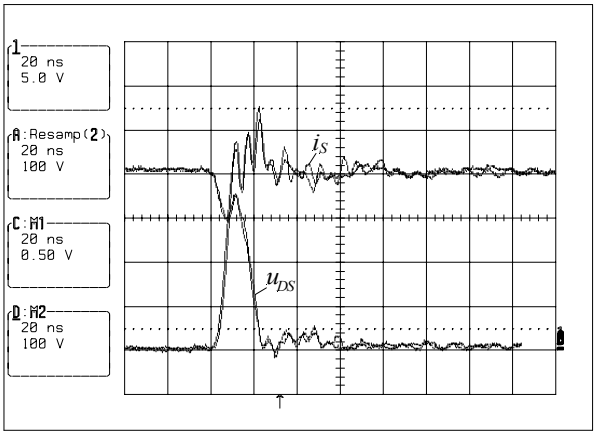


Fig.10: Comparative measurement of the coaxial-shunt and the Pearson current monitor. Both sensors are adequate for high speed switching measurements.

5 CONCLUSIONS

In this paper it is shown that the coaxial-shunt and the Pearson current monitor are both practical for the analysis of the switching behavior and the determination of the switching losses in high speed switching applications. An advantage of the Pearson current monitor is the galvanic isolated current signal. Therefore, a single-ended passive high voltage probe can be used, with the advantage of a higher bandwidth limit of the measured voltage signal compared to a voltage differential probe.

The coaxial-shunt can be easily inserted in the desired current path with a minimum of additional wiring inductance. One disadvantage with the coaxial-shunt is that it does not provide a galvanic isolated current signal.

It is shown that the input inductor of the power circuit has to be designed with a minimum parasitic capacity in order to avoid a charge current through this parasitic element because this charge current is also contributing to the power losses.

Furthermore, in this paper it is shown that for an accurate determination of the turn-on and turn-off energy losses the time-skew between current and voltage waveforms has to be corrected.

Further researches are investigating the influence of still higher switching speeds on the excitation of high frequency ringing, accompanied with the increased switching speed. In particular, a compromise has to be found between the reduction of the switching losses and the increasing radiation of EMI.

REFERENCES

[1] **Kolar, J.W., Ertl, H., Zach, F.C.:** *Design and Experimental Investigation of a Three-Phase High Power Density High Efficient Unity Power Factor PWM (VIENNA) Rectifier Employing a Novel Power Semiconductor Module. Proceeding of the 11th IEEE Applied Power Electronics Conference, San Jose, USA, March 3-7, Vol 2, pp. 514 – 523 (1996).*

[2] **Miniböck J., Kolar, J.W.:** *Experimental Analysis of the Application of Latest SiC Diode and CoolMOS Power Transistor Technology in a 10kW Three-Phase PWM (VIENNA) Rectifier. (2001).*

[3] **Johnson H.W., Graham M.,:** *High-Speed Digital Design: A Handbook of Black Magic. Prentice Hall. (1993).*

[4] **Infineon Technologies AG:** *CoolMOS Power Transistor Preliminary Datasheet SPW47N60C2. www.infineon.com (2000).*

[5] **Infineon Technologies AG:** *Silicon Carbid Schottky Diode Preliminary Datasheet SDP06S60. www.infineon.com (2001).*

[6] **Pearson Electronics, INC.:** *Wide Band Current Monitors Description and Specification. www.pearsonelectronics.com (2002).*

[7] **T&M Research:** *Series SDN-414 Current Viewing Resistors Description and Specification. www.tandamresearch.com (2002).*