# Comparison of different Bidirectional Bipolar Switches for use in Sparse Matrix Converters

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## Abstract

Bidirectional, bipolar switches up to now consisted of a combination of known power semiconductor switches — such as IGBTs and diodes — in different topologies; novel power semiconductor switches — such as reverse blocking or reverse conducting IGBTs — permit to simplify these circuits. The approach of this paper is to define equally sized components incorporating the different topologies and semiconductors. It is thus possible to directly compare those various bidirectional, bipolar switches. An assessment of their properties is given with respect to the operational conditions in the sparse matrix converter.

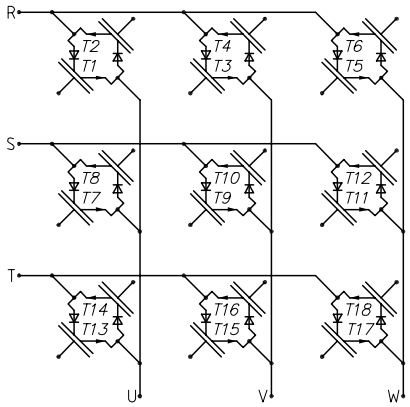


Figure 1: matrix converter with three phase input (R, S, T; filters not shown) and three phase output (U, V, W), using $3 \cdot 3 = 9$ bidirectional bipolar switches, each switch composed of two reverse blocking IGBTs, e. g. $T_1$ and $T_2$

## 1 Introduction

Matrix converters are known from literature, e. g. [1], [2]. As **figure 1** shows, their power section basically consists of bidirectional, bipolar switches between each of the input and each of the output phases. Commutation strategies require that those switches must — at least in certain time intervals — be able to be turned on only for one current direction, while maintaining blocking capability in the opposite sense.

Citing [3] and [4], [5] instead proposes the very sparse matrix converter with the same functionality, but using separated input and output sections, connected by a DC link without storage elements. Input section consists of one bidirectional, bipolar switch each for connection of any input phase to plus and minus of the DC link. Output section has a conventional bridge topology as known from voltage source inverters; for a three phase system operated at mains voltage levels, it typically consists of three phaselegs — two IGBTs with antiparallel free wheeling diodes. A commutation strategy can be applied, changing the switch-

ing state of input section while output section is in free wheeling mode; thus switching of input section can be performed at zero current, which facilitates safe commutation and reduces switching losses to a minimum. Turn on state of the bidirectional, bipolar switches needn't be separately controllable for the two directions of current flow.

# 2 Bidirectional, Bipolar Switches

## 2.1 Dual Antiserial Switching Elements

Typically, a bidirectional, bipolar switch in a matrix converter operated at mains voltage levels is composed of an antiserial connection of two switching elements, each consisting of an IGBT and an antiparallel diode, as depicted in **figure 2**. This topology permits to separately control both directions of current flow. In common collector configuration, only one power supply per input and output of the matrix topology is needed, however a separate driver for each IGBT. Contrary, in common emitter configuration the drivers of each switch have to use a galvanically isolated supply — however one driver for both IGBTs is sufficient, if separate control of current direction is not required.

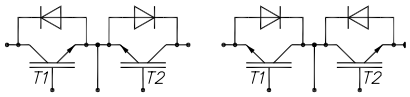


Figure 2: bidirectional, bipolar switches, consisting of two antiserial switching elements, each composed of an IGBT and an antiparallel diode, in common emitter or common collector configuration respectively

It is of course possible to use a novel monolithic semiconductor device, which exhibits an IGBT like behaviour, but provides MOSFET like reverse conducting capability, instead of a hybrid combination of conventional IGBT and diode in the circuits of figure 2. **Figure 3** schematically shows its chip structure: The emitter side on top of the chip corresponds to IGBTs or MOSFETs. The collector side on the bottom side however combines both technologies — there is pattern of alternating $p$ and $n^+$ areas. The $p$ areas are responsible for IGBT like conduction with bipolar carriers, while the $n^+$ shorts lead to a MOSFET like intrinsic reverse *pin* diode in conjunction with the $p$ well on top of the chip.

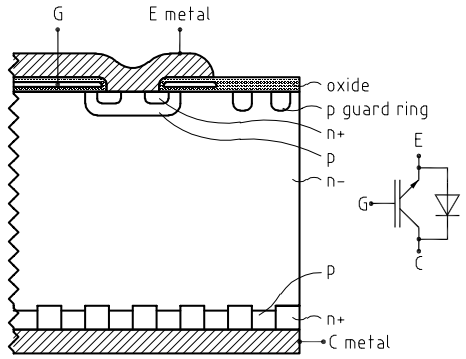


Figure 3: chip structure of and symbol used for reverse conducting IGBT BIMOSFET™

## 2.2 Dual Antiparallel Reverse Blocking IGBTs

A different approach is to use novel monolithic semiconductor devices, which behave like an IGBT, but provide blocking capability for applied reverse voltage $U_{CE} < 0$ [6]. **Figure 4** displays a schematic cross section of this kind of reverse blocking IGBT chip. Cell structure as drawn will continue to the left, while the chip edge with the guard rings for junction termination is shown on the right. Geometry and mode of forward operation basically correspond to NPT IGBTs [7] [8]. However, in addition to the NPT structure, the $p^+$ collector is folded up by isolation diffusion from the bottom to the top at the chip edge. This enables the lower $p^+$-$n^-$ junction to block a reverse voltage — the collector being negative. Without this measure, the junction would break through at the chip edge due to lack of field stop, which is the reason why standard IGBTs must not be connected to significant reverse voltage.

The symbol proposed in the right of figure 4 shows the integrated diode on collector side;

it is used in this paper to represent the reverse blocking IGBT.

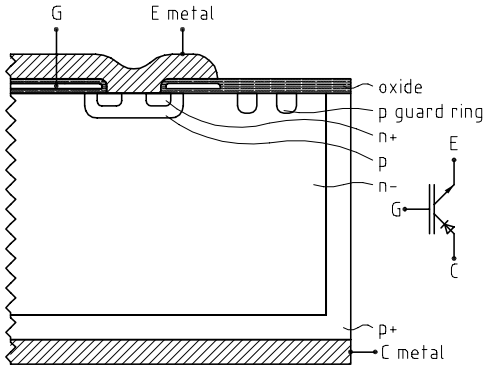


Figure 4: chip structure of and symbol used for reverse blocking IGBT

An antiparallel connection of two of those devices according to **figure 5** operates as bidirectional, bipolar switch. Both directions of current flow can be controlled separately. In a matrix converter, one driver would be needed for each reverse blocking IGBT, and one supply for the drivers of all devices connected with the emitter to the same input or output line.

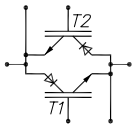


Figure 5: bidirectional, bipolar switch, consisting of two antiparallel reverse blocking IGBTs

### 2.3 IGBT in Diode Bridge

Finally, a bidirectional, bipolar switch may be composed of a single phase diode bridge with a diagonal IGBT according to **figure 6**. Both current directions are controlled by the IGBT's single gate drive, requiring a galvanically isolated supply.

## 3 Sparse Matrix Converter

The basic structure of the power circuit of an Indirect Matrix Converter (IMC), cf. figure 1(b) in [5], is shown in **figure 7**. The IMC,

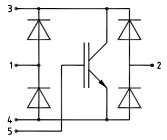


Figure 6: bidirectional, bipolar switch, consisting of a Graetz diode bridge with a diagonal IGBT

i. e. the DC side coupling of a current-source-type rectifier input stage and a voltage-source-type inverter output stage does allow to employ a commutation strategy of significantly lower complexity and/or higher reliability as compared to a Conventional Matrix Converter (CMC, cf. figure 1). For changing the switching state of the input stage, the output current — which is impressed by the inductive load behavior — is free-wheeling via the output stage power semiconductors. Therefore, no multi-step commutation strategy has to be employed and/or the commutation is independent from the sign of the DC link current or on phase voltage difference of the commutating phases. Furthermore, as shown in the following, the realization effort of the power circuit could be reduced considerably, resulting in topologies which have been denoted as Sparse Matrix Converters (SMC) in [5] and are of special interest for future industrial applications.

### 3.1 Realization of the Input Stage and Output Stage Bridge Legs

According to [5] the number of power transistors being employed in the IMC could be reduced without impairing the functionality of the system, what does result in topologies of the input stage bridge legs shown in **figure 8**(1) (Sparse Matrix Converter, SMC) and figure 8(2) (Very Sparse Matrix Converter, VSMC). Further bridge leg topologies which do employ an equal number of turn-off power semiconductors as the IMC (cf. figure 8(3)), but do allow to combine the function of two discrete power semiconductors of the IMC into a single device are shown in figures 8(4) and (5).

In the following the different bridge leg topologies should be evaluated concerning the resulting total input stage conduction losses.

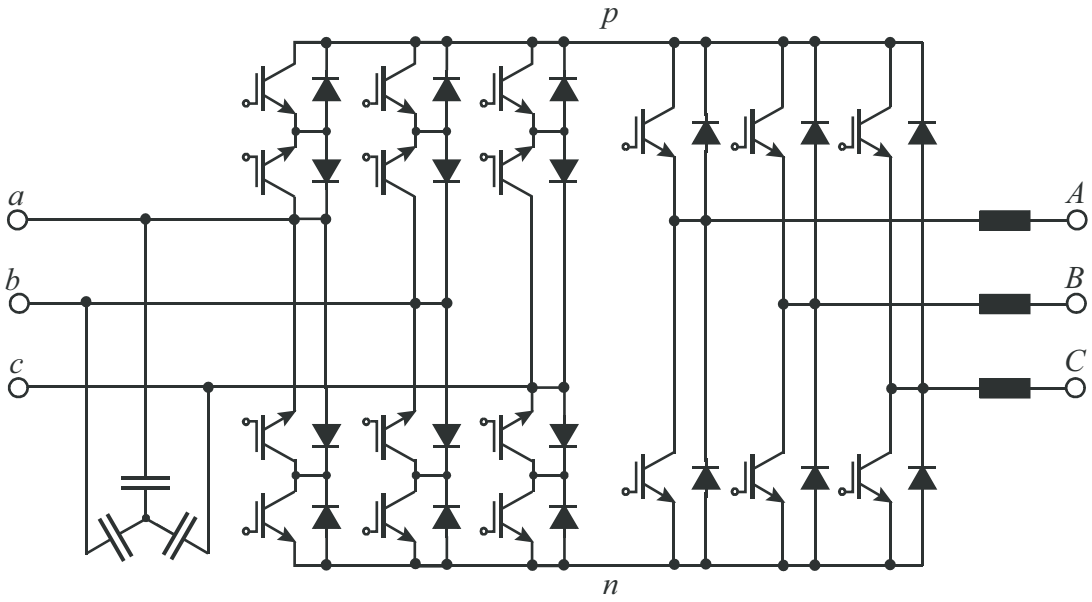


Figure 7: structure of the power circuit of an Indirect Matrix Converter (IMC)

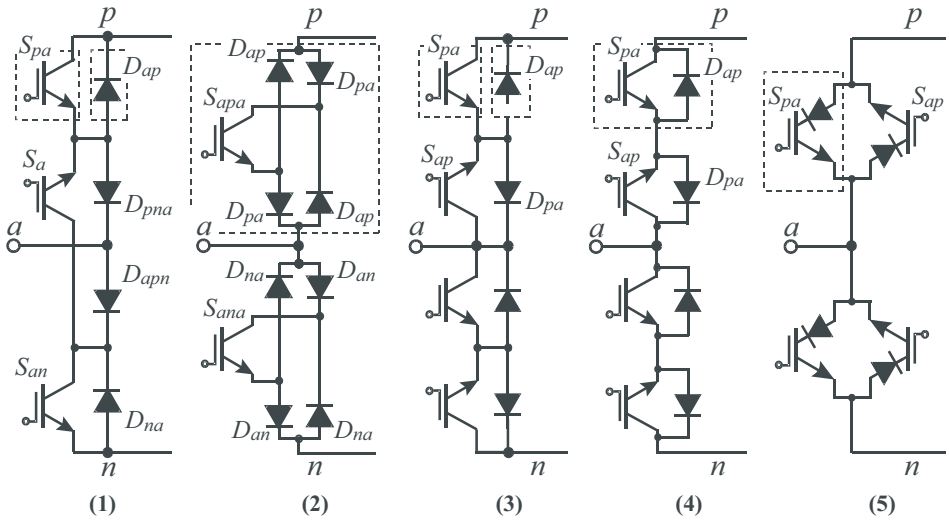


Figure 8: input stage bridge leg topologies of the IMC: (1) Sparse Matrix Converter (SMC); (2) Very Sparse Matrix Converter (VSMC); (3) Indirect Matrix Converter (IMC); (4) IMC for application of reverse conducting IGBTs; (5) IMC for application of reverse blocking IGBTs

There, the bridge legs of the output stage are thought to be realized by power modules of type FII50-12E, containing two high switching speed IGBTs in connection with antiparallel ultra fast recovery diodes.

For the input stage, power semiconductors of equal performance and/or type as for the output stage are employed for the realization of bridge leg topology (1) and (3). This also holds for topology (2), however in this case the combination of power semiconductors forming a four-quadrant switch is available in a single isolated package, i. e. in the form of a power device FIO50-12BD.

By application of reverse conducting IGBTs of type IXBH15N140, a power transistor and the respective antiparallel diode of topology (3) are monolithically combined what does reduce the number of discrete power semiconductors and/or does facilitate the practical realization of the system (cf. (4)).

Finally, the four-quadrant switch formed by antiserial connection of two IGBTs and the respective free-wheeling diodes could be replaced by antiparallel connection of two reverse blocking IGBTs (cf. (5)) of type IXRH50N120. Besides the lower number of discrete power semiconductors this does lower the on-state voltage and/or the conduction losses of the four-quadrant switches.

The calculation of the conduction losses is based on the parameters compiled in **table 1** which have been derived from the power semiconductor data sheets. The conduction losses of a power transistor and/or diode are calculated using

$$P_C = U_{F0} \cdot I_{avg} + r_F \cdot I_{rms}^2 \qquad (1)$$

[10]. There, the average value $I_{avg}$ and the rms value $I_{rms}$ of the component current are calculated referring to the analytical approximations derived in Section VI of [5] for characteristic values of the modulation index

$$M_2 = \frac{\hat{U}_2}{\frac{1}{2} \cdot \overline{U}} \qquad (2)$$

(where $\overline{U} = \frac{9}{\pi} \cdot \ln\left(\sqrt{3}\right) \cdot \hat{U}_1$ denotes the global average value of the DC link voltage, cf. (44) in [5]) and in dependency on the phase displacement $\phi_2$ of the output current and the output voltage fundamentals for two output phase current rms values $I_{2rms}$. (For $M_2 = 1$ we have $\hat{U}_2 \approx 0.787\hat{U}_1$, cf. [5].)

Table 1: parameters of the power semiconductors employed in the output stage and in the different input stage SMC bridge leg topologies; the current independent voltage drop $U_{F0}$ and the differential on-resistance $r_F$ are derived from the power semiconductor data sheets and do approximate the actual on-state characteristic in a current range of $0...30A$, for a junction temperature of $T_J = 125°C$ and a gate voltage of $U_{GE} = 15V$

| | power device | transistor | | diode | |
|---|---|---|---|---|---|
| | | $\frac{U_{F0}}{V}$ | $\frac{r_F}{m\Omega}$ | $\frac{U_{F0}}{V}$ | $\frac{r_F}{m\Omega}$ |
| input stage | | | | | |
| (1) | FII50-12E | 0.8 | 64 | 1.0 | 43 |
| (2) | FI050-12BD | 0.8 | 64 | 1.0 | 43 |
| (3) | FII50-12E | 0.8 | 64 | 1.0 | 43 |
| (4) | IXBH15N140 | 4.0 | 280 | 2.2 | 160 |
| (5) | IXRH50N120 | 1.0 | 62.5 | 1.0 | 62.5 |
| output stage | | | | | |
| | FII50-12E | 0.8 | 64 | 1.0 | 43 |

Remark: For a direct comparison of the different power modules employed in the various input stage bridge leg topologies (cf. figure 8) one would have adapt the parameters given in Tab. 1 with reference to an equal total silicon area employed in each case. There, also the different share of the diodes and transistors could be considered. In the case at hand this side condition is fulfilled only in a rough first approximation. A more detailed comparison which also will include the switching losses will be shown in a future paper.

### 3.2 Comparative Evaluation of the Conduction Losses of SMC Topologies

In **figures 9 and 10** the conduction losses of the output stage and of the different realizations of the input stage are given for $M_2 = 0.5$ and $M_2 = 1$, $\phi_2 = 30°$ and $\phi_2 = 60°$, and for $I_{2,rms} = 10A$ and $I_{2,rms} = 20A$ ($U_{1,rms} = 230V$). There, also the

partitioning of the total losses into the contributions of the diodes and of the power transistors is shown.

The conduction losses of the output stage do increase more than linearly with increasing output phase current rms value $I_{2,rms}$ what could be explained by the relatively large voltage drop across the differential on-resistance of the power semiconductors as compared to $U_{F0}$ at larger currents which does translate into a quadratic dependency of the on-state losses on $I_{2,rms}$.

There is relatively low dependency of the total conduction losses on $\phi_2$ as the on-state characteristics of the power transistor and the power diode are not very much different and the current flow in any case is via one of the devices. For increasing $\phi_2$ only the partitioning of the total losses into transistor and diode losses does change; for $\phi_2 = 30°$ mainly active power is processed by the output stage, i. e. the current flow is mostly via the power transistors. For $\phi_2 = 60°$ the relative on-time of the diodes is increasing and the on-time of the power transistors is correspondingly decreasing as partly energy is only distributed from one phase to another via the DC link connection of the output stage bridge legs.

Also, changing $M_2$ does not take considerable influence on the conduction losses as the output current is carried by the power semiconductors of the output stage also within the free-wheeling intervals.

As for the output stage the conduction losses of the input stage do show a direct dependency on the output current rms value. An increasing phase displacement of the output current does reduce the input stage conduction losses as the average and the rms value of the DC link current which are determining the conduction losses are reduced correspondingly. For a reduction of the output stage modulation index $M_2$ the relative current conduction interval of the input stage power transistors is reduced correspondingly as the free-wheeling interval of the output stage (interval being characterized by zero DC link current, i. e. $i = 0$) is increased in length resulting in a reduction of the input stage conduction losses.

A comparison of the relative total conduction

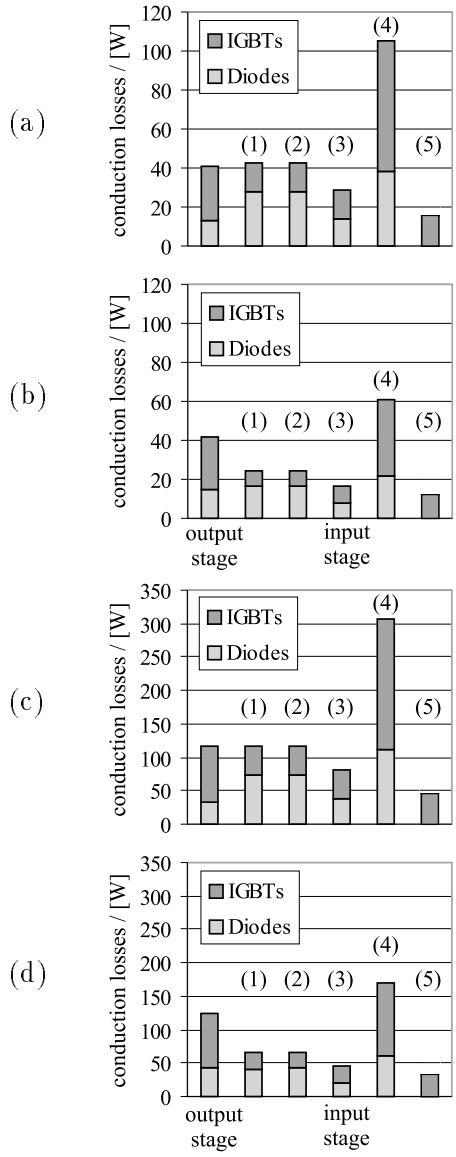


Figure 9: conduction losses $P_{C,abc}$ of the input stage for the different bridge leg topologies, furthermore conduction losses $P_{C,ABC}$ of the output stage; system operating parameters: $M_2 = 0.5$; (a): $I_{2,rms} = 10A$, $\phi_2 = 30°$; (b): $I_{2,rms} = 10A$, $\phi_2 = 60°$; (c): $I_{2,rms} = 20A$, $\phi_2 = 30°$; (d): $I_{2,rms} = 20A$, $\phi_2 = 60°$

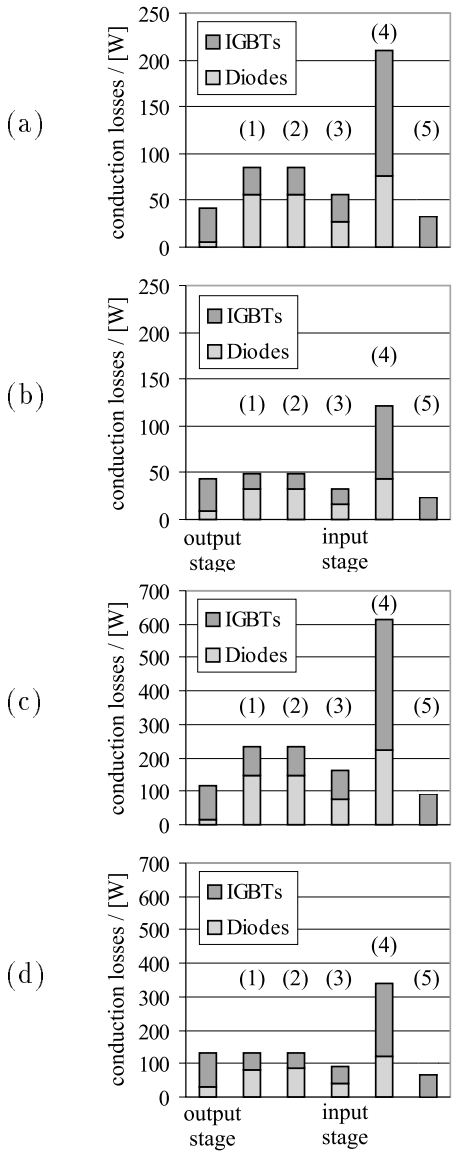


Figure 10: as previous figure but system operation at $M_2 = 1.0$; (a): $I_{2,rms} = 10A$, $\phi_2 = 30°$; (b): $I_{2,rms} = 10A$, $\phi_2 = 60°$; (c): $I_{2,rms} = 20A$, $\phi_2 = 30°$; (d): $I_{2,rms} = 20A$, $\phi_2 = 60°$

losses

$$P_{C,r} = \frac{P_{C,abc} + P_{C,ABC}}{S_2} \tag{3}$$

which are normalized to the rated apparent output power

$$S_2 = 3 \cdot U_{2,rms} \cdot I_{2,rms} \tag{4}$$

with $U_{2,rms} = 0.787 \cdot U_{1,rms}$ ($M_2 = 1$), $U_{1,rms} = 230V$, and $I_{2,rms} = 20A$ ($S_2 = 10.86kVA$) is depicted in **figure 11**. Accordingly, the relative total conduction losses resulting for $M_2 = 1$, $I_{2,rms} = 20A$ and $\phi_2 = 0$ could be interpreted as loss in efficiency, i. e. the efficiency of the system in case only conduction losses would occur would be $\eta \approx 1 - P_{C,r}$.

According to figure 11 the bridge leg topologies (1) und (2) do show little differences concerning the resulting conduction losses, as for $\phi_2 = 30°$ the DC link current $i$, which is formed by segments of the output current, shows only a positive sign and/or a power transistor and two power diodes are conducting $i$ in case a bridge leg is in the turn-on state (cf. figure 17 in [5]). For $\phi_2 = 60°$ $i$ does show minor negative components which are conducted by a power transistor but only a single diode for topology (1) what however does not take noticeable influence on the resulting conduction losses. Therefore, a major advantage of topology (1) only would be given for feeding energy back from the load into the mains, however, this case which would be interesting e. g. for regenerative braking of AC drives is not considered in this paper in order to limit the scope to the most essential aspects.

As compared to topologies (1) and (2), topology (3) does show lower conduction losses, as the current flow always is only via a single power transistor and a single diode.

Bridge leg topology (4) suffers from a high power transistor and diode on-state voltage and high differential on-resistance, but could benefit from low transistor switching losses and elevated blocking voltage. Also for reducing the system throughput power a higher efficiency would be achieved.

By employing a reverse blocking IGBT (topology (5)) the conduction losses as compared to topology (3) could be further reduced as essentially only a single IGBT forward voltage drop is inserted into the current path of a bridge leg.

In summary, as a consequence of a reduction of the number of turn-off power semiconductors (SMC, VSMC) as compared to the IMC one has to accept a reduction of the efficiency of the energy conversion in the range of 1% due to higher conduction losses. For employing the power modules FIO50-12BD and FII50-12E in the input and/or output stage and for realizing a system having a rated (apparent) output power of $10kVA$ the conduction losses do cause a reduction of the efficiency of about 2...3%. In case the switching frequency is selected considering an approximate equality of switching and conduction losses one could achieve a remarkably high total efficiency of the system of about 95%.

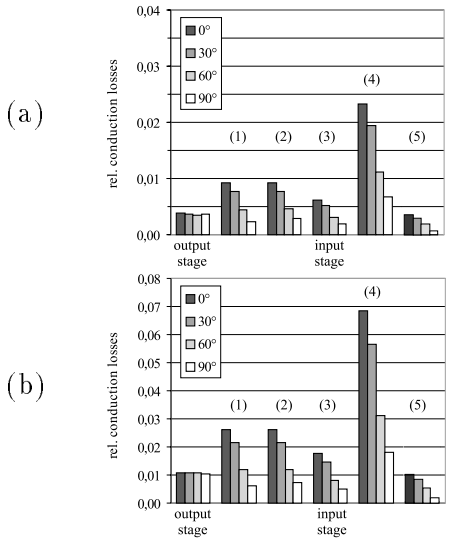


Figure 11: relative conduction losses $P_{C,abc,r}$ of the input stage for the different bridge leg topologies for $M_2 = 1.0$; (a): $I_{2,rms} = 10A$, (b): $I_{2,rms} = 20A$ with reference to $S_2$; furthermore relative conduction losses $P_{C,ABC,r}$ of the output stage (also normalized to $S_2$)

### 3.3 Switching Losses

As already mentioned, the commutation of the IMC, SMC, and VSMC input stage is at zero DC link current. Therefore, one would assume that only the output stage power semiconductors are subject to switching losses. However, as a more detailed analysis shows, e. g. for switching over the positive DC link bus $p$ from input phase $b$ to input phase $a$ in $t_2$ (cf. **figure 12**), due to charge carriers being still present in $S_{bpb}$ a current pulse via $S_{apa}$ and $S_{bpb}$ does occur which does cause losses in the already blocking IGBT $S_{bpb}$ and turn-on losses of $S_{apa}$ which are further increased by the charging and/or discharging of the parasitic DC link capacitance via $S_{apa}$.

Furthermore, a turn-on recovery voltage does occur across the diodes of the input stage once the output stage is changing from free-wheeling into a subsequent active switching state being connected with a DC link current $i$ forcing the diodes into conduction. The forward recovery voltage does reduce the turn-on voltage of the power transistor and/or the turn-off voltage of the respective diode, i. e. the switching losses of the output stage are partly transferred to the input stage.

Therefore, the switching losses of the input stage are mainly determined by parasitic effects of the power semiconductors. A calculation of the switching losses with reference to data sheets for this reason does not provide sufficient accuracy. Thus the switching losses have not been considered in this paper in a first step. A detailed breakdown of the switching and conduction losses to the individual components will be shown for the final circuit PCB layout in a future paper.

## 4 Conclusions

Sparse matrix converter topologies in connection with latest power semiconductor components do allow to considerably reduce the realization effort of an AC/AC-converter as compared to a conventional matrix converter topology. According to the results of an analysis of the conduction losses, the system shows a high efficiency and therefore is of special interest for an industrial application, e. g. for realizing a motor-integrated converter.

In a next step the switching losses [11] of the various SMC topologies will be analyzed in detail and the silicon utilization [12] will be calculated. Furthermore, the rated system output power which could be achieved by employing a power module at a given switching frequency will be determined for operation in the European 400V line-to-line rms low-voltage mains.

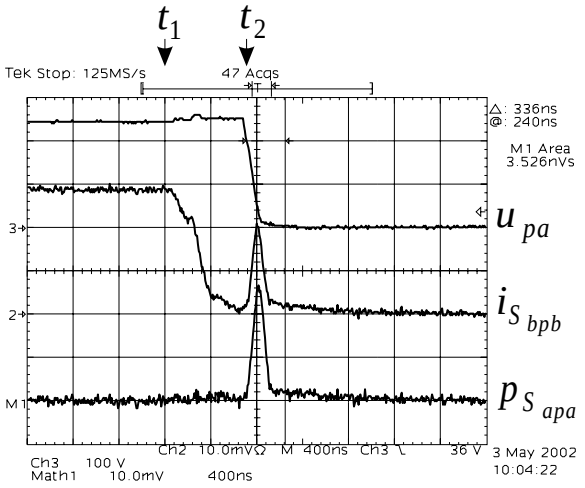


Figure 12: Time behavior of the switch voltage $u_{pa}$, of the current $i_{Sbpb}$ in power transistor $S_{bpb}$ for turn-on of $S_{apa}$ at $t_2$ subsequent to the turn-off of $S_{bpb}$ at $t_1$ — scales: $100\frac{V}{div.}$ and $5\frac{A}{div.}$; furthermore turn-on power losses $p_{Sapa}$ in $S_{apa}$ caused by charge carriers still present in $S_{bpb}$ at $t_2$; for the realization of the input stage power modules of type FIO50-12BD and for the output stage power modules of type FII50-12E are employed.

Finally, a four-quadrant switch being realized by SiC Schottky diodes and a SiC-J-FET/Si-MOSFET-cascode switch will be experimentally evaluated in a 200kHz switching frequency VSMC of extremely high power density.

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