Optimized Pulse Patterns for the 5-Level ANPC Converter for High Speed High Power Applications

Jörg Meili[1,2], Srinivas Ponnaluri[2], Leonardo Serpa[1], Peter K. Steimer[2], Johann W. Kolar[1]

[1]Power Electronic Systems Laboratory
Swiss Federal Institute of Technology Zurich
ETH-Zentrum / ETL
CH-8092 Zürich

[2]ABB Switzerland Ltd
Power Electronics and MV Drives
Austrasse
CH-5300 Turgi

Abstract – **This paper presents the analysis of the Active Neutral-Point-Clamped 5-Level converter (ANPC5L) with regards to the total harmonic distortion (THD) for high speed, high power applications. A 5MW machine with fundamental frequency of 500Hz is considered. The converter can be switched up to 2kHz, thereby making the switching frequency to fundamental frequency ratio in the range of 3-4. Different optimized pulse patterns (OPP) are studied for this case. It is shown that no extra filter is necessary to limit the THD in the considered application, when applying the proposed pulse patterns. Topology specific issues, such as the floating capacitor voltage balancing and the switching frequency of the devices, are investigated in detail for the proposed pulse patterns. The results are compared with a traditional pulse width modulation (PWM) approach.**

Index Terms: **Selective harmonic elimination, optimized pulse patterns, multilevel converters, ANPC, floating capacitor balancing.**

I. INTRODUCTION

The topology under consideration is the 5-level active neutral-point-clamped converter in Fig. 1, which has been introduced in [1]. This new topology only needs one floating capacitor to produce the five different output voltage levels. The redundant switching states are used to balance the capacitor, while providing the desired output voltage. The definition of the switching states and the impact on the floating capacitor voltage have been presented in [1]. They are repeated in Table I. It can be seen that only the middle voltage levels $-V_{dc}/2$ and $V_{dc}/2$ affect the floating capacitor. The appropriate switching state for a charge or discharge of the capacitor is chosen according to the actual current direction. The switching devices S_5 to S_8 are chosen to be IGCTs as they must withstand double the voltage rating of S_1 to S_4 and only need to switch at the fundamental frequency.

The ANPC5L converter is assumed to be integrated into a 5MW power conversion system, which is presented in Fig. 2. The high speed generator has a fundamental frequency of 500Hz. A power conversion system operating at such a high frequency can be significantly reduced in size. However, a smaller generator provides a reduced rotor area, which makes cooling more difficult. It is therefore of great importance that the current harmonics are kept low in order to reduce power losses. With this high frequency, only a small number of

switching pulses can be generated during one fundamental period, which results in a switching frequency to fundamental frequency ratio of 3-4. Therefore, PWM cannot provide acceptable results. The final goal is to run the introduced system with a current THD of less than 5% without the use of an additional filter. A minimum of 35% inductance is common in the considered generator.

Many papers have reported that the use of optimized pulse patterns is a well-known approach to operate a power converter with low losses [2]-[9]. The most popular method is known as selective harmonic elimination (SHE) where certain harmonics can be fully eliminated by proper choice of the switching angles. In [3], the analysis and experimental verification of a 2-level converter have been carried out. In [4] and [5], the equations of a 3-level and 5-level converter have been derived. The result of such an analysis is always a set of nonlinear transcendental equations.
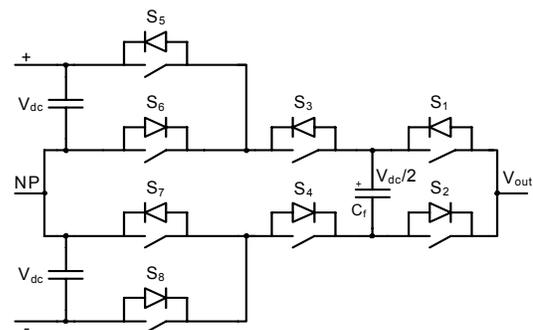

Fig. 1. ANPC5L converter topology

TABLE I
SWITCHING STATES AND IMPACT ON THE FLOATING CAPACITOR VOLTAGE

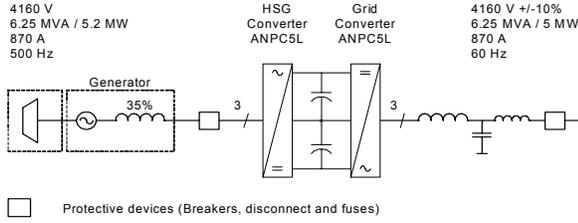| Cell 3			Cell 2		Cell 1			Cell Voltages	Phase Voltage	Effect on C_f		Switching State
S8	S7	S6	S5	S4	S3	S2	S1			I>0	I<0	
1	0	1	0	1	0	1	0	$-V_{dc}$	$-V_{dc}$	-	-	V1
1	0	1	0	1	0	0	1	$-V_{dc}+V_{dc}/2$	$-V_{dc}/2$	discharge	charge	V2
1	0	1	0	0	1	1	0	$-V_{dc}/2$	$-V_{dc}/2$	charge	discharge	V3
1	0	1	0	0	1	0	1	0	0	-	-	V4
0	1	0	1	1	0	1	0	0	0	-	-	V5
0	1	0	1	1	0	0	1	$V_{dc}/2$	$V_{dc}/2$	discharge	charge	V6
0	1	0	1	0	1	1	0	$V_{dc}-V_{dc}/2$	$V_{dc}/2$	charge	discharge	V7
0	1	0	1	0	1	0	1	V_{dc}	V_{dc}	-	-	V8

Fig. 2. Investigated power conversion system

Different approaches to solve these sets of nonlinear equations have been applied and reported in various publications. One of them is the mathematical theory of resultants which has been introduced in [6]. In [7], the same method has been improved with the use of symmetric polynomials. A general generic algorithm has been introduced in [8]. It solves the same set of equations as in [6] and [7] but provides a simpler formulation of the problem. Another publication proposed the use of a numerical Newton algorithm [9]. A predicting algorithm has been applied by the author to calculate the initial values which are first-order approximations of the exact solutions.

So far, the goal has always been to fully eliminate the low order harmonics in order to reduce the converter losses and THD. However, it could be beneficial to leave a small amount of each harmonic, so that the THD is minimized. This approach can not be performed with selective harmonic elimination but has to be solved numerically using an iterative method (IM).

The set of equations for SHE on a 5-level converter is presented here. In addition, an IM is introduced which finds OPP without the full elimination of harmonics. Furthermore, the 5-level ANPC converter topology specific issues, such as floating capacitor voltage balancing and switching frequency, are investigated with the proposed pulse patterns. The results are presented and verified by simulation results.

II. SELECTIVE HARMONIC ELIMINATION

Several template waveforms for the 5-level converter have been considered and analyzed. The selected waveform type is shown in Fig. 3 and Fig. 4. This waveform template with no pulses in the lower voltage levels was found to be optimal for an operation up to the overmodulation region. All switching instants a_n together form a pulse pattern.

The set of equations for the elimination of harmonics b_n can be obtained by a Fourier series representation of the square waveform. This results in the following general equations:

$$b_1 := \frac{2}{\pi}\left[\cos(a_1) + \sum_{k=2}^{N+1}(-1)^k \cos(a_k)\right] = m \qquad (1a)$$

$$b_n := \frac{2}{n\pi}\left[\cos(na_1) + \sum_{k=2}^{N+1}(-1)^k \cos(na_k)\right], \qquad (1b)$$

where n is the order of harmonics and m represents the modulation index. The latter can be defined as:

$$m = \frac{\hat{V}_1}{V_{dc}}, \qquad (2)$$

where $\hat{V}_1$ represents the amplitude of the fundamental voltage and V_{dc} is half of the total dc-link voltage. It can be seen from (1) that $N+1$ equations with $N+1$ unknowns have to be set up in order to eliminate N harmonics.

Boundary conditions have to be defined to assure the proper square waveforms of Fig. 3 and Fig. 4. The following constraints have been applied:

$$0 \le a_1 \le a_2 \le \ldots \le a_k \le \frac{\pi}{2}. \qquad (3)$$

In this work the total harmonic distortion has always been calculated out of the line current with the following equation:

$$THD = 100 \cdot \frac{\sqrt{\sum\left(I_k \cdot I_k^*\right)}}{|I_1|}. \qquad (4)$$

Here, I_k^* represents the complex conjugated value of the kth harmonic component of the current spectrum.

III. ITERATIVE METHOD

An iterative method has been used to find optimized pulse patterns which do not fully eliminate harmonics, but attempts to find solutions with a minimized THD. The reason for this effort is that it could be beneficial to leave a small part of every harmonic in order to achieve a minimal THD. Moreover, solutions with a larger availability range could arise because of fewer restrictions. In contrast to the SHE approach a small, unknown part of every harmonic remains. Therefore, it is not possible to define a set of equations that can be solved for the solutions.
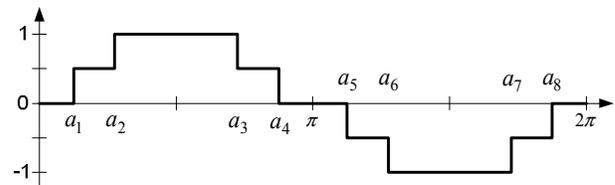

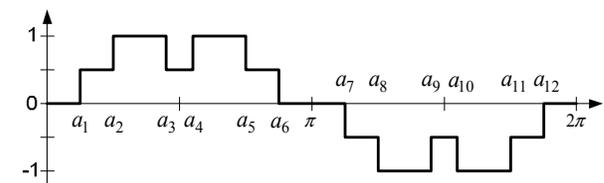Fig. 3. Proper 5-level square waveform, 2 angles

Fig. 4. Proper 5-level square waveform, 3 angles

Instead, for obtaining a starting point, the values of the first *N*-1 angles are changed in small steps and the resulting THD is calculated for each step. Equation (1a), which represents the fundamental, has still to be met. With the initial modulation index, the remaining angle a_N can be calculated using equation (1a). Like this, the number of trials is considerably reduced and the modulation index is met with certainty.

A new search around the obtained starting values is made afterwards in order to achieve the solution angles for the next modulation index step. Pulse patterns are assumed to be continuous. It is therefore sufficient to perform a search in the domain of ±5° around the solution of the previous step. The accuracy can be set to 1° in a first attempt and a fine-tuning around the best solution point can be done in a second step, in order to achieve a precision of 0.1°.

IV. RESULTS - OPTIMIZED PULSE PATTERNS

The methods described in sections II and III have been performed for the 5-level converter with up to four harmonics being eliminated. Analytical as well as numerical solution methods have been used. As the computational effort highly rises with the number of angles, it was not possible to solve a set of equations with more than three unknowns analytically. Results are presented in the following sections for the elimination of one and two harmonics.

A. Selective Harmonic Elimination

1) Elimination of the 5th harmonic: Two solutions could be found for the elimination of the 5th harmonic. The OPP are shown in Fig. 5(a) and (b), whereas the solution in Fig. 5(b) is only valid in a small range of $0.61 \leq m \leq 0.71$.

2) Elimination of the 5th and 7th harmonics: Fig. 5(c)-(e) present the solutions found for the elimination of the 5th and 7th harmonics. Three different pulse patterns could be found, but all of them are only valid in a small modulation index range.

3) Elimination of further harmonics: The additional elimination of the 11th and 13th harmonics was possible within some limited range of the modulation index. Several solutions could be found and approved.

B. Iterative Method

1) Pulse patterns with two angles: One dominating solution could be obtained by the IM for a pulse pattern with two angles. It is presented in Fig. 6(a). The pulse pattern looks similar to the one in Fig. 5(a) obtained by SHE, except for some regions around *m*=0.7 and *m*=1.1.

This solution could be found for the whole modulation index range, but because of the boundary conditions, the second angle got clamped at 90° until a modulation index of *m*=0.35. Still, solution points could be obtained even with a clamped angle, whereas the SHE approach simply was not able to obtain a result.

2) Pulse patterns with three angles: Two solutions using a pulse pattern with three angles are presented in Fig. 6(b) and (c). The solution in Fig. 6(c) is similar to the one in Fig. 5(c), however, it is valid for the modulation index range up to 1.15 because the third angle got clamped at 90°. A second solution without clamped angle is presented in Fig. 6(b).

C. Comparison of SHE and IM

1) Pulse patterns with two angles: The pulse patterns of Fig. 5(a) and Fig. 6(a) are compared in this section. They are revisualized in Fig. 7. The modulation index range is chosen from 0.56 to 1.15 for a better survey. It can be seen, that the THD, which is shown in the middle part of the plots, is actually better in the regions where the IM found a different pulse pattern. The reason for this low THD is a reduced 7th harmonic in case of the IM as can be seen in the bottom part of the plots. Even if the 5th harmonic is still present, the 7th is so much reduced that the total effect on the THD is positive.

2) Pulse patterns with more than two angles: For pulse patterns with more than two angles it could be observed that the IM encountered mostly the same solutions as the SHE approach. However, with the IM, different solutions could be found and all of them showed a large validity range.

On the other hand, the calculation of pulse patterns with a large number of angles becomes difficult as the number of trials highly increases with the number of angles. A large computation time or a strong computer has to be considered for such cases.
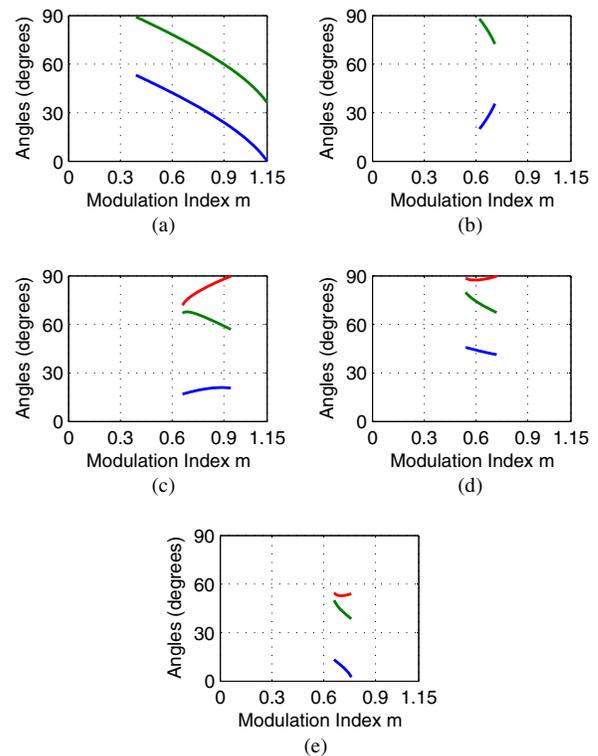

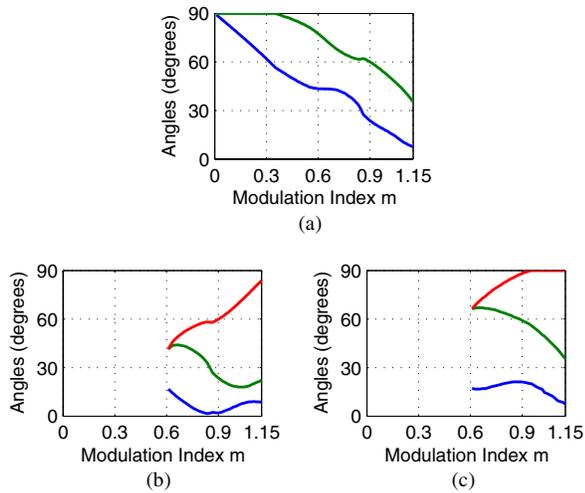Fig. 5. Solutions from the SHE approach using two and three angles

Fig. 6. Solutions from the IM using two and three angles

Fig. 7. Comparison of OPP with two angles

D. Switch Blanking Time

The blanking time of the switching devices can be introduced in order to maintain more real conditions. Due to the fact that the fundamental frequency is 500Hz, the blanking time becomes most significant in the search for OPP. A blanking time of 30μs was used as a realistic value for IGCT devices, which leads to a minimal allowed gap between two switching angles of 5.4°. The effect of this additional restriction is that the validity range of the found pulse patterns is even more compressed. This emphasizes again the advantages of an IM, where new restrictions can be comprised in the search for optimized pulse patterns.

E. Comparison of OPP and PWM pulse patterns

A simulation model has been built in order to validate the mathematically derived results and to compare the found pulse patterns with PWM pulse patterns. Fig. 8 shows the simulation results for a modulation index of 1.06. The square waveforms, line currents and spectra are shown for both, PWM pulse patterns and optimized pulse patterns with three angles.

A large difference in the current waveform can be observed. The examination of the corresponding spectra emphasizes the better results of the optimized pulse patterns with a THD of 3.86, compared to a THD of 8.8 for the PWM pulse patterns.

V. FLOATING CAPACITOR OPTIMIZATION

An optimization for the floating capacitor's capacitance has been made. The goal of this part of research was to find pulse patterns, which are optimized for the floating capacitor of the 5-level converter. Because only the middle voltage levels –1/2 and +1/2 affect the capacitor, a pulse pattern with short middle voltage levels is preferred. A general guideline is to allow up to ±10% voltage deviation.
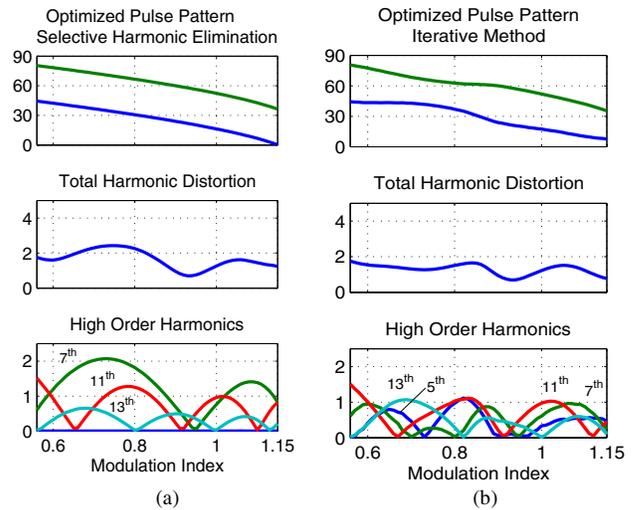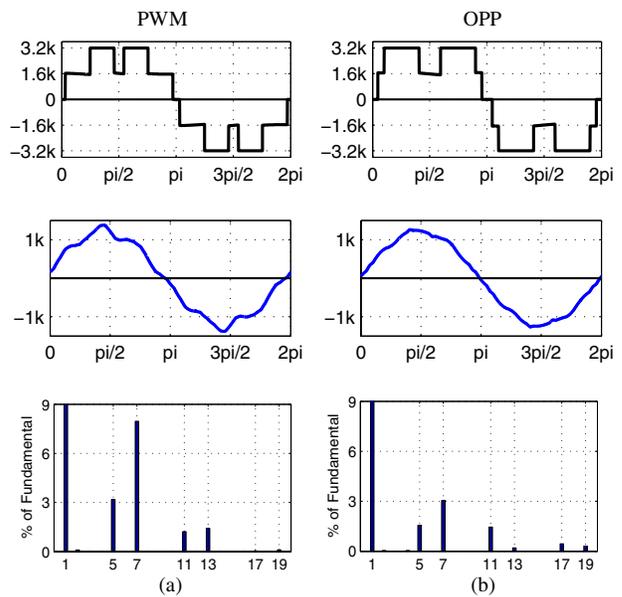

Fig. 8. Simulation results for PWM and optimized pulse patterns

The selective harmonic elimination approach cannot be used to find such OPP because the solutions are predefined by equations (1). There exist only a limited number of solutions for a given number of switching angles. Therefore, the single pulse patterns can only be judged as useful or not useful for a certain capacitor size. An iterative method however appears to be most suitable for finding appropriate solutions. Instead of validating all possible combinations of angles for the smallest THD, the expected voltage deviation is calculated and the combination with the smallest effect on the capacitor is chosen.

The equation for the calculation of the voltage deviation can be stated as in (5) where C represents the capacitance, I_{rms} the rms line current and w the rotating fundamental frequency. a_i and a_{i+1} mark the beginning and the end of a middle voltage level.

$$dV_c = \frac{\sqrt{2}}{C} I_{rms} \int_{t_i}^{t_{i+1}} \sin(\omega t)dt$$

$$= \frac{\sqrt{2}}{\omega C} I_{rms} [\cos(a_i) - \cos(a_{i+1})]$$

(5)

Fig. 9 presents the obtained pulse patterns for two different capacitor sizes. Fig. 9(a) shows in comparison to Fig. 7(b) that the gap between the angles is already slightly shortened at small modulation indices. A capacitance of 1mF was used for the calculations. To obtain the solution shown in Fig. 9(b) a capacitance of only 400µF was used. The middle voltage levels are further shortened in order not to exceed the proposed voltage deviation limits of 10%. The total harmonic distortion has markedly risen but is still below the demanded limit of 5%.

A trade-off between a low THD and a small effect on the floating capacitor voltage could be the best overall solution for the 5-level ANPC converter. Both demands can be met at the same time by correct setup of restrictions in the iterative method.

VI. SWITCHING FREQUENCY

A closer investigation on the optimal sequence of switching states has been done for the 5-level ANPC converter. It was found that the expected average switching frequency for the fast-switching IGBT devices can be reduced by the amount of the fundamental frequency with a minor change in the sequence of switching states.

Basically, the states V4 and V5, which were defined in [1], have to be set as shown in Fig. 10. Like this, no change in the switching state occurs at 0 and Pi. The functioning of this new sequence could be successfully tested with the simulation model.

Fig. 9. Shortening of the middle voltage level

VII. POWER FACTOR

The effect of different power factors on the operation of the 5-level converter has been studied. It could be shown that the power factor does not influence the balancing of the floating capacitor voltage. Always the most appropriate switching state is chosen, independent of the phase shift of voltage and current. However, the power factor has an influence on the size of voltage deviation.

Fig. 11 shows a simulation plot of the voltage deviation across the full range of power factor. As can be seen, the balancing of the capacitor voltage is always working as expected. Fig. 12 and Fig. 13 show the waveforms at power factor 1 and power factor 0 where a maximal and minimal influence on the capacitor voltage can be observed. The largest deviation is always reached when the maximum of the current is situated across the middle voltage level with the longest duration. This conclusion can also be derived from equation (5).
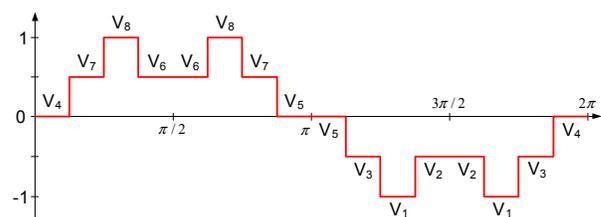

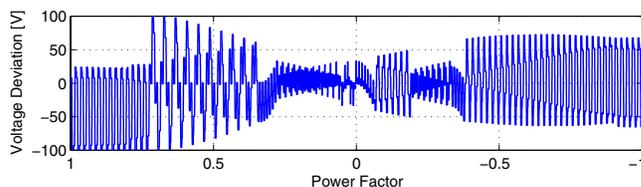Fig. 10. Proposed sequence of switching states

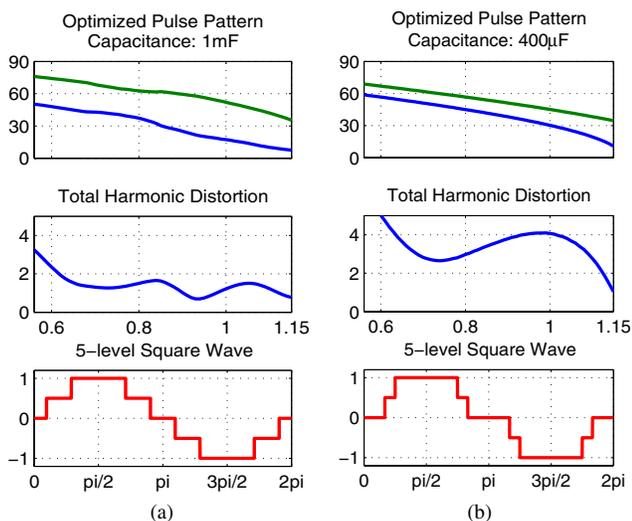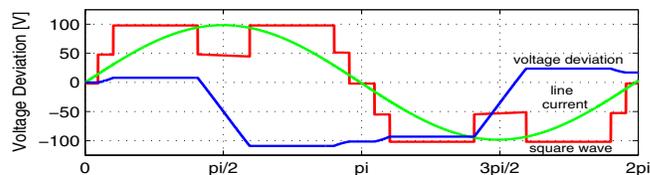Fig. 11. Voltage deviation at different power factors

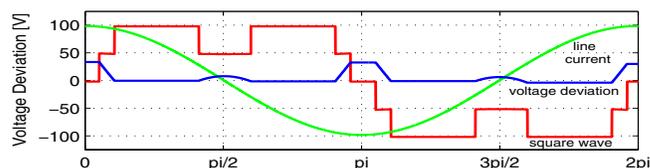Fig. 12. Maximal effect on the capacitor voltage

Fig. 13. Minimal effect on the capacitor voltage

2591

VIII. CONCLUSION

An analysis of the Active Neutral-Point-Clamped 5-Level converter has been presented in this paper. Optimized pulse patterns have been found with both, a selective harmonic elimination approach and an iterative method. It could be demonstrated that the full elimination of certain harmonics is not always the best solution with respect to the total harmonic distortion. Moreover, the iterative method found more pulse patterns, which were normally valid in a larger modulation index range. With the aid of a simulation model it could be proven that the introduced power system with fast-rotating generator can be operated without additional filter.

A search for suitable pulse patterns regarding the floating capacitor has been introduced and results have been presented. The iterative method is capable of simultaneously considering the THD and the effect on the capacitor voltage while obtaining optimized pulse patterns.

A closer investigation on the sequence of switching states has been done for the converter under consideration. A new sequence could be found, which reduces the frequency of a part of the switching devices by the amount of the fundamental. The new sequence was successfully tested with a simulation model.

It could be shown that the power factor does not influence the capacitor voltage balancing of the 5-level converter. However, it has an influence on the size of the voltage deviation. This fact can be considered in the selection of optimized pulse patterns when the expected power factor is known.

X. REFERENCES

[l] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper and N. Celanovic, "Active Neutral-Point-Clamped Multilevel Converters," in Power Electronics Specialists, 2005 IEEE 36th Conference, June 2005, pp. 2296-2301

[2] H.S. Patel, R.G. Hoft, "Generalised Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I – Harmonic Elimination," *IEEE Trans. Industry Applications*, vol. 9, June 1973, pp. 310-317.

[3] V.G. Agelidis, A. Balouktsis, I. Balouktsis, C. Cossar, "Multiple Sets of Solutions for Harmonic Elimination PWM Bipolar Waveforms: Analysis and Experimental Verification," *IEEE Trans. Power Electronics*, vol. 21, no. 2, Mar. 2006, pp. 415-421.

[4] J.N. Chiasson, L.M. Tolbert, K.J. McKenzie, Z. Du, "A Complete Solution to the Harmonic Elimination Problem," *IEEE Trans. Power Electronics*, vol. 19, no. 2, Mar. 2004, pp. 491-499.

[5] V.G. Agelidis, A. Balouktsis, I. Balouktsis, C. Cossar, "Five-Level Selective Harmonic Elimination PWM Strategies and Multicarrier Phase-Shifted Sinusoidal PWM: A Comparison," at IEEE PESC Conference in Recife, Brasil, June 2005, pp. 1685-1691.

[6] J.N. Chiasson, L.M. Tolbert, K.J. McKenzie, Z. Du, "Eliminating Harmonics in a Multilevel Inverter using Resultant Theory," in Power Electronics Specialists, 2002 IEEE 33th Conference, June 2002, pp. 503-508.

[7] J.N. Chiasson, L.M. Tolbert, K.J. McKenzie, Z. Du, "Elimination of Harmonics in a Multilevel Converter Using the Theory of Symmetric Polynomials and Resultants," *IEEE Trans. Control Systems*, vol. 13, no. 2, Mar. 2005, pp. 216-223.

[8] B. Ozpineci, L.M. Tolbert, J.N. Chiasson, "Harmonic Optimization of Multilevel Converters using Generic Algorithms," *IEEE Trans. Power Electronics*, vol. 3, no. 3, Sept. 2005, pp. 92-95.

[9] J. Sun, H. Grotstollen, "Solving Nonlinear Equations for Selective Harmonic Eliminated PWM using Predicted Initial Values," Int. Conference on Power Electronics and Motion Control, Nov. 1992, pp. 259-264.