A Novel Concept for Mains Voltage Proportional Input Current Shaping of a VIENNA Rectifier Eliminating Controller Multipliers

Part I: Basic Theoretical Considerations and Experimental Verification

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Abstract. Part I of this paper proposes a novel mains voltage proportional input current control concept eliminating the multiplication of the output voltage controller output and the mains AC phase voltages for the derivation of mains phase current reference values of a three phase/level/switch PWM (VIENNA) rectifier system. Furthermore, the concept features a low input current ripple amplitude as, e.g., achieved for space vector modulation, a low amplitude of the 3rd harmonic of the current flowing into the output voltage center point and a wide range of modulation. The practical realization of the analog control concept as well as experimental results for application with a 5kW prototype of the PWM rectifier are presented. Furthermore, a control scheme which relies only on the absolute values of the input phase currents and a modified control scheme which does not require information about the mains phase voltages and therefore is ideally suited as a basis for the development of an integrated control circuit for three phase power factor correction is presented. In Part II of the paper a comparison of the experimental results of a conventional average current mode control scheme employing controller multipliers and of the proposed control scheme in case of a heavily unbalanced mains as well as for two phase operation is treated in detail.

I.1 Introduction

Conventional single-phase and three-phase power factor correction systems employ analog multipliers for the generation of the input current reference values for the current mode controllers. But, as shown in [1]-[4] ohmic mains behavior can be achieved for single-phase boost type PWM rectifier systems in continuous conduction mode (CCM) without measurement of the input voltage and without a multiplication in the output voltage feedback loop.

According to [3] and [4] there the relative off-time of the power transistor $d'T_P$ ($T_P = 1/f_P$ denotes the pulse period) is defined by comparing the actual input current with a carrier signal with switching frequency. For given amplitude $\hat{I}_D$ of the saw-tooth shaped carrier signal and neglection of the ripple component of the input current, i.e.,

$$ i_N \approx \bar{i}_N \qquad (\bar{i}_N = \frac{1}{T_P} \int_0^{T_P} i_N \mathrm{d}t \ ) \tag{I.1} $$

$$ \frac{i_N}{\hat{I}_D} = d' , \tag{I.2} $$

and for taking into consideration the stationary equilibrium of the input voltage u_N and the local average value $\bar{u}'$ of the voltage u',

$$ u_N = \bar{u}' = d' u_O \tag{I.3} $$

(as valid for CCM, in case the output voltage ripple is neglected, i.e. $u_O \approx \bar{u}_O$ is assumed), the proportionality of i_N and u_N is obtained by

$$ u_N = i_N \frac{u_O}{\hat{I}_D} \tag{I.4} $$

and can be described by an equivalent input resistance value

$$ R_N = \frac{u_O}{\hat{I}_D} \quad . \tag{I.5} $$

Consequently, the input current and/or the power consumption of the system can easily be adjusted by the output voltage control by changing the amplitude of the carrier signal $\hat{I}_D$. A lower amplitude of the carrier signal
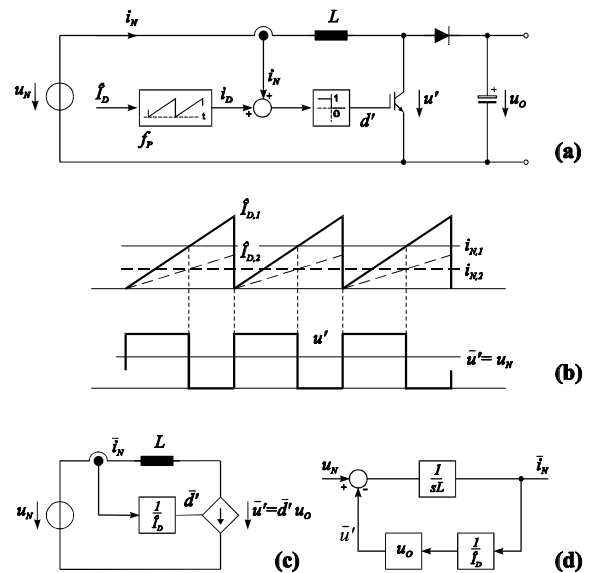

Fig.I.1: Basics of an input voltage proportional guidance of the input current i_N of a PWM boost converter system by means of a proportional relationship of the turn-off interval d' of the power transistor and i_N. Structure of the power circuit and block diagram of the control **(a)**, detailed time behavior of the input current i_N, of the carrier signal i_D and of the resulting drive signal of the power transistor **(b)**, equivalent circuit of the input stage **(c)** and control oriented block diagram **(d)**.

leads to $d' = u_N / u_O$ at smaller values of the input current, cf. $i_{N,2}$ in **Fig.I.1**(b). This system function can be realized without a multiplier in the control circuit (cf., e.g., Fig. 10 in [4]).

The dynamic behavior of the system corresponds in the first approximation (for neglection of the low frequency output ripple voltage due to the pulsation of the output power level with twice the mains frequency) to a first order delay [4]

$$i_N(s) = \frac{u_N(s)}{R_N} \frac{1}{1 + s\dfrac{L}{R_N}} , \qquad (I.6)$$

this can be clearly explained by the negative feedback of an integration element $1/sL$ representing the input inductor via the modulation stage (an increase of the input current i_N results in an increase of d' and/or of the voltage $\overline{u}'$ and subsequently in a decrease of the voltage $u_N - \overline{u}'$ which is applied to the inductor L, cf. Fig.I.1(b) and Fig.I.1(c). Fig.I.1(d) can be interpreted as a control loop having u_N as reference value. As shown in [4] the unity gain bandwidth of the control loop results for common dimensioning of the system typically in $f_P/30$, hence the considerations for processes with mains frequency can be in a quasi-stationary manner; therefore, the input current of the system is guided directly proportional to the input voltage without the requirement of an analog or digital multiplier for generating reference current waveforms.

In this paper this basic control concept now shall be applied and investigated in modified form [7] in connection with a three-phase/switch/level PWM (VIENNA) rectifier (cf. **Fig.I.2**, [8]), which already is well established in the industry for three-phase power factor correction like the boost converter for single phase applications. Advantages of the system are a low blocking voltage stress on the power semiconductors and a high efficiency besides a low ripple with switching frequency of the sinusoidal mains current.

In the following in **section I.2** the realization of the control circuit in analog technique is described. In **section I.3** a modification of the proposed control concept which does not require a sensing of the mains phase voltages and therefore is ideally suited as a basis for the development of an integrated control circuit for three phase power factor correction is proposed; furthermore, a control scheme relying on the absolute values $|i_{N,i}|$ of the input phase currents is discussed. **Section I.4** shows the experimental investigation of the control concepts in connection with a 5kW prototype of the PWM rectifier. There, special attention is paid to the quality of the guidance of the input currents in the vicinity of the zero-crossings and at light load (resulting in discontinuous conduction mode).

I.2 Multiplier Free Control Concept

Fig.I.4 shows the block diagram of the two-loop control of the VIENNA Rectifier incorporating the proposed multiplier free input phase current control concept [7] in the inner loop. The outer loop controls the total value of the output voltage to a constant value by proper adjustment of the amplitude of the carrier signal $\hat{I}_D$ and balances the values of the two partial output voltages by means of the zero-current component i_0.

The basic operating behavior of the inner current control loop is identical to single-phase power factor correction when adding a connection between the output voltage center point and the mains star point what results in a decoupling of the phases.
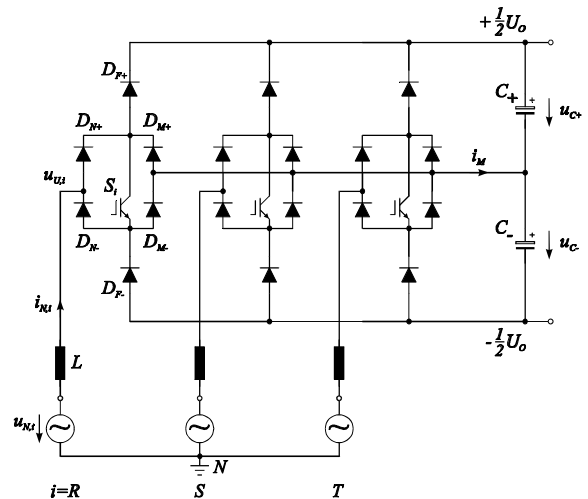

Fig.I.2: Structure of the power circuit of the PWM (VIENNA) rectifier system.

Then, for positive mains phase voltages the (single-phase) boost converter topology is formed by the input inductor L (with series diode D_{N+}), the power transistor S_i (with series diode D_{M-}), the free wheeling diode D_{F+} and the output capacitor C_+; for negative mains phase voltages the boost structure is formed by the input inductor L (with D_{N-}), S_i (with D_{M+}), D_{F-} and C_-. However, due to deriving the off-time of the power transistors directly from the ac input current $i_{N,i}$ (instead of taking the absolute values) one now has to shift the triangular carrier signal by $\pm\hat{I}_D$ ($+\hat{I}_D$ for positive phase current, $-\hat{I}_D$ for negative phase current). Furthermore, an inversion of the switching decisions s_i' of the modulator stages in dependency of the signs of the input phase currents $i_{N,i}$ and/or of the input phase voltages $u_{N,i}$ ($u_{N,i}$ prop. $i_{N,i}$) has to be performed.

Because the actual system does not show a connection between the mains neutral point and the capacitive rectifier output voltage center point a coupling of the phases must be taken into consideration. According to

$$i_{N,R} + i_{N,S} + i_{N,T} = 0 \qquad (I.7)$$

and/or

$$\frac{di_{N,R}}{dt} + \frac{di_{N,S}}{dt} + \frac{di_{N,T}}{dt} = 0 \qquad (I.8)$$

the change of a switching state of a rectifier bridge leg and/or the change of a phase current takes influence also on the currents of the two other phases. Therefore, the switching decisions of the phases are coordinated advantageously by using a single carrier signal i_D with triangular shape for all three phases as, e.g., for ramp comparison current control (regarding the drawbacks of a sawtooth shaped carrier signal please refer to [9]). The system in this case advantageously has the property of a natural stability of the partition of the total output voltage U_O to u_{C+} and u_{C-}. However, in order to ensure high system reliability, additionally an active symmetry control of the partial output voltages is provided by offsetting all measured phase currents by i_0. As shown in [8] i_0 directly results in a global average value I_M of the center point current i_M and therefore can be used for guaranteeing $u_{C+} = u_{C-} = {}^1/_2 U_O$.

Using directly the actual sinusoidal input phase current for the PWM modulator stage would allow the formation of a fundamental of the maximum rectifier input phase voltage of only $\hat{U}_{N,max} = u_O / 2$. Therefore, besides low-pass filtering for suppression of the switching frequency ripple the measured actual phase currents $i_{N,i}$ are extended by a zero-sequence

component $i_{0,m}$ with three-times the mains frequency [10] (cf. **Fig.I.3**), ($i_{N,i}' = i_{N,i} + i_{0,m}$; $i = R, S, T$). This (theoretically) increases the modulation limit to

$$\hat{U}_{N,\max} = \frac{2}{\sqrt{3}} \frac{u_O}{2},$$ and results in a significant reduction of the input

current ripple amplitude and of the amplitude of the 3rd harmonic of the center point current i_M (as compared to purely sinusoidal modulation). We would like to point out that despite the addition of $i_{0,m}$ the phase current waveforms are still guided sinusoidally, i.e., proportional to the phase voltages; $i_{0,m}$ only leads to the formation of a zero sequence component of the rectifier input voltage which according to Eq.(I.7) does not result in a current flow.
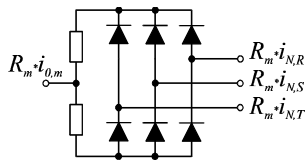

Fig.I.3: Principle of generation of the zero-sequence component $i_{0,m}$ with a pronounced 3rd harmonic from the measured input phase currents. In the practical realization the diodes are replaced by ideal diodes realized by means of operational amplifiers.

I.3 Control Methods Without Multipliers and Without Input Voltage Sensing

The disadvantage of the realization shown in Fig.I.4 is the need of the determination of the sign of the input phase voltages for shifting the triangular-shaped carrier signal and for the inversion of the switching signals s_i' with line frequency. Therefore, a realization of a control concept which relies only on the absolute values $|i_{N,i}|$ of the input phase currents would be of special interest. A block diagram of a possible realization is given in **Fig.I.5**. However, in this case unfortunately the triangular shaped carrier signal $\hat{I}_D$ needs to be shifted by 180° in switching frequency (inverted) in case of negative input phase voltages and/or negative input phase currents for a minimization of the input current ripple and/or of the size of the input inductors as has been proven by theoretical considerations simulation (details are omitted here for the sake of brevity). This again gives a reason for detecting the signs of the input phase voltages or the signs of the input phase currents where the latter could cause problems with light loads and/or in idle mode. But, advantageously that the total realization effort is comparably low.

An alternative is to generate not only a single triangular carrier signal i_D but to generate a positive and a negative carrier where both signals are synchronized and in phase. These two signals are compared directly with the measured (bipolar) input phase currents by separate comparators. The switching signals s_i then can be derived by a simple combinatorial logic, i.e. dependent on the sign of the comparison and a type of transistor drive circuit (high or low active) by an AND, OR, NAND or NOR Gate, **Fig.I.7**. This allows to operate the whole control circuit without a detection of the sign of the input voltage and/or a derivation of the sign information from the input current (**Fig.I.6**). It is necessary to point out that there is also no need of a recognition of sectors of the mains period (as defined by the relationship of the mains phase voltages) as described in [5] what could probably cause problems in case of heavily unbalanced mains conditions and/or in case of a phase loss.
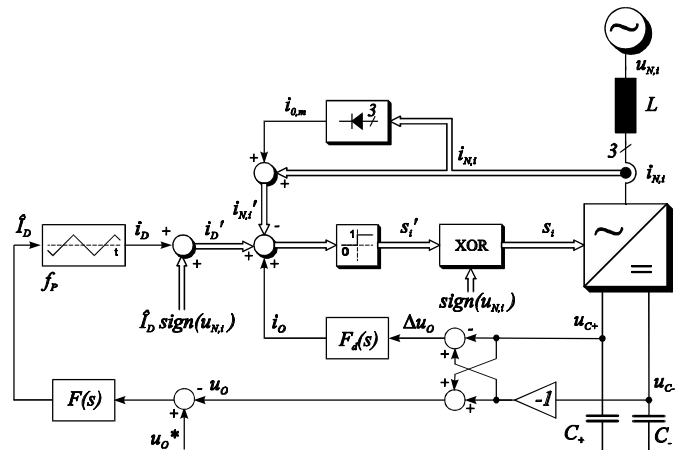

Fig.I.4: Structure of the proposed multiplier free current control concept [7]. Signal paths being equal for different phases are shown by double-lines.
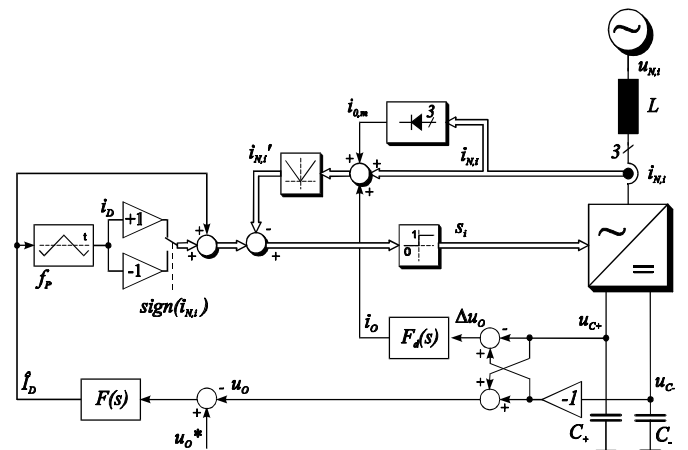

Fig.I.5: Structure of a multiplier free current control concept which relies on the absolute values $|i_{N,i}|$ of the input phase currents and which does not require a detection of the sign of the input phase voltages. Signal paths being equal for different phases are shown by double-lines.
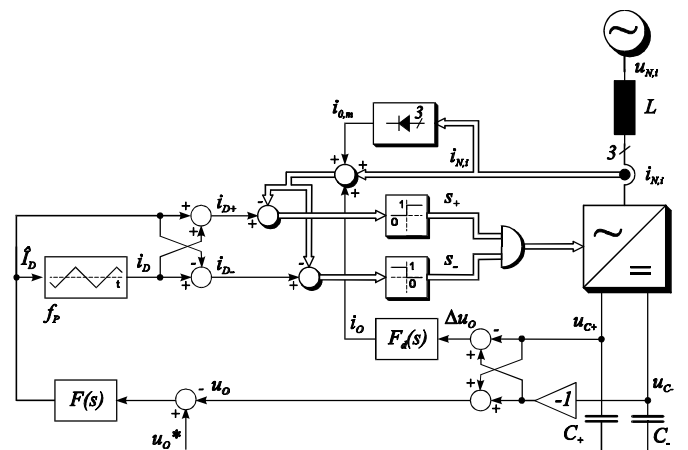

Fig.I.6: Structure of a multiplier free current control concept employing two unipolar carrier signals i_{D+} and i_{D-} where no information about the sign of the input voltages or currents is required.
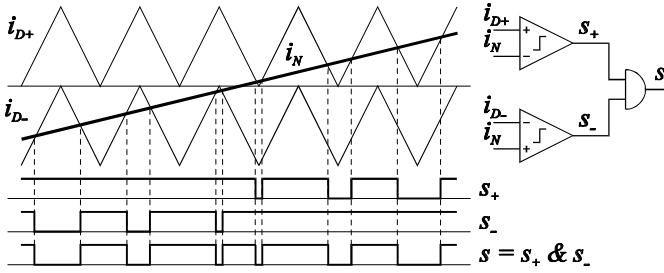
Fig.I.7: Generation of a phase switching function s by intersection of the corresponding phase current i_N with a positive carrier signal i_{D+} and a negative carrier signal i_{D-}. The carrier signals i_{D+} and i_{D-} are common for all three phases.

I.4 Experimental Results

The investigation of the multiplier free control concept was done in the first step with the structure shown in Fig.I.4 for two different load conditions (cf. **Tab.I.1**(a): full load; (b): half the nominal load) in order to show the basic performance of the concept. In **Fig.I.8** (a) and (d) show one of the three mains ac phase voltages $u_{N,R}$ and the corresponding converter input inductor current $i_{N,R}$ recorded in peak detection mode for the demonstration of the ripple of the inductor current; furthermore, $i_{N,R}$ is recorded in high-resolution mode in order to show the current in the mains resulting after adequate EMI-filtering. In Fig.I.8. (b) and (e) the modulating input current $i_{N,R}$' (zero-sequence component $i_{0,m}$ added to the low-pass filtered actual current $i_{N,R}$), the triangular carrier signal i_D' shifted according to sign($u_{N,R}$) and the switching signal s_R' of the PWM stage for one fundamental period are depicted. Fig.I.8 (c) and (f) show the time behavior in the vicinity of the zero-crossing of a phase current.

	$U_{N,rms}$ [V]	I_N [A]	P_N [kW]	l	THD V [%]	THD A [%]	U_O [V]	I_O [A]	P_O [kW]	h [%]
(a)	400	7.68	5.30	1.000	2.7	3.2	676	7.60	5.14	97.0
(b)	400	3.59	2.47	0.999	2.7	3.2	677	3.55	2.40	97.3

Tab.I.1: Operating parameters for the experimental investigations (cf. Fig.I.8) of the multiplier free control system according to Fig.I.4 for two different input power levels.

	$U_{N,rms}$ [V]	I_N [A]	P_N [kW]	l	THD V [%]	THD A [%]	U_O [V]	I_O [A]	P_O [kW]	h [%]
(a)	400	7.60	5.25	0.999	2.7	3.1	675	7.57	5.11	97.3
(b)	400	0.56	0.389	0.986	2.7	11.2	677	0.54	0.366	94.0

Tab.I.2: **(a)**: Operating parameters for the experimental investigations (cf. Fig.I.9) of the multiplier free control system according to Fig.I.6; **(b)**: discontinuous conduction mode (DCM) corresponding to Fig.I.10.
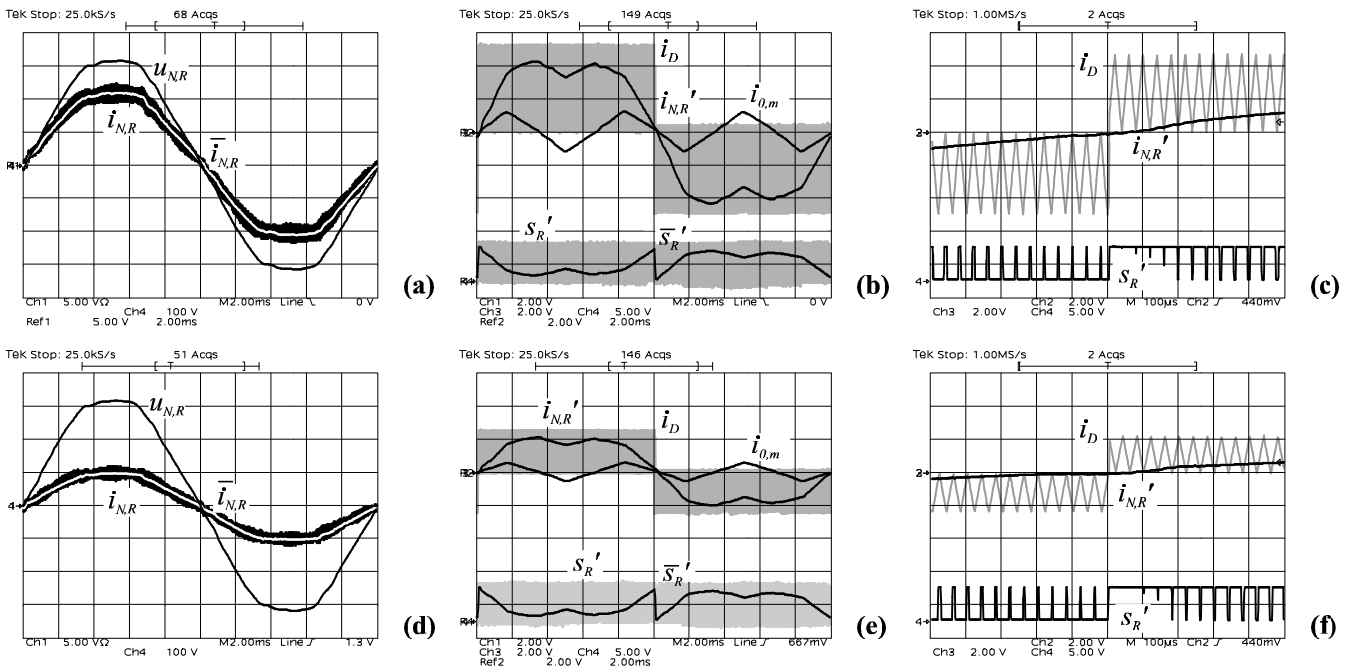

Fig.I.8: Experimental analysis of the control concept according to Fig.I.4 in connection with a 5kW prototype of the VIENNA Rectifier. Operating parameters: $U_{N,rms}$ = 400V (line-to-line voltage), U_O = 675V, Output power P_O = 5.14kW for **(a)**, **(b)**, **(c)**, P_O = 2.40kW for **(d)**, **(e)**, **(f)**. **(a)** and **(d)**: mains ac phase voltage $u_{N,R}$ and corresponding input current $i_{N,R}$; (recorded in peak detection mode and in high resolution mode in order to attenuate the switching frequency ripple, 5A/div) **(b)** and **(e)**: modulating input current $i_{N,R}$' (zero-sequence component current $i_{0,m}$ added to the low-pass filtered actual current $i_{N,R}$), triangular carrier signal i_D' shifted according to sign($u_{N,R}$) and switching signal s_R' of the PWM stage for one fundamental period; **(c)** and **(f)**: details of waveforms shown in (b) and (e) in the vicinity of the zero-crossings of the phase current.
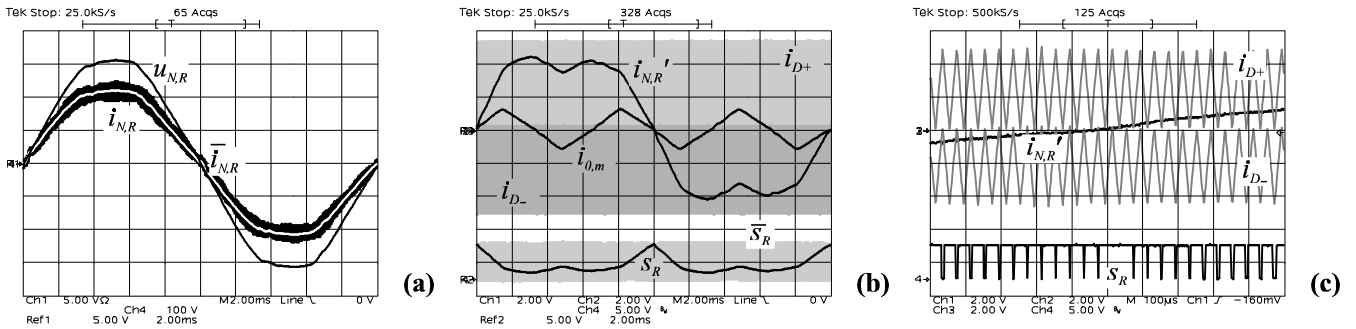
Fig.I.9: Experimental analysis of the control concept according to Fig.I.6 in connection with a 5kW prototype of the VIENNA Rectifier. Operating parameters: $U_{N,rms}$ = 400V (line-to-line voltage), U_O = 675V, output power P_O = 5.11kW. Mains ac phase voltage $u_{N,R}$ and corresponding input current $i_{N,R}$; (recorded in peak detection mode and in high resolution mode in order to attenuate the switching frequency ripple, 5A/div) **(a)**, modulating input current $i_{N,R}'$ (zero-sequence component $i_{0,m}$ added to the low-pass filtered actual current $i_{N,R}$), triangular carrier signals i_{D+} and i_{D-} and switching signal s_R of the PWM stage for one mains period **(b)**; **(c)**: details of waveforms shown in (b) in the vicinity of the zero-crossings of the phase current.

These results lead directly to the control concept according to Fig.I.6 (no need of input phase voltage detection), which is investigated in the following in **Fig.I.9** for full load conditions as detailed in **Tab.I.2**.
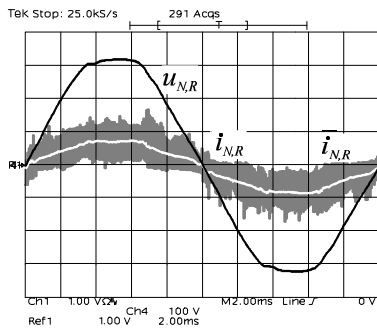

Fig.I.10: Input inductor current $i_{N,R}$ (1A/div) recorded in peak detection mode and the corresponding average value $\bar{i}_{N,R}$ (recorded using high resolution mode) in partly discontinuous conduction mode (light load) according to Tab.I.2(b).

Fig.I.10 shows the input phase voltage $u_{N,R}$ and the corresponding input inductor current recorded in peak detection mode in order to show the input current ripple and the mode of operation with discontinuous conduction mode (DCM) occurring at very light loads (P_O=366W). The average value of the input current is still of approximately sinusoidal shape (and/or proportional to the phase voltage) with a total harmonic distortion of *THD_A* =11.2% and a power factor l=0.986. Therefore, although the theory compiled in section I.1 does not hold in DCM the system shows a relatively good performance at light loads (a detailed investigation of the performance of the control concept in DCM will be presented in a future paper). A reason for this also is the nonlinearity of the iron powder cores employed for the input inductors which show the highest inductance values at zero and/or

small current values, correspondingly the systems enters into DCM only at relatively light loads. Also the circumstance, that if one of the input currents is in the vicinity of a zero crossing and therefore discontinuous, the other two phases have according to Eq.(I.7) current values differing from zero and therefore still stay in continuous conduction mode (for operating conditions as shown in Fig.I.10) and since the three phases are not decoupled still force an approximately voltage proportional guidance of all three input currents. The input current would become discontinuous within the whole mains period for low input current amplitudes, but in the realization at hand the converter enters a hickup mode below a defined input power level in order not to control the output voltage to a constant value also in idle mode (at no load every single pulse would increase the output voltage). The behavior of the system in discontinuous conduction mode could be further improved by increasing the switching frequency at light loads as proposed in [11]; this also is treated in detail a research project currently being under way.

I.5 Summary Part I

Part I of this paper presents a novel concept for a mains voltage proportional input current shaping which eliminates analog or digital multipliers in the control loop. The concept features a wide modulation range comparable to space vector modulation by extending the modulating phase current values by a zero-sequence component with a significant 3rd harmonic content. Besides a basic theoretical analysis an experimental verification of the concept is given in connection with a 5kW prototype of the PWM VIENNA Rectifier for symmetric three-phase input.. Also a modified control scheme which relies on the absolute values of the input phase currents and a modified control scheme which directly employs the input phase currents as modulating signals and does not need no information about the signs of the input phase currents and/or voltages are presented and the latter is verified experimentally also for discontinuous conduction mode. The fact, that the converter system behaves like a star-connection of equal ohmic resistors leads now motivates the investigation of the system system behavior also for unbalanced mains conditions which will be given in Part II of this paper.