Evaluation of a Delta-Connection of Three Single-Phase Unity Power Factor Rectifier Modules (Δ-Rectifier) in Comparison to a Direct Three-Phase Rectifier Realization

Part II – Component Stress Evaluation, Efficiency, Control

Johann MINIBÖCK
miniboeck@t-online.at
m-pec
Power Electronics Consultant
A-3752 Purgstall 5
AUSTRIA

Roland GREUL
+41-1-632-5324
greul@lem.ee.ethz.ch

Johann W. KOLAR
+41-1-632-2834
kolar@lem.ee.ethz.ch

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
ETH-Zentrum/ETL/H22
CH-8092 Zurich/SWITZERLAND

Abstract. In this paper the voltage and current stress of a delta-connection of three single-phase boost-type unity power factor rectifier modules *(Δ-Rectifier*) is analyzed in order to perform a design comparable to a direct three-phase three-level six-switch unity power factor (*conventional*) rectifier system. The conduction losses of the power semiconductors are calculated using analytical approximations of the average and rms values of the component currents, the switching losses are taken from previous experimental investigations. Based on this data an overview of the estimated power losses is given for the Δ-Rectifier as well as for the conventional rectifier for 10kW output power, 800VDC output and 320V/400V/ 480V/530V (rms, line-to-line) mains voltage. These investigations finally lead to efficiency and component count figures. Furthermore, special attention is paid to the control of the whole three-phase system including the DC/DC converter output stages of the line-to-line modules of the Δ-Rectifier. Finally, topics of the continuation of the research are identified as, e.g., the realization of a prototype in order to verify the theoretical results experimentally also for unbalanced mains voltage conditions and with nonideal components such as nonlinear input inductors employing iron powder cores and the analysis of a Δ-Rectifier being formed by single-stage SEPIC-type line-to-line modules.

1 INTRODUCTION

Modern high-power telecom power supply modules are designed for a rated output power of typically $P_{O,max}$ = 48V · 200A = 10kW and show a two-stage topology, i.e. a three-phase high power factor rectifier does supply an output-side DC/DC converter.

For the realization of a three-phase unity power factor rectifier in [1] the topology depicted in **Fig.1(a)** has been proposed which is characterized by a delta-connection of three single-phase modules (Δ-Rectifier). Single-phase unity power factor rectifier modules are highly developed and well known in the industry. Furthermore, the Δ-Rectifier shows advantages as high modularity and the possibility to deliver the full output power also in case of a missing mains phase if the diode bridge rectifiers at the inputs of the line-to-line modules are replaced by three-phase thyristor bridge rectifiers (cf. Fig.1: gray shaded components) which do allow a switching over to the two remaining phases in case a mains phase fails.

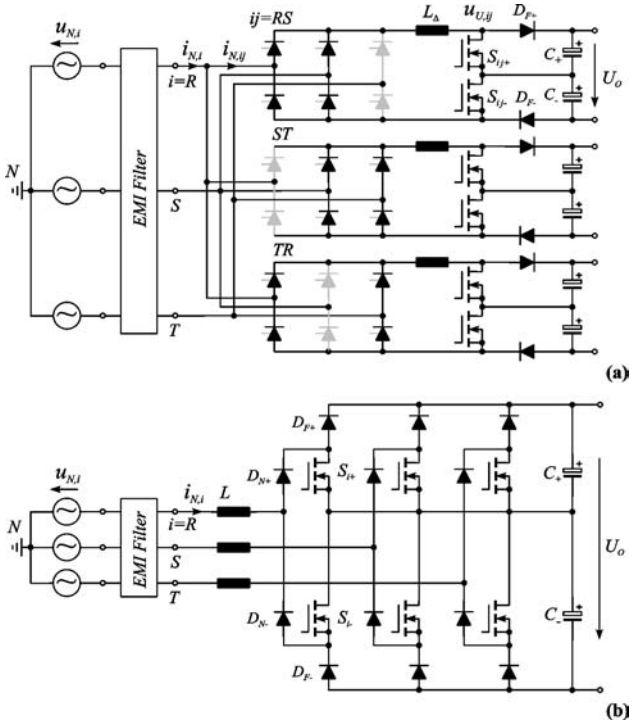

Fig.1: Basic structure of the power circuits of three-phase boost-type unity power factor rectifiers; **(a):** delta connection of single-phase modules (*Δ-Rectifier*), or **(b)** direct three-phase realization as proposed in [3] (denominated as *conventional* rectifier in the following).

In contrast, the output power of a direct three-phase realization of the rectifier [3] as shown in **Fig.1(b)** (denoted as *conventional* rectifier in the following) which can be considered as a first step in the development of the well known VIENNA Rectifier [2] has to be reduced to $P_O = {}^1/_{\sqrt{3}}\, P_{O,max} = 0.58 P_{O,max}$ for two-phase operation [4]. In the case at hand the six-switch direct three-phase topology has been selected as a basis for an evaluation of the Δ-Rectifier instead of the three-switch VIENNA Rectifier in order to have an equal number of switches employed in both systems. The six-switch conventional

rectifier topology can be thought to be derived from the VIENNA Rectifier topology by replacing the two center point diodes of the bi-directional switch in each phase by an additional switch (requiring an additional gate drive). As a more detailed analysis shows the efficiency and the power factor of the conventional rectifier is very close to the high performance of the VIENNA Rectifier.

The conventional rectifier and the Δ-Rectifier employ an equal number of switches and fast recovery free-wheeling diodes. Consequently, a direct comparative evaluation of both systems can be performed considering the current stresses on the switches, on the diodes and on the input inductors as well as the complexity of the control circuit. The fact, that the DC/DC conversion for the Δ-Rectifier does require three individual DC/DC converters in contrast to only a single one for the conventional rectifier is not considered in this study because also the DC/DC converter stage of the conventional rectifier could be split into several modules in order to decrease the power to be handled by the individual converter and/or to achieve a very compact design.

We would like to point out, that the three-level line-to-line modules of the Δ-Rectifier in **Fig.1(a)** could also be realized in a two-level structure [1] by omitting one free-wheeling diode D_F and one switch S_{ij} per line-to-line module. However, this does result in an increased voltage stress of the remaining power semiconductors and/or in a lower efficiency. Furthermore, there a significantly higher inductance of the input inductor L_Δ would be required for equal average ripple $\Delta i_{N,i}$ of the mains current resulting in a higher inductor volume. Therefore, the two-level Δ-Rectifier is not considered in this paper.

The voltage space vectors of the equivalent input phase voltages $u_{U,i}$' [1] of the three-level Δ-Rectifier are shown in **Fig.2(a)** and for the conventional rectifier in **Fig.2(b)**. Both systems show for a given input voltage range an equal value for the required output voltage level $U_O \geq \sqrt{3}\cdot\hat{U}_N$ ($\hat{U}_N$ denotes the peak value of the input phase voltage) resulting in an equal voltage stress of the switches S and the free-wheeling diodes D_F. As described in [1] the modulation limit $M_{max} = 2/\sqrt{3}$ of the Δ-Rectifier results from the fact, that the zero-sequence component u_0 of the PWM line-to-line rectifier module voltages has to show a local average value equal to zero, i.e. $u_{0,\mathrm{avg}} = 0$.

For both systems one does not have to employ a space vector modulation technique for the input current control. An average current mode controller based on the absolute value of the line-to-line currents for the Δ-Rectifier (cf. **Fig.3)** and directly on the phase currents for the conventional rectifier in combination with a triangular-shaped carrier signal and certain mains voltage pre-control signals m does allow to achieve comparable performance. There, for the Δ-Rectifier the current measurement could be done as for single-phase PFC systems on the DC side by means of a conventional shunt. Then, the inversion of the triangular-shaped carrier signal of a line-to-line module in dependency of the corresponding sign of the input line-to-line voltage as investigated in [1] for AC side current measurement can be omitted considering the three-level operation, i.e. 180° phase shift in switching frequency of the gating of the switches S_{ij+} and S_{ij-}. The control of the Δ-Rectifier has to generate six independent switching functions $s_{ij,+-}$ (ij=RS, ST, TR), while the conventional rectifier, although also utilizing six switches, does employ only three gating signals, i.e. $s_{i+} = s_{i-} = s_i$, (i=R, S, T).

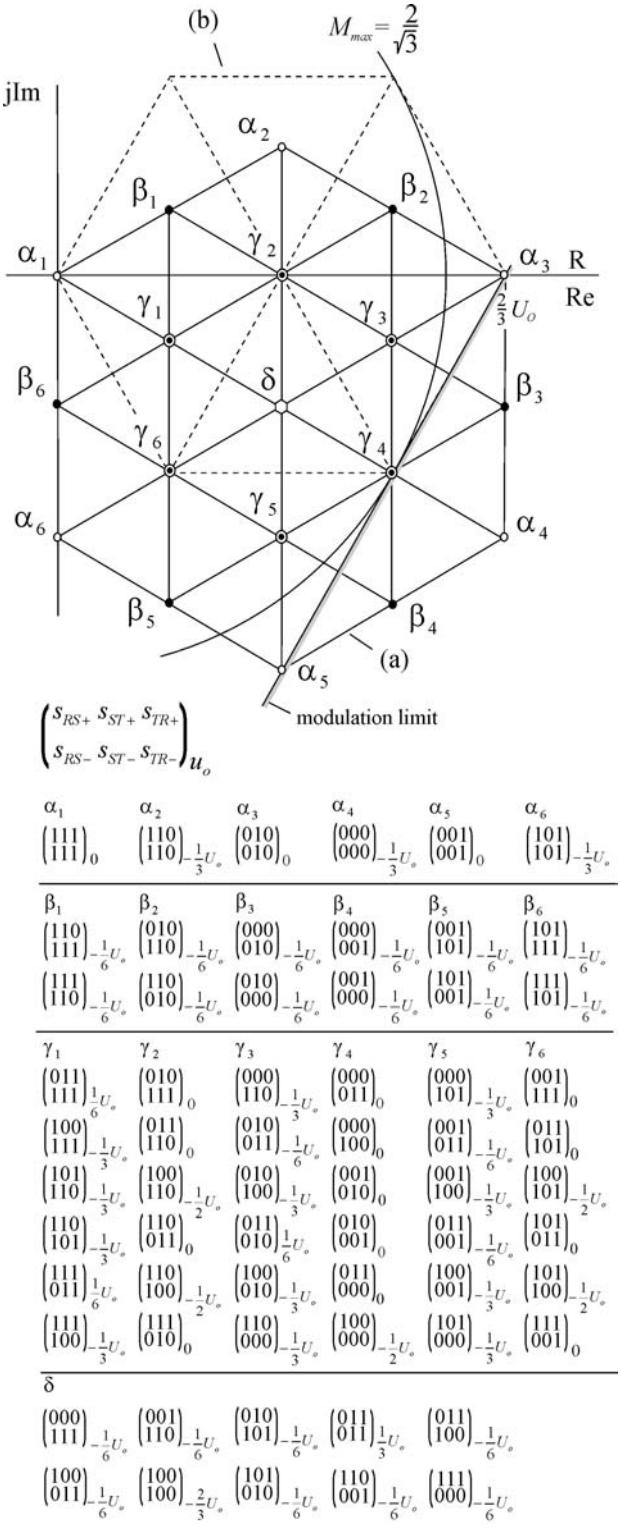

Fig.2: Voltage space vectors available for input current control; **(a)** three-level Δ-Rectifier, **(b)** conventional rectifier (cf. Fig. 4 in [1]).

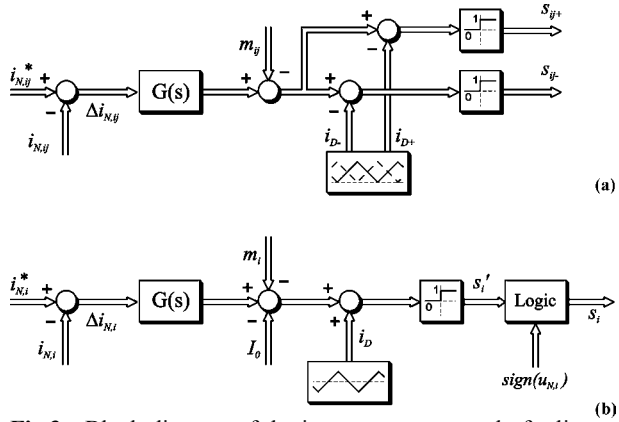

Fig.3: Block diagram of the input current control of a line-to-line module of a three-level Δ-Rectifier (cf. (**a**)) and phase current control of a conventional rectifier (cf. (**b**)).

According to **Fig.4** the Δ-Rectifier and the conventional rectifier show a largely comparable ripple of the mains phase currents due to the high number of switching states and/or space vectors available for current control in both cases.

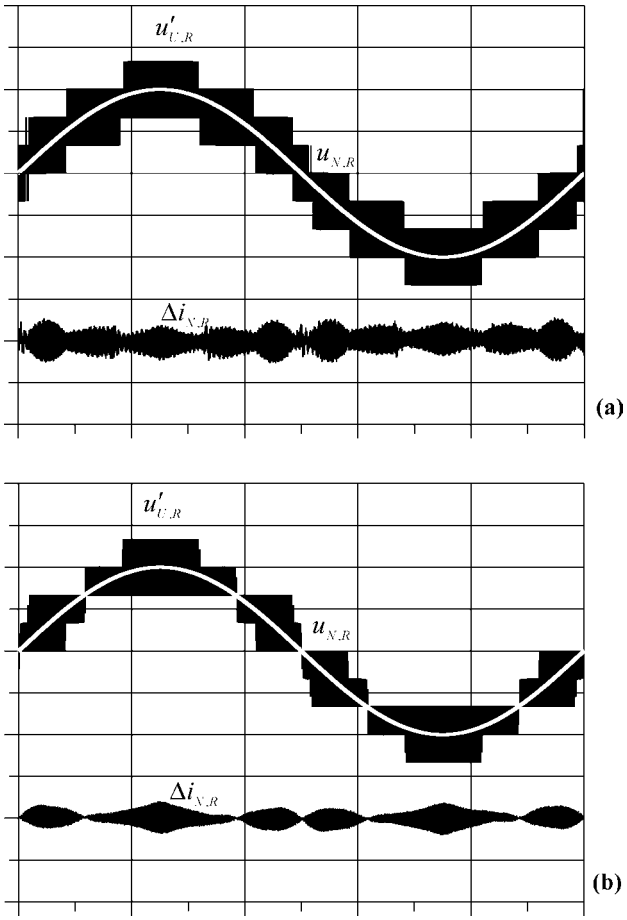

Fig.4: Time behavior of a mains phase voltage $u_{N,R}$, of the equivalent rectifier input phase voltage $u'_{N,R}$ (cf. Fig.2 in [2]) and of the current ripple $\Delta i_{N,R}$ of the mains phase current $i_{N,R}$ of the conventional rectifier (cf. **(a)**) and of the Δ-Rectifier (cf. **(b)**).

In the following in **section 2** the average and rms current stresses of the power components of the rectifier systems are calculated in analytical form. **Section 3** shows a typical dimensioning of a line-to-line module of a Δ-Rectifier for an input line-to-line voltage range of $U_{N,ij} = 320...530V$ and an output power level of $P_{O,\Delta} = 3.5kW$ required for supplying a DC/DC converter module with an estimated efficiency of $\eta_{DC/DC} \approx 95\%$. This leads to an output power of $P_O = 10kW$ for a three-phase unit. In **section 4** a control concept is proposed for the Δ-Rectifier, which does allow to handle a mains phase loss. Finally, the main advantages and drawbacks of the Δ-Rectifier as compared to the conventional rectifier are discussed in **section 5.** Furthermore, in **section 6** an outlook on the continuation of the research is given.

2 STRESSES ON THE COMPONENTS

In the following the average and the rms values of the current stresses on the power semiconductor components are calculated as required for the calculation of the conduction losses. Simple analytical approximations are derived which can be used beyond the scope of this paper for the dimensioning of the power components of a Δ-Rectifier. We assume:

- a purely sinusoidal phase current shape;
- ohmic fundamental mains behavior;
- no low frequency voltage drop across the boost inductor for the shaping of the current according to the absolute value of a line-to-line mains voltage;
- constant switching frequency;
- linear behavior of the boost inductors (inductance not dependent on the current level.

Accordingly, restricting our considerations to the positive half wave of a mains line-to-line voltage $u_{N,ij} = \sqrt{3}\hat{U}_N \sin(\varphi_N)$ we have to provide by proper modulation a local average value of the voltage across the corresponding switches S_{ij+} and S_{ij-} of $u_{U,ij,avg} \approx u_{N,ij}$.

For characterizing the modulation we define a modulation index

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_O} \approx \frac{\hat{U}_N}{\frac{1}{2}U_O} \tag{1}$$

which according to Fig.2 shows a maximum value of

$$M_{\max} = \frac{2}{\sqrt{3}}. \tag{2}$$

2.1 Inductor Current Ripple

For the calculation of the input inductor current rippel one has to decide between two modes of operation of the three-level boost converter

$$u_{N,ij}(t) < U_O/2 \quad \text{for } t < \xi \text{ or } t > \pi\text{-}\xi \tag{3}$$

$$u_{N,ij}(t) \geq U_O/2 \quad \text{for } \xi \leq t \leq \pi\text{-}\xi \tag{4}$$

where

$$\xi = \arcsin(\frac{U_o}{2\sqrt{3}\hat{U}_N}) \quad . \tag{5}$$

For $u_{N,ij}(t) < U_O/2$ ($M \in (0...\frac{1}{\sqrt{3}})$, cf. Eq.(4)) the ripple envelope is defined by

$$\Delta\hat{i}_{N,ij} = \Delta i \frac{2}{\sqrt{3}} M \sin(\omega_N t)(\frac{1}{2} - \frac{\sqrt{3}}{2} M \sin(\omega_N t)) \tag{6}$$

with

$$\Delta i = \frac{U_o T_p}{8L} = \frac{U_o T_p}{8\frac{L_\Delta}{3}} \quad . \tag{7}$$

For $u_{N,ij}(t) \geq U_O/2$ ($M \in (\frac{1}{\sqrt{3}}...\frac{2}{\sqrt{3}})$, cf. Eq.(4)) we have for the envelope

$$\Delta\hat{i}_{N,ij} = \Delta i \frac{2}{\sqrt{3}}(M \sin(\omega_N t) - \frac{1}{\sqrt{3}})(1 - \frac{\sqrt{3}}{2} M \sin(\omega_N t)) \,. \tag{8}$$

The maximum value of the envelope of the inductor ripple current within a mains half period results as

$$\Delta\hat{i}_{N,ij} = \frac{1}{12}\Delta i \,. \tag{9}$$

As a more detailed analysis shows this maximum value is reduced by a factor of 4 as compared to a two-level boost converter realization [1].

For $M \in (\frac{1}{\sqrt{3}}...\frac{2}{\sqrt{3}})$ the global rms value of the ripple current (rms value related to a mains voltage period) is

$$\Delta I^2_{N,ij,rms} = \frac{8}{9\pi}\Delta i^2[(\frac{9\pi}{64}M^4 - \frac{1}{\sqrt{3}}M^3 + \frac{13\pi}{16}M^2 + \frac{\pi}{6}) - (\frac{3M^2}{2} + \frac{1}{3})\arctan(\frac{1}{\sqrt{3M^2-1}}) - \sqrt{3M^2-1}(\frac{6M^2+1}{9} + \frac{1}{2})] \quad . \tag{10}$$

For the derivation of (10) one has to consider that the operation of the system within a mains half period is partly according to (3) and partly according to (4).

For the normalized rms value (index n) of the input inductor current ripple we define

$$\Delta I^2_{N,ij,rms,n} = \frac{1}{\Delta i}\Delta I^2_{N,ij,rms} \quad . \tag{11}$$

The global normalized rms value of the input inductor ripple current for $M \in (0...\frac{1}{\sqrt{3}})$, where the operation within a mains half period is only according to (3), can be calculated as

$$\Delta I^2_{N,ij,rms,n} = \Delta i^2(\frac{1}{18}M^2 - \frac{8}{9\sqrt{3}\pi}M^3 + \frac{1}{8}M^4) \,. \tag{12}$$

In **Fig.5** the normalized rms value of the line-to-line current and of the input phase current of a Δ-Rectifier as well as the normalized ripple of the input phase current of a conventional rectifier are depicted. Advantageously, the Δ-Rectifier shows a low rms value of the input current ripple within the whole modulation range. However, for calculating the core losses of an input inductor one has to keep in mind, that three times the inductance value L of the conventional system is employed in the Δ-Rectifier ($L_\Delta = 3L$, [1]). For a first estimation of the core losses of an input inductor an iron powder core and a modulation index $M = 1$ are assumed. According to (10) and (11) we then have for the normalized rms value of the ripple current

$$\Delta I_{N,ij,rms,n} = 0.038 \tag{14}$$

and with (7) and the specifications in [1] a rms value of

$$\Delta I_{N,ij,rms} = 0.038 \cdot 5.714 = 217\text{mA} \tag{15}$$

what results for $L_\Delta = 3L = 2.1$mH in a rms value of the flux linkage ripple

$$\Delta\Psi_{rms} = L_\Delta \cdot \Delta I_{N,ij,rms} = 456\mu\text{Vs} \,, \tag{16}$$

which is required for a core loss calculation according to [10].

The related flux density ΔB_{rms} for a number of turns of N=121Wdg and a toroidal core of type Micrometals T184-40 (A=1.88cm^2) results as

$$\Delta B_{rms} = \frac{\Delta\Psi_{rms}}{NA} = 20\text{mT} = 200\text{Gauss} \,. \tag{17}$$

According to the three-level characteristic of the line-to-line module the first harmonic of the inductor current ripple is at twice the pulse frequency f_P = 32kHz, i.e. at f_{Fe} = 64kHz. With this set of operating data we have in a first approximation for the core losses

$$P_{Fe} = 5.97 \cdot 10^{-10} \cdot f^{1.39}_{Fe[\text{Hz}]} \cdot B^{2.03}_{rms[\text{Gauss}]} \cdot V_{Fe[\text{cm}^3]} = 2.82\text{W} \tag{18}$$

which can be tolerated in case the core is arranged in a forced air-cooled environment.

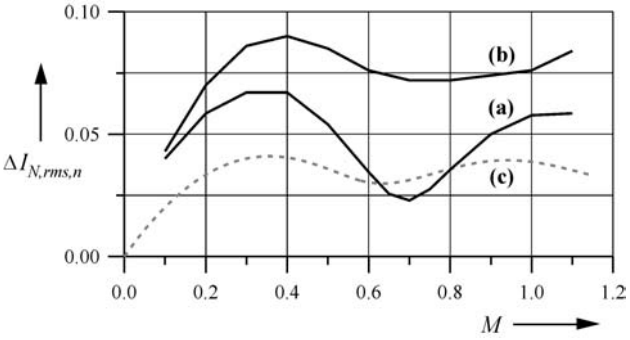

Fig.5: Normalized rms value $\Delta I_{N,rms,n}$ of the phase current of the three-level Δ-Rectifier (cf. **(a)**) and of a conventional rectifier (cf.**(b)**). Furthermore shown: rms value of the ripple $\Delta I_{N,ij,rms,n}$ of the input current of a line-to-line module of a Δ-Rectifier (cf.**(c)**) as used for the calculation of the inductor core losses.

As a more detailed analysis shows, for the conventional rectifier the inductor ripple current harmonics do occur dominantly at the pulse frequency $f_1 = f_P$ and at twice the pulse frequency $f_2 = 2f_P$ in about equal shares. It is interesting that for assuming a linear dependency on the frequency and a quadratic dependency of the core losses on the flux density this does reduce the core losses due to the fact, that for the loss calculation one has to take the squares of half of the total value $\Delta B_1 = \Delta B_2 = \Delta B/2$, i.e.:

$$P \sim f_1 \Delta B_1^2 + f_2 \Delta B_2^2 = \frac{3}{4} f_P \Delta B^2 . \quad (19)$$

As a more detailed analysis shows the core loss of a conventional rectifier employing an inductor of equal volume (L = 700µH, cf. [1]) in each phase is approximately P_{Fe} = 1.24W per inductor.

2.2 Current Stresses on the Power Components

The ripple of the inductor current is not considered for the analytical calculation of the average and rms current stresses [6] of the power components. One has to point out that a three-level and a two-level Δ-Rectifier show equal (!) current stresses on the mains side diodes, on a power transistor and on a free-wheeling diode.

2.2.1 Mains Diodes

For the average and the rms current stress on the mains diodes D_N we have

$$I_{D_N,avg} = \frac{\hat{I}_N}{\sqrt{3}\pi} \quad (20)$$

$$I_{D_N,rms} = \frac{\hat{I}_N}{2\sqrt{3}} . \quad (21)$$

2.2.2 Free-wheeling Diodes

The average and the rms current stress on the free-wheeling diodes D_F is

$$I_{D_F,avg} = \frac{\hat{U}_N}{2U_o}\hat{I}_N \quad (22)$$

$$I_{D_F,rms} = \frac{2}{\sqrt[4]{27}\sqrt{\pi}}\sqrt{\frac{\hat{U}_N}{U_o}}\hat{I}_N . \quad (23)$$

2.2.3 Power Transistors

The average and the rms current stress on the power transistors S_{ij+} and $S_{ij\_}$ is

$$I_{S_{avg}} = \frac{1}{\sqrt{3}}\left(\frac{2}{\pi} - \frac{\sqrt{3}\hat{U}_N}{2U_o}\right)\hat{I}_N \quad (24)$$

$$I_{S_{rms}} = \frac{1}{\sqrt{3}}\sqrt{\frac{1}{2} - \frac{4\hat{U}_N}{\pi\sqrt{3}U_o}}\hat{I}_N . \quad (25)$$

2.2.4 Output Capacitor

The rms current stress on the output capacitor is calculated using

$$I_{C_{out},rms}^2 = I_{D_F,rms}^2 - I_{D_F,avg}^2 \quad (26)$$

as

$$I_{C_{out},rms} = \sqrt{\left(\frac{4}{3\sqrt{3}\pi} - \frac{\hat{U}_N}{4U_o}\right)\frac{\hat{U}_N}{U_o}}\hat{I}_N . \quad (27)$$

The results of the analytical calculations are compiled in **Fig.6**.

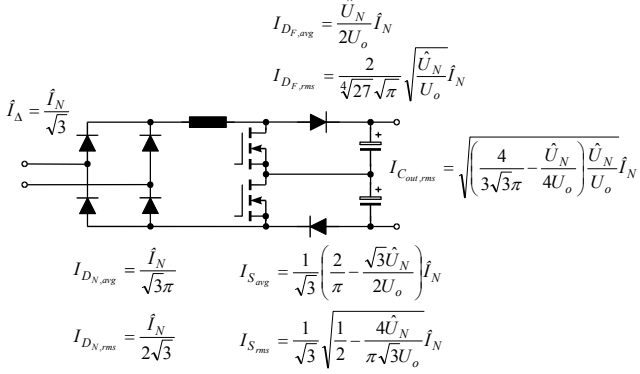

Fig.6: Circuit structure of a line-to-line module of the Δ-Rectifier and current stresses on the power components according to (20) – (27).

For the current stresses on the power components of the conventional rectifier we would like to refer to [6] for the sake of brevity.

2.3 Third Harmonic Injection

For the calculation of the average and rms current stresses on the power components an ideal sinusoidal shape of the input current of a line-to-line rectifier module has been assumed.

As proposed in [1] a reduction of the peak value of the power component currents can be achieved by a third harmonic of the line-to-line *currents* (zero sequence component), which could be imagined as a current circulating inside the delta-connection. This is of particular interest in connection with the magnetic dimensioning of the input inductor. For minimum peak value the amplitude of the third harmonic should be $^1/_6$ of the line-to-line current fundamental.

The rms and average values of the component currents with third harmonic injection show only minor differences to the values calculated for purely sinusoidal current, e.g. we have for the mains diodes D_N

$$I_{D_N,avg} = \frac{\hat{I}_N}{\sqrt{3}\pi} \quad (20)$$

$$I_{D_N,rms} = \frac{\hat{I}_N}{2\sqrt{3}} \quad \text{without 3rd harmonic} \quad (21)$$

and

$$I_{D_N,avg} = \frac{19}{18}\frac{\hat{I}_N}{\sqrt{3}\pi} \quad (28)$$

$$I_{D_N,rms} = \frac{\sqrt{37}\hat{I}_N}{12\sqrt{3}} \quad \text{with 3rd harmonic injection.} \quad (29)$$

For the conventional rectifier a zero sequence *voltage* component is employed in order to extend the modulation range M ∈ 0...1 as given for purely sinusoidal modulation to $M \in (0...2/\sqrt{3})$. Advantageously this furthermore results in a reduction of the input inductor ripple current and in a reduction of the amplitude of the third harmonic of the center point current. The optimum ratio of the third

harmonic component amplitude to the rectifier input voltage fundamental amplitude to be generated differs according to the optimization to be performed; e.g. for maximum modulation range we have a ratio of $M_3/M_1=1/6$, for a minimization of the ripple current rms value $M_3/M_1 \approx 1/4$ and for the elimination of the third harmonic of the center point current $M_3/M_1 = 7/27$. The current stress values of the conventional rectifier have been calculated based on purely sinusoidal modulation in [6]. As for the Δ- Rectifier these current values do hold with sufficient accuracy also in case a third harmonic is injected in order to extend the modulation range.

3 DIMENSIONING, EFFICIENCY

For the dimensioning of the Δ-Rectifier the following specifications are assumed:

- line-to-line input voltage range $U_{N,ij} = 320...530V_{rms}$
- output voltage U_O=800V
- total output power of the three-phase system P_O = 10kW, which results in an input power of a line-to-line module of $P_{I,\Delta}$ = 3.5kW assuming an efficiency the DC/DC converter connected in series of $\eta_{DC/DC} \approx 95\%$
- pulse frequency f_P = 32kHz.

The stresses on the components and the resulting component power losses are listed in **Tab.1**.

The calculations are based on the analytical expressions derived in section 2 and on experimental switching loss data according to [7] and [8]. The efficiency is for an input line-to-line voltage of, e.g. $U_{N,ij} = 480V$ in the range of $\eta = 97.4\%$ for hard switching.

In case a soft turn-on technique according to [9] is employed which does not cause an increase of the transient turn-off overvoltage the efficiency could be improved to $\eta_S = 97.7\%$.

The stresses on the power components of a conventional rectifier of equal specifications (output power P_O = 10.5kW) were calculated based on [6] and are listed in **Tab.2**.

As a comparison of **Tabs. 1** and **2** shows, the efficiency of the Δ-Rectifier is lower by ≈ 0.3 ... 0.4% as compared to the conventional rectifier. This is due to the higher current stress on the output electrolytic capacitors and/or due to the higher resulting capacitor losses. The differences of the losses of the semiconductor components are not significant because the peak current stress of the Δ-Rectifier is reduced by a factor of √3 as compared to the conventional rectifier but the stress is applied within the whole mains period in contrast to the conventional rectifier where the peak current stress is higher but applied only for half a mains period.

Input power	$P_{I,\Delta}$=	3500	3500	3500	3500	W
Input voltage	$U_{N,l\text{-}l}$=	320	400	480	530	V
Input current (line-to-line)	$I_{N,ij,rms}$=	10.94	8.75	7.29	6.60	A
Output voltage	U_O=	800	800	800	800	V
Switch current	$I_{S,rms}$=	7.89	5.53	3.86	2.99	A
$R_{DS,on}$ = 0.12Ω @125°C	$I_{S,avg}$=	5.47	3.50	2.19	1.57	A
Conduction loss	$P_{S,C}$=	7.46	3.67	1.78	1.07	W
Turn-on (k_{on} =28.5µJ/A)	$P_{S,on}$=	12.74	10.19	8.49	8.49	W
Turn-off (k_{off}=8.2µJ/A)	$P_{S,off}$=	2.58	2.07	1.72	1.56	W
2x Switch total losses	P_S=	38.1	25.8	19.0	16.1	W
Free-wheeling diode current	$I_{DF,rms}$=	7.58	6.78	6.19	5.89	A
U_{DF0}=0.95V, R_{DF}=24mΩ	$I_{DF,avg}$=	4.38	4.38	4.38	4.38	A
2x Free-wheeling diode losses	P_{DF}=	11.1	10.5	10.2	10.0	W
Mains diode current	$I_{DN,rms}$=	7.73	6.19	5.16	4.67	A
U_{DN0}=0.85V, R_{DN}=10mΩ	$I_{DN,avg}$=	4.92	3.94	3.28	2.97	A
4x Mains diode losses	P_{DN}=	19.1	14.9	12.2	11.0	W
Total power semiconductor losses		68.3	51.3	41.4	37.1	W
Input choke (R_L=152mΩ, P_{FE} =5W)	P_L=	23.2	16.7	13.1	11.6	W
Output capacitor current	$I_{CO,rms}$=	6.19	5.18	4.38	3.94	A
4x Output capacitor 470µF/400V (R_{ESR}=0.3Ω)	P_{CO}=	23.0	16.1	11.5	9.3	W
Auxiliary power (housekeeping, fans)	P_{aux}=	10.0	10.0	10.0	10.0	W
Snubbers, PCB, var. distributed losses	P_{add}=	16.7	16.7	16.7	16.7	W
Total power losses	P=	141.1	110.7	92.6	84.7	W
Efficiency	η=	96.0	96.8	97.4	97.6	%
Efficiency with turn-on snubber	η_s=	96.5	97.2	97.7	97.9	%

Tab.1: Losses of a 3.5kW/32kHz line-to-line module of a Δ-Rectifier. The improvement of the overall efficiency in case a turn-on snubber is employed is in the range of 0.3 … 0.5%.

Input power	P_I=	10500	10500	10500	10500	W
Input voltage	$U_{N,l\text{-}l}$=	320	400	480	530	V
Input current	$I_{N,i,rms}$=	18.94	15.16	12.63	11.44	A
Output voltage	U_O=	800	800	800	800	V
Switch current	$I_{S,rms}$=	8.94	5.94	3.66	2.31	A
$R_{DS,on}$ = 0.12Ω @125°C	$I_{S,avg}$=	4.15	2.45	1.31	0.77	A
Conduction loss	$P_{S,C}$=	9.59	4.23	1.61	0.64	W
Turn-on (k_{on} =28.5µJ/A)	$P_{S,on}$=	7.78	6.22	5.18	4.70	W
Turn-off (k_{off}=8.2µJ/A)	$P_{S,off}$=	2.24	1.79	1.49	1.35	W
6x Switch total losses	P_S=	117.7	73.5	49.7	40.1	W
Free-wheeling diode current	$I_{DF,rms}$=	9.97	8.92	8.14	7.75	A
U_{DF0}=0.95V, R_{DF}=24mΩ	$I_{DF,avg}$=	4.38	4.38	4.38	4.38	A
6x Free-wheeling diode losses	P_{DF}=	39.3	36.4	34.5	33.6	W
Mains diode current	$I_{DN,rms}$=	13.40	10.72	8.93	8.09	A
U_{DN0}=0.85V, R_{DN}=10mΩ	$I_{DN,avg}$=	8.53	6.82	5.69	5.15	A
6x Mains diode losses	P_{DN}=	54.3	41.7	33.8	30.18	W
Total power semiconductor losses		211.2	151.5	118.0	103.9	W
Input choke (R_L = 51mΩ, P_{FE} = 5W, worst case)	P_L=	69.7	50.0	39.3	34.9	W
Output capacitor current	$I_{CO,rms}$=	12.3	9.3	6.6	4.8	A
12x Output capacitor 470µF/400V (R_{ESR}=0.1Ω)	P_{CO}=	15.1	8.6	4.3	2.3	W
Auxiliary power (housekeeping, fans)	P_{aux}=	30	30	30	30	W
Snubbers, PCB, var. distributed losses	P_{add}=	50	50	50	50	W
Total power losses	P=	375.9	290.2	241.6	221.1	W
Efficiency	η=	96.4	97.2	97.7	97.9	%
Efficiency with turn-on snubber	η_s=	96.9	97.6	98.0	98.2	%

Tab.2: Losses of a 10.5kW/32kHz three-phase conventional rectifier. The improvement of the overall efficiency in case a turn-on snubber is employed is in the range of 0.3 … 0.5% (as for the Δ-Rectifier, cf. Tab.1).

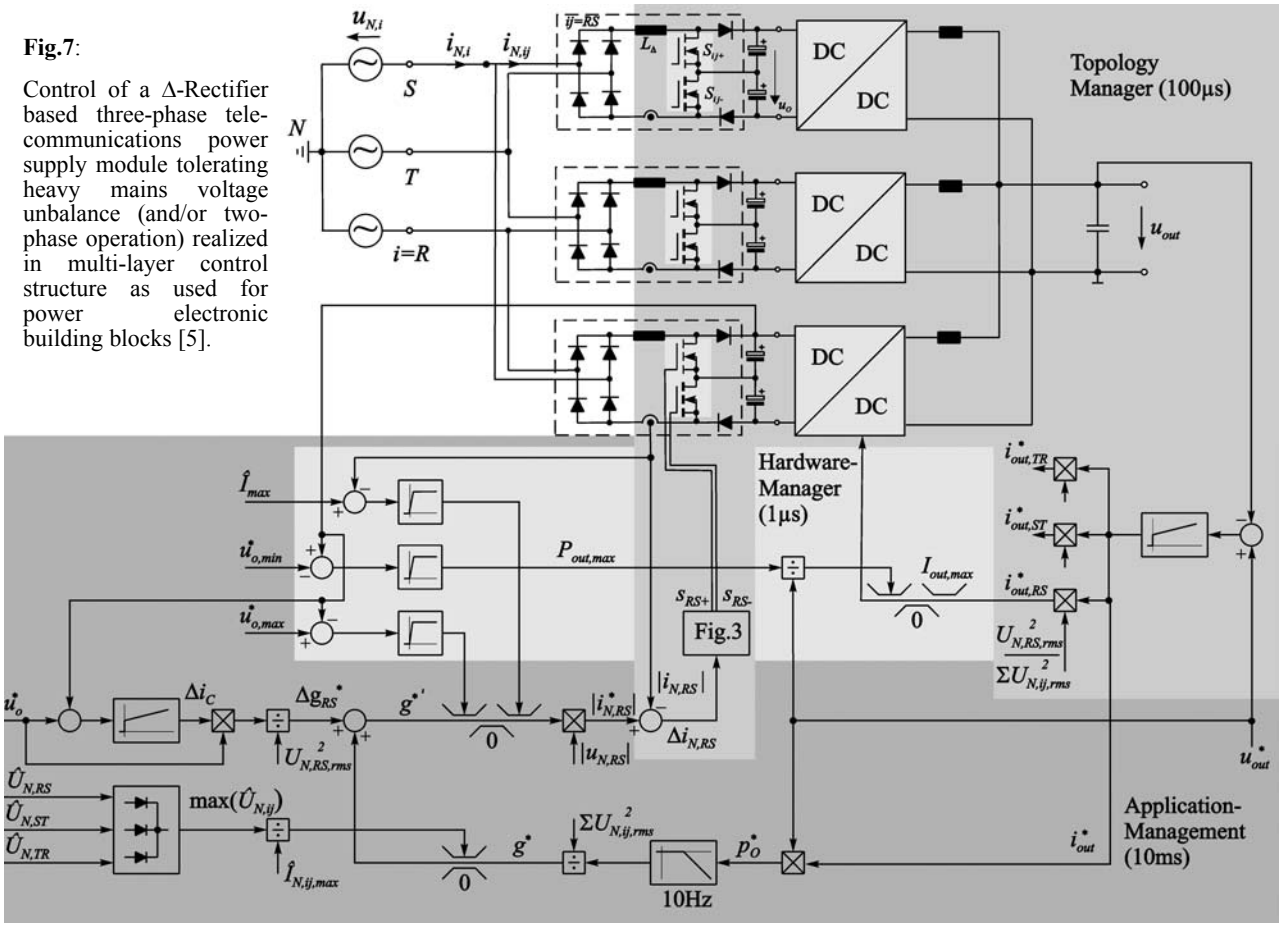

Fig.7:

Control of a Δ-Rectifier based three-phase telecommunications power supply module tolerating heavy mains voltage unbalance (and/or two-phase operation) realized in multi-layer control structure as used for power electronic building blocks [5].

In **Table 3** the semiconductor components employed for the calculation of the efficiency are compiled.

Part	Type
S	Infineon SPW47N60C2
D_F	Int. Rect. HFA25PB60
D_N	ST TYN1040 (Thyristor)

Tab.3: List of power semiconductor components which have been selected as basis for the calculation of the efficiency of the Δ-Rectifier (cf. Tab.1) and of the conventional rectifier (cf. Tab.2).

4 System Control

Figure 7 shows the structure of the control of a three-phase Δ-Rectifier-based telecommunications power supply module, which is able to handle heavily unbalanced mains voltage conditions. The cascaded system control is organized in a multi-layer structure as employed in power electronic building blocks (PEBB) [5]. Corresponding to the dominant time constants there are four layers:

- Hardware manager: transistor gate-drive, current sensors, fast protection (<1µs);
- Topology manager: current control, hardware interfaces, communication backbone, synchronization and power management of the line-to-line modules (<100µs);
- Application manager: mains frequency current shaping, conventional protection, output voltage control (<10ms);
- System manager: communication to central supervising unit, power management.

The switching functions s_{ij+} and s_{ij-} of each line-to-line module are generated by an inner current control (cf. Fig.3). This inner control loop requires a current reference value $i_{N,ij}$*, ij = *RS, ST, TR*, which is generated by multiplying a reference conductance g*' with the actual absolute value of the line-to-line voltages $|u_{N,ij}|$. The conductance g*' is defined by the DC/DC converter output voltage control and by the module output voltage controller Δg_{ij}^* (both realized as PI-type controllers), i.e. $g^{*\prime} = g^* + \Delta g_{ij}$. Highly dynamic limiting of g*' is provided in order not to exceed the maximum allowable peak current stress $\hat{I}_{max}$ of the power semiconductor components and/or a maximum level $u_{o,max}$ (as defined by the voltage rating of the electrolytic capacitors and by blocking capability of the power semiconductors) of the rectifier module output voltage in case of, e.g. a load dump or in case of the return of a missing mains phase. The reference conductance g^* is derived with low bandwidth ($f_g \approx$ 10Hz) from the DC/DC converter output voltage controller $p^*_o = i_{out}^* u_{out}^*$, consequently a division by the sum of squares of the input line-to-line voltage rms value has to be performed for calculating a mains-side reference input conductance for all line-to-line rectifier modules which does fulfill the output power requirement.

The limitation of g^* is with reference to the peak values of the three line-to-line mains voltages in order not to exceed $\hat{I}_{max}$ in the stationary case.

We would like to point out that the above-mentioned requirements are given not only for the Δ-Rectifier but for any two-stage three-phase and/or single-phase rectifier system. For the conventional rectifier the different functions need to be implemented only once [4], for the Δ-Rectifier some functions have to be implemented for each line-to-line module.

A special issue of the realization of a three-phase unit by three line-to-line modules is the division of the output voltage controller output (total output current reference value) into reference values of the output currents $i_{out,ij}^*$ of the DC/DC converter connected to the line-to-line modules. The calculation of $i_{out,ij}^*$ is performed by multipliers considering the squares of the normalized input line-to-line voltages. The multipliers are shown in **Fig.7** on the left-hand-side of the output voltage controller. The output current reference values $i_{out,ij}^*$ are limited according to the maximum admissible output current $I_{out,max}$ of the DC/DC converters as defined by the system design and are decreased in case the rectifier module output voltage (DC link voltage) goes under a certain minimum level $u_{o,min}^*$.

5 DISCUSSION

As the analysis in the previous sections shows the Δ-Rectifier is characterized by a voltage and current stress on the power transistors and free-wheeling diodes and/or a realization effort of the power circuit which is very much comparable to the conventional direct three-phase approach. Also, concerning the complexity of the control both systems does not show large differences. The main difference is the additional effort for the two-phase input bridge rectifier of each line-to-line module which has to be compared to two input diodes as required for each phase of the conventional rectifier and the current stress on the DC link capacitors. In case of a symmetrical mains the conventional rectifier shows a significantly lower current stress on the output capacitors due to the constant power flow of the three-phase system. This, however is only a minor advantage in case a high hold-up time is required where a large capacitance of the output capacitors has to be installed. Further research will show the possibility of reducing the losses of the DC link capacitors by connecting foil-type capacitors in parallel for the handling of the switching frequency components of the capacitor current.

The second weakness of the Δ-Rectifier is the high effort for the realization of a DC/DC converter output stage. However, for high-power telecom power supply modules with an output power in the range of $P_O \approx 10$kW this is not of much relevance because the DC/DC converters could be realized by six individual modules with 400V input voltage, where always a single DC/DC converter module is connected to a partial output voltage of a line-to-line rectifier module and all DC/DC converter module outputs are connected in parallel. There, each DC/DC converter module has to be designed for a convenient power level of ≈1.5 … 2kW, which does allow to avoid bulky heatsinks and/or transformers and/or does facilitate a very compact design. The control of the individual modules could easily be integrated into the multi-layer control structure of the Δ-Rectifier.

As a main advantage of the Δ-Rectifier, one has to point out that the modification of the two-phase input rectifier bridge to a three-phase thyristor bridge does allow to supply the full output power also in the case of a mains phase loss by switching over to the two remaining mains phases. There, however, one should take care that the resulting high current stress on the remaining phases does not cause problems. Furthermore, the thyristors could be employed for short-circuiting the pre-charge resistors after output capacitor pre-charging at system start-up.

A further advantage of the Δ-Rectifier is the possibility of using a low-cost shunt for the input current measurement. This concept is well known from single-phase PFC.

6 CONCLUSIONS

As this paper shows the Δ-Rectifier is an interesting alternative to a direct three-phase three-level unity power factor rectifier system. Accordingly the Δ-Rectifier concept will be further investigated at the ETH Zurich in collaboration with m-pec where the main topics will be:

- practical realization of a Δ-Rectifier system including a DC/DC conversion connected in series and the system control;
- investigation of the influence of a mains voltage unbalance, of a non-linearity of the boost inductor iron cores, and of the discontinuous inductor current mode occurring at light load concerning the formation of a zero sequence component of the ripple currents of the line-to-line input currents and/or the partial mutual compensation of the ripple components of the line-to-line currents in the mains phase currents;
- single-stage realization of the line-to-line modules, e.g. in the form of a SEPIC converter (cf. **Fig.8,** [11]). The increase of the voltage and current stresses as compared to the boost-type modules could be of minor concern in low power and/or low voltage applications where a true three phase system is provided as, e.g. for the powering of the in-flight entertainment systems in future airplanes where 100W could be a typical power demand per passenger seat in the business-class.

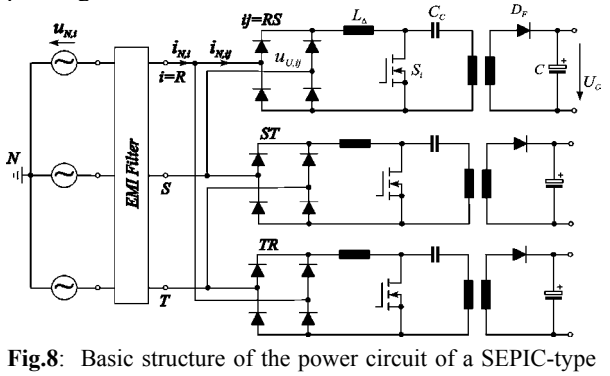

Fig.8: Basic structure of the power circuit of a SEPIC-type Δ-Rectifier [11].

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