Wide Input Voltage Range High Power Density High Efficiency 10kW Three-Phase Three-Level Unity Power Factor PWM Rectifier

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Abstract – **In this paper the current stresses on the power components of a direct three-phase boost-type unity power factor rectifier are analysed in order to provide a basis for a system design under restriction of the height to 2-U. The conduction losses of the power semiconductors are calculated using analytical approximations of the average and rms values of the component currents. The switching losses are taken from experimental investigations where a novel turn-on snubber has been employed. Based on this data an overview of the estimated power losses is given for a rectifier system of 10.5kW/800VDC output for 320V/400V/480V/530V (rms, line-to-line) mains voltage. Corresponding efficiency figures are calculated and the improvement achieved by the turn-on snubber as compared to hard switching is determined. The snubber topology and operating principle is discussed in detail. Finally, the theoretical results are verified by experimental investigation of a system prototype.**

1 INTRODUCTION

Modern high-power telecom power supply modules are typically designed for a rated output power of $P_{O,max}$ = 50V · 200A = 10kW and show a two-stage topology, where a three-phase high power factor rectifier is supplying an output-side DC/DC converter.

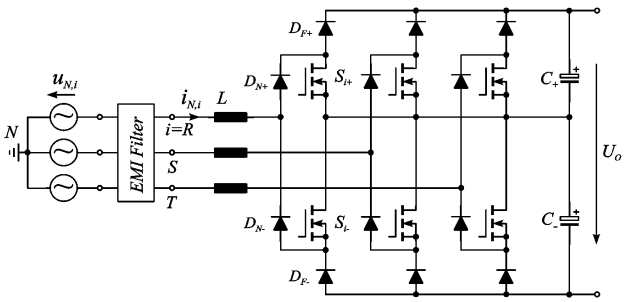

Fig.1: Basic structure of the power circuit of the three-phase six-switch three-level boost-type unity power factor rectifier.

The six-switch rectifier system shown in **Fig.1** [1] can be considered as a first step in the development of the well known VIENNA Rectifier [2] where two individual switches and series connected diodes per phase are replaced by a four-quadrant switch formed by a diode bridge and a turn-off power semiconductor. Employing two switches per phase does result in increased gate drive effort and reduced switch utilization but, as a more detailed analysis shows, the efficiency and the power factor of the system depicted in Fig.1 are very close to the high performance of the VIENNA Rectifier.

The space vectors of the input phase voltages $u_{U,i}$, i=*R,S,T,* [3] of the three-level rectifier are shown in **Fig.2**. The system shows for a given input voltage a required output voltage level of $U_O \geq \sqrt{3}\cdot\hat{U}_N$ ($\hat{U}_N$ denotes the peak value of the input phase voltage) which corresponds to the modulation limit $M_{max} = 2/\sqrt{3}$ (cf. (2)). However, one does not have to employ a space vector modulation technique for the input current control. An average current mode control based on a triangular-shaped carrier signal and incorporating a mains voltage pre-control or, according to [4], a multiplier-free approach (cf. **Fig.3**) does allow to achieve comparable performance. The rectifier, although utilizing six switches, does employ only three gating signals, i.e. $s_{i+} = s_{i-} = s_i$, (i = R, S, T).

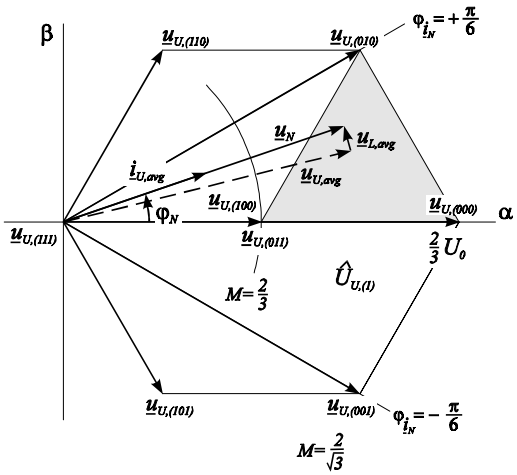

Fig.2: Rectifier input voltage space vectors available for input current control (cf. Fig. 2 in [3]).

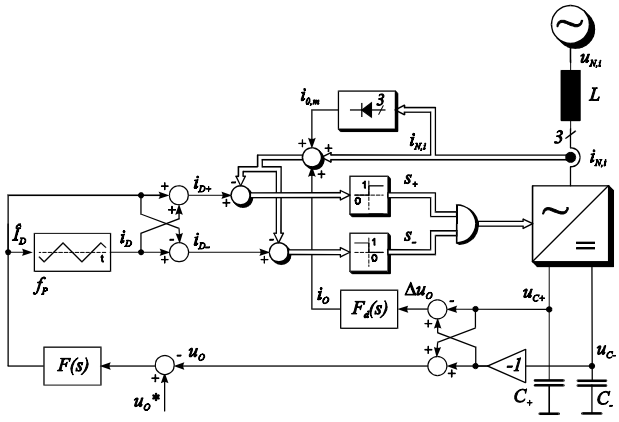

Fig.3: Block diagram of the output voltage and multiplier-free input current control (cf. Fig.I.6 in [4]).

According to [5] the rectifier shows a nearly constant peak-to-peak value of the ripple of the input phase currents over a mains fundamental period due to the high number of switching states and/or input voltage space vectors available for current control.

In the following in **section 2** the average and rms current stresses on the power components of the rectifier system are calculated in analytical form. The analysis of the switching behavior with hard switching is done in **section 3**. **Section 4** shows the dimensioning of the rectifier system for an input line-to-line voltage range of $U_{N,ij}$ = 320…530Vrms and an output power level of P_O = 10.5kW as required for supplying a 10kW output DC/DC converter module with an estimated efficiency of $\eta_{DC/DC} \approx 95\%$. The mode of operation and performance of the proposed turn-on snubber [6] is analysed in detail in **section 5** together with the experimental system and measurement results (power factor, THD, efficiency).

2 STRESSES ON THE COMPONENTS

In the following the average and the rms values of the current stresses on the power semiconductor components as required for the calculation of the conduction losses are determined. Simple analytical approximations are derived which can be used beyond the scope of this paper for the dimensioning of the power components of the rectifier.

We assume:

- a purely sinusoidal phase current shape;
- ohmic fundamental mains behavior;
- no (neglectable) mains frequency voltage drop across the boost inductors required for the sinusoidal shaping of the input current;
- constant switching frequency;
- linear behavior of the boost inductors (inductance not dependent on the input current level.

For characterizing the modulation we define a modulation index

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_O} \approx \frac{\hat{U}_N}{\frac{1}{2}U_O} \tag{1}$$

which according to Fig.2 shows a maximum value of

$$M_{\max} = \frac{2}{\sqrt{3}}. \tag{2}$$

For a first estimation of the losses in the iron power core of an input inductor a modulation index M = 1 is assumed. According to [5] we then have for the normalized rms value of the ripple current

$$\Delta I_{N,rms,n} = \frac{\Delta I_{N,rms}}{\Delta i} = 0.075\,. \tag{3}$$

For a pulse frequency of $f_P = 1/T_P$ = 38kHz, an inductance value of L = 225µH, and an output voltage of U_O = 800V this results in

$$\Delta i = \frac{U_o T_p}{8L} = 11.7 \tag{4}$$

and/or in an rms value of current ripple of

$$\Delta I_{N,rms} = 0.075 \cdot 11.7 = 877\text{mA}\,. \tag{5}$$

This is related to a rms value

$$\Delta\Psi_{rms} = L \cdot \Delta I_{N,rms} = 197\mu\text{Vs} \tag{6}$$

of the ripple of the flux linkage which is required for a core loss calculation according to [7].

The input inductor is realized employing a helical winding ([8], Schott corporation [9], type number: 33299). The related flux density ΔB_{rms} for a number of turns of N = 48 and an E-type core (A=2.28cm^2) results as

$$\Delta B_{rms} = \frac{\Delta\Psi_{rms}}{NA} = 18.0\text{mT} = 180\text{Gauss}\,. \tag{7}$$

As a more detailed analysis shows, for the conventional rectifier the inductor ripple current harmonics do occur dominantly at the pulse frequency $f_1 = f_P$ and at twice the pulse frequency $f_2 = 2f_P$ in about equal shares [5]. It is interesting that for assuming a linear dependency on the frequency and a quadratic dependency of the core losses on the flux density this does reduce the core losses due to the fact, that for the loss calculation one has to take the squares of half of the total value $\Delta B_1 = \Delta B_2 = \Delta B/2$, i.e.:

$$P \sim f_1 \Delta B_1^2 + f_2 \Delta B_2^2 = \frac{3}{4} f_P \Delta B^2 \tag{8}$$

with $f_{Fe} = f_P$ = 38kHz, V_{Fe} = 27.5cm^3 and (7) the iron power loss of one input choke results in approximately

$$P_{Fe} \sim \frac{3}{4} \cdot 9.07 \cdot 10^{-10} \cdot f_{Fe[\text{Hz}]}^{1.26} \cdot B_{rms[\text{Gauss}]}^{2.11} \cdot V_{Fe[\text{cm}^3]} = 633\text{mW} \tag{9}$$

which can easily be tolerated even if the core is not arranged in a forced air-cooled environment.

2.1 Current Stresses on the Power Components

The ripple of the inductor current is not considered for the analytical calculation of the average and rms current stresses [10] of the power components. The results of the analytical calculations according to [11] are compiled in **Fig.4**.

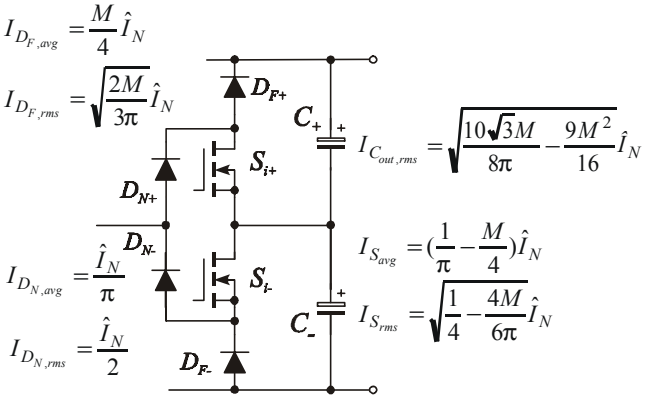

Fig.4: Circuit structure of a bridge leg of the rectifier and current stresses on the power components according to [11].

2.2 Third Harmonic Injection

A zero sequence voltage component, i.e. a third harmonic at the pulse-width modulator input of each phase is employed in order to extend the modulation range $M \in 0...1$ given for purely sinusoidal modulation, to $M_1 \in (0...2/\sqrt{3})$.

Advantageously, this furthermore results in a reduction of the ripple of the input inductor current and in a reduction of the amplitude of the third harmonic of the center point current. The optimum ratio of the amplitude of the third harmonic component to the amplitude of the pulse-width modulator input generating the rectifier input voltage fundamental differs according to the optimization to be performed; e.g. for achieving a maximum modulation range we have a ratio of $M_3/M_1 = {}^1/_6$, for a minimization of the input current ripple rms value $M_3 / M_1 \approx {}^1/_4$ and for the elimination of the third harmonic of the center point current $M_3 / M_1 = {}^7/_{27}$. The current stress values of the rectifier have been calculated based on purely sinusoidal modulation. However, as a more detailed analysis shows the results do hold with sufficient accuracy also in case a third harmonic is injected for extending the modulation range.

3 Analysis of the Switching Behavior

The analysis of the turn-on and turn-off behavior has been done for the final layout of the power circuit PCB of the actual converter prototype without turn-on snubber. There,

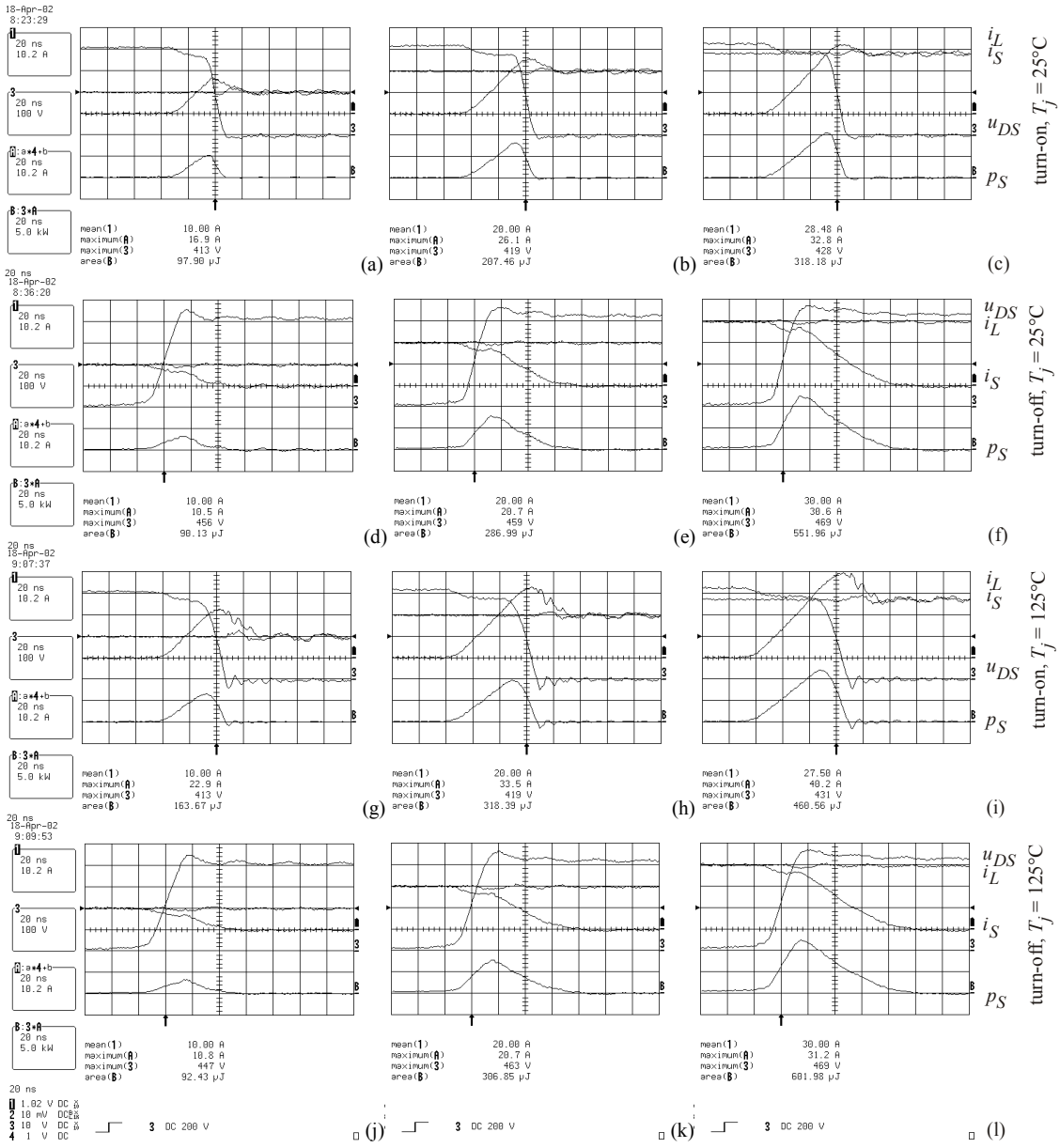

Fig.5: Experimental analysis of the switching behavior of the power MOSFET SPW47N60C2 (Infineon) in combination with a free-wheeling diode ISL9K3060G3 (Stealth, Fairchild) in the three-phase three-level PWM rectifier topoloy. **(a)-(f)**: T_j = 25°C; **(g)-(l)** T_j = 125°C; **(a)**, **(b)**, **(c)** and **(g)**, **(h)**, **(i)**: turn-on of the power transistor *S*; **(d)**, **(e)**, **(f)** and **(j)**, **(k)**, **(l)**: turn-off of the power transistor *S*. **(a)**, **(d)**, **(g)**, **(j)**: power transistor current being switched i_S = 10A, **(b)**, **(e)**, **(h)**, **(k)**: i_S = 20A, **(c)**, **(f)**, **(i)**, **(l)**: i_S = 30A. 1: Inductor current i_L (10.2A/div), 3: Drain-source voltage of the power transistor u_{DS} (100V/div), A: Source current of the power transistor i_S (10.2A/div), B: switching power loss p_S (5kW/div).

due to the extremely fast switching speed the measurement of the transistor current and voltage has to be with high bandwidth, i.e. by a coaxial shunt and a passive voltage probe [12].

The results of the experimental investigation of the turn-on and turn-off behavior are depicted in **Fig.5(a)-(l)** for transistor currents of i_S = 10, 20 and 30A, junction temperatures of T_j = 25°C and T_j = 125°C and a gate resistor of R_G = 18Ω. Based on these measurements the relation between transistor switching current and switching energy loss is calculated in the form of trendlines assuming a linear dependency of the energy loss on the switching current. The linear approximations are characterized by coefficients

$$k_{0,on} = -38.8\mu\text{J}\ ,\ k_{1,on} = 19.1\mu\text{J/A} \qquad (10), (11)$$

$$k_{0,off} = -175.8\mu\text{J}\ ,\ k_{1,off} = 25.5\mu\text{J/A} \qquad (12), (13)$$

(cf. **Fig.6**). A reduction of the gate resistance value from R_G = 18Ω to R_G = 9Ω would result in

$$k_{0,on} = -2.81\mu\text{J}\ ,\ k_{1,on} = 9.49\mu\text{J/A} \qquad (14), (15)$$

$$k_{0,off} = -127.5\mu\text{J}\ ,\ k_{1,off} = 18.0\mu\text{J/A} \qquad (16), (17)$$

but does increase the power transistor switching overvoltage at turn-off from 469V to 488V (the blocking capability of the power transistors is 600V). Therefore, R_G = 18Ω has been selected for all analysis and experiments throughout the paper.

The switching losses per power transistor now can be approximated by

$$P_S = f_P \left[\left(k_{1,on} + k_{1,off} \right) \cdot I_{S,avg} + k_{0,on} + k_{0,off} \right]. \qquad (18)$$

According to [6] the turn-on losses of the power MOSFETs can be reduced by approx. 85% for employing a turn-on snubber which does not increase the turn-off voltage. Therefore, for calculating the efficiency of the converter system with turn-on snubber the turn-on loss is assumed to be zero, i.e. $P_{S,on}$ = 0, in a first rough approximation.

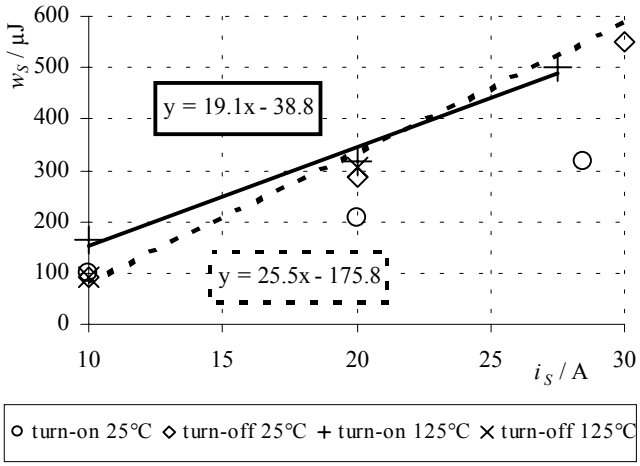

Fig.6: Measured values of the transistor turn-on and turn-off energy losses w_S dependent on the switching current i_S and the junction temperature T_j. Furthermore shown: linear trend lines and corresponding formulas ($y = w_s$ [µJ], $x = i_s$ [A]) for the measurements at T_j = 125°C.

4 DIMENSIONING, EFFICIENCY

The dimensioning of the rectifier system is according to the following specifications:

- line-to-line input voltage range $U_{N,ij}$ = 320 … 530V_{rms}
- output voltage U_O = 800V
- output power of the DC/DC converter supplied by the rectifier stage $P_{O,DC/DC}$ = 10kW, which results in an input power of the rectifier of P_I = 10.85kW assuming an efficiency the DC/DC converter of $\eta_{DC/DC} \approx$ 95% and a rectifier efficiency of $\eta_R \approx$ 97%.
- pulse frequency f_P = 38kHz.
- optional turn on snubber.

Input power	P_I =	10850	10850	10850	10850	W
Input voltage	$U_{N,l\text{-}l}$ =	320	400	480	530	V
Input current	$I_{N,rms}$ =	19.58	15.66	13.05	11.82	A
Output voltage	U_O =	800	800	800	800	V
Modulation index	M =	0.65	0.82	0.98	1.08	
Switch current	$I_{S,rms}$ =	9.24	6.14	3.79	2.39	A
$R_{DS,on}$ = 0.12Ω @125°C	$I_{S,avg}$ =	4.29	2.53	1.35	0.80	A
Conduction loss	$P_{S,C}$ =	10.24	4.52	1.72	0.68	W
Turn-on loss	$P_{S,on}$ =	5.60	4.33	3.49	3.09	W
Turn-off loss	$P_{S,off}$ =	5.12	3.44	2.32	1.79	W
6x Switch total losses	P_S =	128.8	73.7	45.2	33.4	W
Free-wheeling diode current	$I_{DF,rms}$ =	10.31	9.22	8.42	8.01	A
U_{DF0}=0.81V, r_{DF}=33mΩ	$I_{DF,avg}$ =	4.52	4.52	4.52	4.52	A
6x Free-wheeling diode losses	P_{DF} =	43.0	38.8	36.0	34.7	W
Mains diode current	$I_{DN,rms}$ =	13.84	11.07	9.23	8.36	A
U_{DN0}=0.85V, r_{DN}=10mΩ	$I_{DN,avg}$ =	8.81	7.05	5.87	5.32	A
6x Mains diode losses	P_{DN} =	56.4	43.3	35.1	31.3	W
Total power semiconductor losses		225.2	155.8	116.2	99.4	W
Input choke (R_L = 19.5mΩ, P_{FE} = 0.633W)	P_L =	24.3	16.3	11.9	10.1	W
Output capacitor current	$I_{CO,rms}$ =	12.7	9.6	6.8	4.9	A
12x Output capacitor 330µF/450V (R_{ESR}=0.1Ω)	P_{CO} =	16.1	9.2	4.6	2.4	W
Auxiliary power (housekeeping, fans)	P_{aux} =	30	30	30	30	W
Snubbers, PCB, var. distributed losses	P_{add} =	50	50	50	50	W
Total power losses	P =	345.7	261.3	212.7	191.9	W
Efficiency	η =	96.81	97.59	98.04	98.23	%
Eff. with turn-on snubber ($P_{S,on}$ = 0)	η_s =	97.12	97.83	98.23	98.40	%

Tab.1: Losses of a 10.85kW/50kHz three-phase rectifier according to Fig.1. The improvement of the overall efficiency in case a turn-on snubber would be employed would be in the range of 0.17 … 0.31%.

Part	Type
S	Infineon SPW47N60C2 (CoolMOS)
D_F	Fairchild ISL9L3060G3 (Stealth)
D_N	ST TYN640 (Thyristor)

Tab.2: Power semiconductor components which have been selected as basis for the calculation of the efficiency of the rectifier system (cf. Tab.1). The devices D_N in Fig.1 are replaced by thyristors in the actual circuit and are used besides rectification for bridging of the output capacitor precharge resistors after start-up in order to avoid mechanical contacts, i.e. a relay.

The stresses on the power components and the resulting power losses are listed in **Tab.1**. The characteristic figures

compiled in Tab.1 are based on the analytical expressions derived in section 2 and on the experimental switching loss data defined by (10)-(13). For an input line-to-line voltage of, e.g. $U_{N,ij} = 400V_{rms}$ there a remarkably high efficiency of $\eta \approx 97.6\%$ is achieved for hard switching. In case a soft turn-on technique [13] would be employed (which in principle would not cause an increase of the transient turn-off overvoltage, [6]) the efficiency could be improved to $\eta_S \approx 97.8\%$.

In **Tab.2** the power semiconductor components employed in the power circuit and considered in the calculation of the efficiency are compiled.

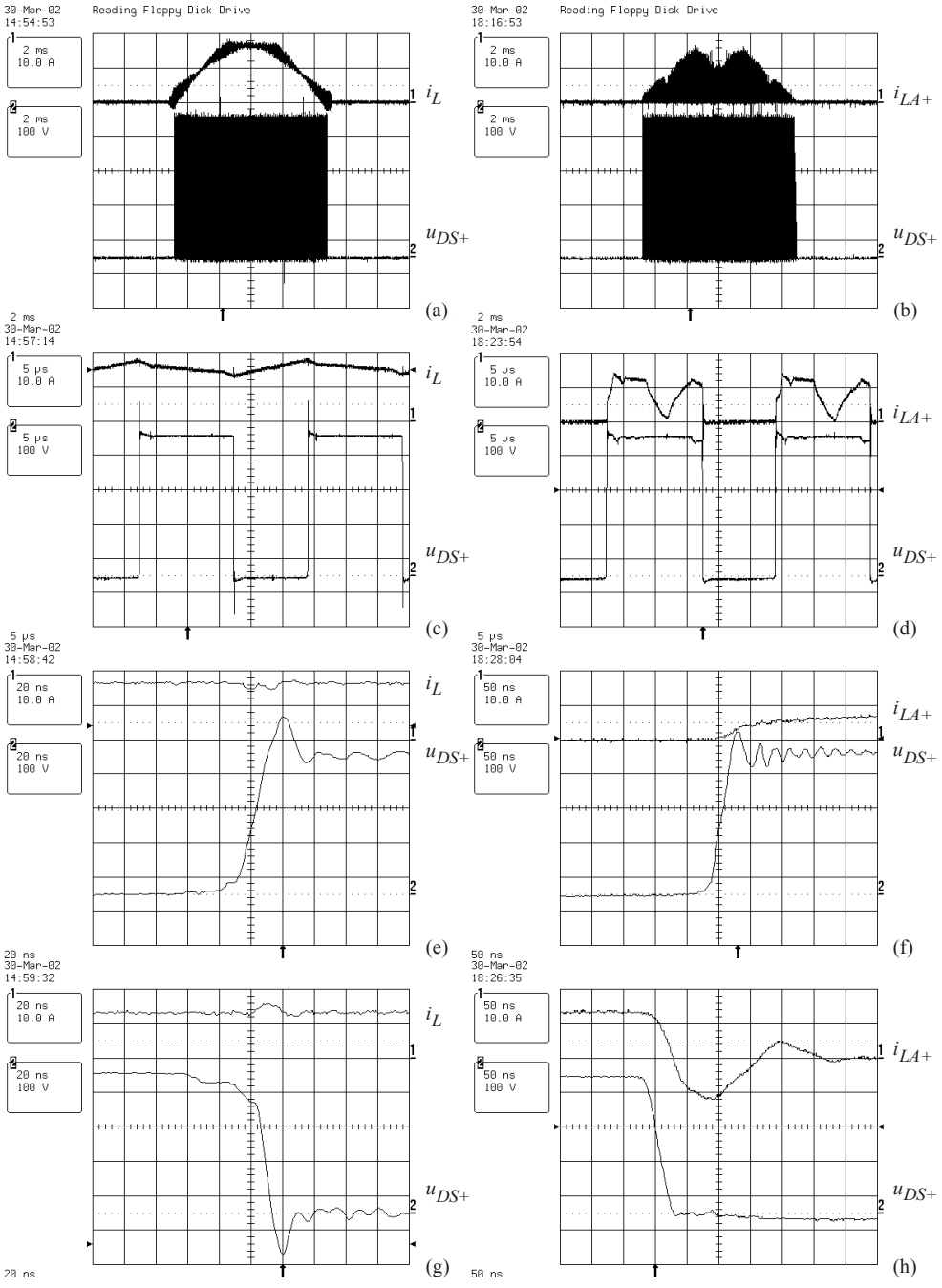

Fig.8: Left column **(a)**, **(c)**, **(e)**, **(g)**: waveforms without turn-on snubber, top trace **1**: mains diode current i_{DN+}, bottom trace **2**: power transistor drain-source voltage u_{DS}; right column **(b)**, **(d)**, **(f)**, **(h)**: waveforms with turn-on snubber, top trace **1**: auxiliary winding current i_{A+}, bottom trace **2**: power transistor drain-source voltage u_{DS}. **(b)**: the turn-on snubber does not work properly in the whole mains period, especially at the maximum (peak) of the input inductor current (in the middle of **(a)**), where most of the losses are caused. **(d)**: the subsequent switching of another phase ocurring within the turn-off interval of the phase considered does affect the current commutation into the auxiliary winding and/or does impair the proper operation of the snubber. **(e)**, **(f)**: the turn-on snubber does not increase turn-off overvoltage. **(g)**, **(h)**: turn-on with zero voltage in case of applying the turn-on snubber.

5 EXPERIMENTAL RESULTS

5.1 Investigation of the turn-on snubber

Figure 7 shows the schematic of the applied turn-on snubber. The auxiliary winding L_{A+} is realized by $N_{A+} = 3$ turns wound together with the main winding of $N = 48$ turns on the center leg of an iron powder E-core. For a detailed description of the principle of operation of the snubber circuit please refer to [13] and [6]. The results of the experimental analysis of the snubber are shown in **Fig.8** for a mains voltage of $U_{N,l\text{-}l} = 320V$ where a reduction of the turn-on losses and/or an improvement of the efficiency would be of special importance due to the high conduction losses and/or large switching current.

As shown in Figs.8(e) and (f) the turn-on snubber does not increase the power transistor turn-off overvoltage and the turn-on is at zero voltage (cf. Fig.8(g) and (h)). However, although the winding ratio has been selected according to the dimensioning guidelines ($n = N / N_A = 16$), the turn-on snubber does not operate properly within the whole mains voltage and current range, i.e. it is not possible to force the free-wheeling diode current completely into D_{A+} within each turn-off interval (cf. Fig.8(b)).

In the vicinity of the maximum of a mains phase

voltage and/or mains phase current the switching state change of another phase leg occurring subsequently to the turn-off of the power transistor considered does change the sign of the voltage across the phase input inductor. Accordingly, the auxiliary current does start to commutate back from the auxiliary diode into the conventional free-wheeling diode D_{F+} (see middle of the turn-off period in Fig.8(d)). The time remaining after the removal of the disadvantageous switching state until again turning-on the power transistor then could be not sufficiently for forcing the current again back into the auxiliary diode.

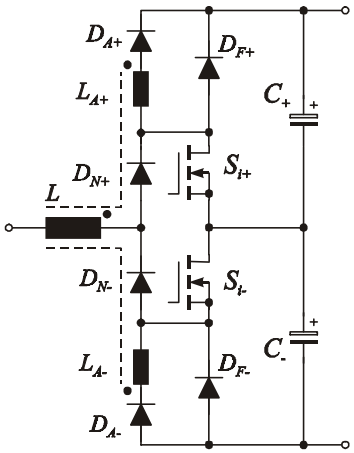

Fig.7: Detail of a bridge leg incorporating an extension of the turn-on snubber concept proposed in [6].

This behavior is specific to three-wire three-phase systems ($i_{N,R} + i_{N,S} + i_{N,T} = 0$) where a change of a switching state of a phase leg does take influence on all three phases and cannot be observed in single-phase PWM rectifier systems.

Another drawback of the snubber is the overvoltage clamping required for the auxiliary diodes D_A. A *DRC*-snubber circuit connected across the auxiliary winding and a capacitor in parallel to the auxiliary diode have to be provided in order to limit the transient turn-off overvoltage of the auxiliary diode to admissible values. These clamping circuits (C_{LA} = 1.5nF, C_{DA} = 470pF) do cause additional realization effort and additional losses. Accordingly, in combination with the limited functionality of the turn-on snubbers in intervals of a mains period no measurable power loss reduction does result for employing the turn-on snubber. Therefore, the snubber concept cannot be recommended for practical application for wide input voltage range three-phase three-wire PWM rectifier systems. A more detailed description of the snubber operating behavior therefore shall be omitted here for the sake of brevity.

5.2 Efficiency, Power Factor, THD

The results of the experimental analysis of the efficiency, the power factor and the current total harmonic distortion for different input voltages ($U_{N,l-l}$ = 320, 400, 480, 530V) are shown in **Fig.9**. Although the unit is designed originally for an output power of P_O = 10kW the measurements are performed up to an output power of $P_{O,max}$ = 12.5kW which corresponds to a permanent overloadability of 20%. It turned out, that the efficiency without employing the turn-on snubber ($\eta \approx 97.15\%$ @ P_O = 10.5kW, $U_{N,l-l}$ = 320V) is higher as expected according to the calculation of Tab.1 (η = 96.81% @ P_O =10.5kW, $U_{N,l-l}$ = 320V).

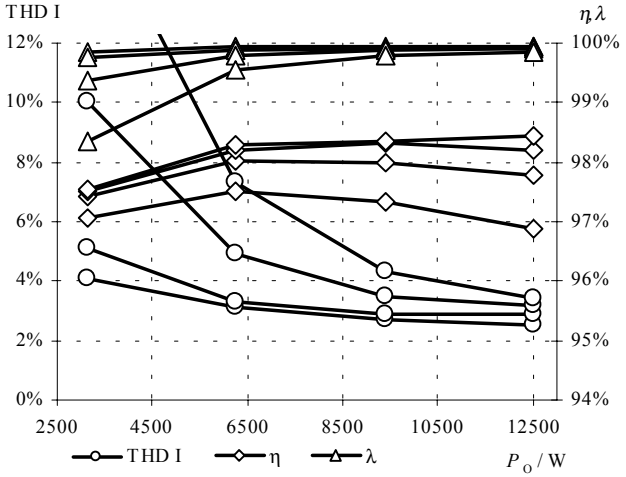

Fig.9: Graph of the current total harmonic distortion THD I, the power factor λ and the efficiency η in dependency on the output power P_O of the rectifier system for input voltages $U_{N,l-l}$ = 320, 400, 480 and 530V. THD I has lower values (better performance) for $U_{N,l-l}$ = 320V, correspondingly the power factor λ (higher power factor for lower input voltage). The efficiency is best (up to η = 98.5%) for $U_{N,l-l}$ = 530V.

5.3 Practical Realization, Power Density

The practical realization of the rectifier system fitting into an enclosure of 2-U height is shown in **Fig.10**. The system does have a base area of 160 x 250mm^2 which corresponds together with the height of 2-U (V = 3.52dm^3) and a permanent output power capability of P_O = 12.5kW to a power density of

$$\rho = \frac{P_O}{V} = 3.55 kW/l \qquad (19)$$

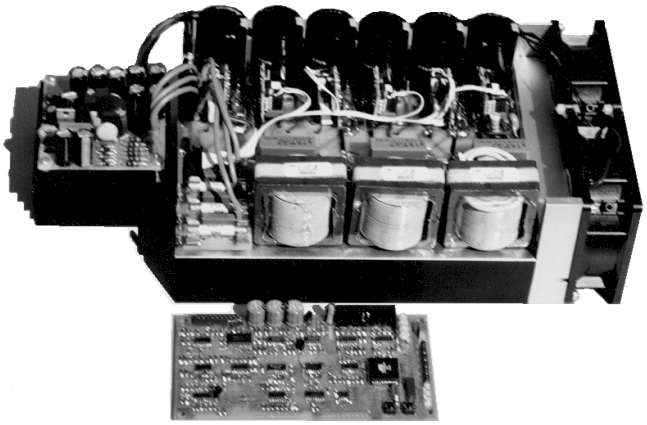

Fig.10: Prototype of the 10kW/2-U three-phase PWM rectifier system. The input inductors employing helical windings [8], [9] are mounted on top of the heatsink, the output capacitors (6 x 330µF/450V) are arranged along the power circuit PCB in immediate vicinity to the power semiconductors in order to minimize wiring inductances. Cooling is by two 80mm high airflow fans, the control board is realized in surface mount technology and is shown in front of the power circuit. The auxiliary power supply is shown on the left hand side. Overall dimensions without auxiliary power supply but including the cooling fans: 250mm x 160mm x 88mm (2-U).

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