Ultra Compact Three-Phase Rectifier with Electronic Smoothing Inductor

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***Abstract* — This paper describes the practical realization of an Electronic Smoothing Inductor (ESI) topology, which can reduce the harmonic current level, the output voltage ripple, and the volume of diode bridge rectifiers with a low realization effort. The control strategy and an EMI filtering concept for the ESI are presented and are verified by numerical simulation and experimental results for steady state and dynamic operation. By using the ESI a power density of 7.9kW /dm^3 for a 5kW rectifier prototype is realized. Furthermore a high efficiency of 98.6% and an improved power factor of 0.956 is obtained.**

I. Introduction

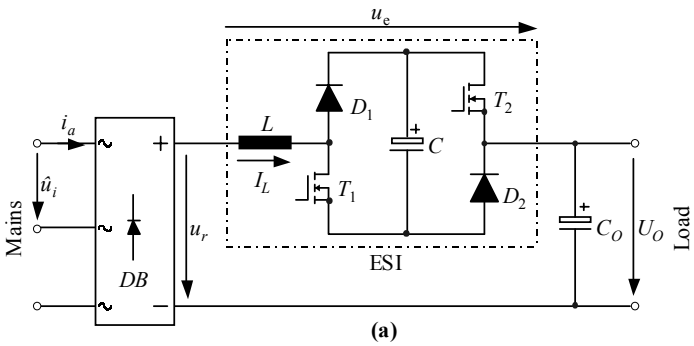
Three-phase rectifiers are widely used in motor drives, UPS, telecommunication and industrial process equipment. It is necessary that these three-phase rectifiers should have a low effect on the mains. This is typically achieved by applying inductor(s) on the DC side and/or the AC side of a three-phase diode bridge rectifier. Nevertheless, the volume and the weight of the rectifiers is significantly increased for large inductance values. In order to reduce the volume and the weight, PWM rectifier topologies, such as the bidirectional six-IGBT three-phase rectifier and unidirectional three-switch rectifiers have been developed. These rectifiers can realize sinusoidal mains currents that have a near unity power factor. However, the large number of power semiconductors, the associated gate drivers, and the complexity of the control circuits cause a high realization effort. Furthermore, the efficiency is reduced by 2 to 3% as compared to standard diode rectification. In order to avoid these disadvantages, the **E**lectronic **S**moothing **I**nductor (ESI), which consists of a small inductor, a minimum number of low voltage semiconductors and a low voltage capacitor, has been proposed [1]. The ESI performs the function of an inductor that has a controlled variable impedance and thus allows the reduction of the harmonic currents drawn from the mains with a low realization effort and reduced volume.

In [1], the hysteresis control and the PWM control schemes for the ESI have been described and the basic operation has been demonstrated with a laboratory prototype. However, aspects relevant for implementation in an industrial application, such as the detailed control strategy and the EMI filter design have not been considered.

In this paper, the practical realization of the ESI including the DC-link voltage control, the active damping for filter resonances, and the EMI filtering concept is described. The basic principle of operation and the advantages of the ESI are explained in **Section II**. In **Section III**, the main circuit design for a 5kW prototype including the EMI filter for fulfilling the requirements of CISPR 22 - Class A is described. The control concept for DC-link voltage control and the active damping of resonant currents is proposed in **Section IV**. In **Section V**, the proposed control scheme and the performance of the designed EMI filter are verified with simulation results. Finally, the experimental results of steady state and dynamic operation are demonstrated in **Section VI**.

II. Principle of Operation and Potential Advantages

In this section the principle of the ESI, operated by PWM control, and the advantages are introduced. The circuit schematic of the ESI connected to a three-phase diode rectifier, the time behaviour of the voltages, and the gate signals of the power transistors are depicted in **Fig.1**. Theoretically, the ESI voltage u_e varies within the range given by (1).



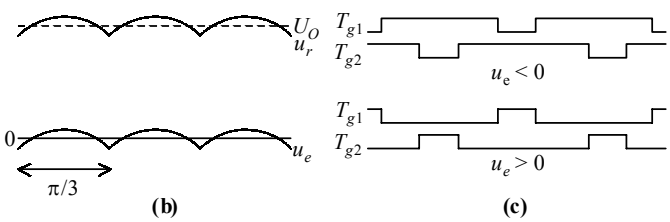


Fig.1: Circuit schematic of the ESI connected to a three-phase diode bridge rectifier **(a)**, time behaviour of operational voltages **(b)** and gate signals produced by PWM control **(c)**.

$$\frac{\sqrt{3}}{2}\hat{u}_i - U_O(=-0.089\hat{u}_i) \le u_e \le \hat{u}_i - U_O(=0.045\hat{u}_i) \quad (1).$$

In (1), $\hat{u}_i$ denotes the amplitude of the line-to line input voltage. The inductor current I_L can be controlled to a constant value (DC current with superimposed switching frequency current ripple) by operating T_1 and T_2 with variable duty cycle. In the turn-on period of both T_1 and T_2, the DC-link capacitor C is discharged and I_L increases. On the other hand, C is charged and I_L decreases when both transistors are turned off. In the period when either T_1 or T_2 is turned on, I_L does not flow in C. Therefore C is charged when u_e is positive and is discharged when u_e is negative. This topology brings the following advantages:

- low voltage semiconductors such as Schottky diodes and power MOSFETs can be employed in ESI since the DC-link voltage U_C is much lower than $\hat{u}_i$, which allows a high switching frequency, low conduction losses, and low switching losses;
- the inductance of L and/or the switching frequency current ripple is small since the apparent switching frequency is the doubled as compared to a synchronous operation of T_1 and T_2;
- the volume and the weight of ESI is considerably smaller when compared to a conventional passive smoothing inductor;
- the ripple current stress on the output capacitor C_O is lower as compared to a passive diode rectifier due to the constant DC-line current.

III. System Dimensioning

In this section the system dimensioning of a 5kW prototype including the main components of the ESI and the EMI filters is introduced.

A. Main Components

The specifications of the prototype of the ESI including the diode bridge rectifier are defined as:

Input line-to-line voltage: $U_{IN} = 400V_{ac} \pm 15\%$ (50/60Hz)
Nominal output power: $P_O = 5kW$
Nominal output voltage: $U_O = 540V_{dc}$
Nominal output current: $I_O = 9.26A_{dc}$
Switching frequency: $f_S = 70kHz$
(effective frequency: 140kHz).

The switching frequency, f_S, is set so that the resulting effective switching frequency, $2f_S$, is below the minimum frequency of the EMI standard minus one half of the bandwidth of the EMI receiver. In this case the use of an effective frequency of 140kHz is below the 150kHz starting frequency of CISPR 22. The inductance L is selected such that the amplitude of the current ripple is ±15% of DC current I_L at the nominal operating point. Accordingly, the inductance is calculated using (2).

$$L = \frac{(\sqrt{3}/2)\hat{u}_i - (U_O - U_C)}{0.3I_L \times 2f_S} D_{\max} \quad (2).$$

Note that D_{max} denotes the maximum duty cycle of the power MOSFETs. To achieve DC current control, U_C must be set as $U_C \ge 0.089\hat{u}_i$ (see (1)). In order to guarantee the operation also for unbalanced mains voltage, U_C is adjusted to $70V_{dc}$ ($=0.12\hat{u}_i$ at $U_{IN} = 400V_{ac}$). The current stress on C is defined by (3) [1].

$$I_{C,rms} = 0.186 I_L \sqrt{\frac{\hat{u}_i}{U_C}} \quad (3).$$

For the sake of briefness, the detailed derivation of (3) is omitted here. Capacitors showing sufficient ripple current capability are selected for C and C_O. Theoretically the average duty cycle of T_1 and T_2 is 0.5 (considering a π/3-wide interval of the mains period) and the current stress on the power transistors T_1 and T_2 and the power diodes D_1 and D_2 is equal [1]. **TABLE I** lists the main components and the calculated current stresses.

TABLE I Main circuit components and current ripple of 5kW ESI prototype: U_{IN}=400V_{rms}, P_O=5kW, f_S=70kHz.

Component	Symbol	Value	Ripple current
Inductor	L	20µH (2 in series)	0.8A
DC-link capacitor	C	330µF / 100V_{dc} (4 in parallel)	4.9A
Schottky diode	D_1, D_2	150V / 2 × 10A	
MOSFET	T_1, T_2	150V / 41A	
Three-phase rectifier bridge	DB	800V / 28A	
Output capacitor	C_O	47µF / 400V_{dc} (2 in parallel, 2 in series)	0.8A
Heat sink and fan		0.7K/W	

B. Filtering Concept and Realization

Due to the high switching frequency of the ESI an EMI filter attenuating the high frequency components is required. The chosen filtering strategy and topology is presented in **Fig.2**. As the converter is a three-phase rectifier a conventional approach would be to place a three-phase filter topology only at the input side of the diode bridge so that it is responsible for filtering any noise that could be coupled to the power grid. However, since the high frequency ESI is inserted in the DC-line, the part of the filter stage should be placed directly at the ESI input and/or on the DC side. This brings some advantages, namely:

- the RMS current in the output capacitor is decreased;
- the high frequency noise coupled to the output and to the input is lowered. This causes the mains side filter to be of smaller volume and the output voltage to present less high frequency ripple;
- high frequency noise is filtered more effectively and/or total volume of the filter can be reduced since the noise is directly filtered close to its origin;
- the rated voltage for the ESI input filter capacitors is much lower than for a mains side filter capacitor and the total number of components is smaller as just a single filter stage has to be employed on the mains side for guaranteeing sufficient attenuation.

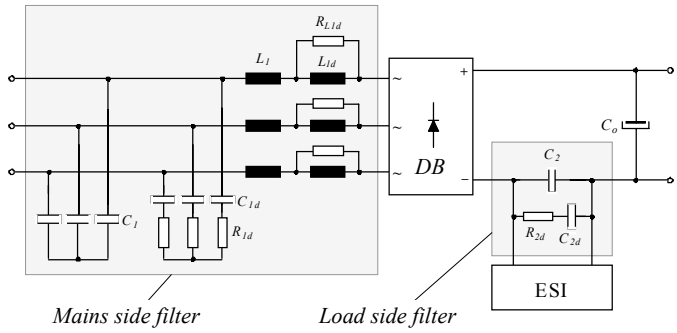


Fig.2: Filtering concept and topology.

For the system described in this paper the filter is designed according to the requirements of CISPR 22 for equipment classified as Class A. The design of the filter stages is performed using a procedure described in [2]. The components used in the filtering are listed in **TABLE II**.

TABLE II EMI Filter components of 5kW ESI prototype for fulfilling CISPR 22 – Class A.

Component	Symbol	Qty.	Value
Capacitor	C_1	3	470 nF / 275 V_{ac}
Capacitor	C_{1d}	3	68 nF / 275 V_{ac} (3 in parallel)
Resistor	R_{1d}	3	39 Ω / 0.25 W (3 in parallel)
Inductor	L_1, L_{1d}	6	40 μH
Resistor	R_{LId}	3	33 Ω / 0.25 W (3 in parallel)
Capacitor	C_2	1	680 nF / 100 V_{dc}
Capacitor	C_{2d}	1	10 μF / 100 V_{dc}
Resistor	R_{2d}	1	18 Ω / 0.25 W (6 in parallel)

IV. CONTROL SCHEME

The basic control scheme including DC-link voltage control and reduction of resonances with active damping of the ESI is described in this section. The control block diagram and the current and voltage sensing is shown in **Fig.3**. The ESI is placed in the negative DC line to allow all the currents required for the control implementation to be measured by shunt resistors. The ESI input current, I_L, is controlled to reach the output current, I_O, by using feed forward control. There, a low-pass filter LPF_1 has to be employed for attenuating high frequency components being present in case of pulsating load current such when the rectifier is supplying a PWM inverter or a DC-DC converter. To detect the average output current two low pass filters, each with a cut-off frequency of 5.3kHz, are connected in series in LPF_1 in order to achieve sufficient attenuation of pulsating load currents as well as minimizing the detection delay time when the load is dynamically changes.

Any resonant currents that occur in the load side filter at the diode bridge commutations are detected by using a high-pass filter and are actively damped by the main control loop. The high pass filter, *HPF*, is used to sense the resonant current and to block the low frequency components of the rectifier current.

The loss compensation value R, which is the gain for the current control, is adjustable in order to control the current shape of I_L [1]. A High R-value produces a low six times mains frequency current ripple on the DC-line. However the detected signal of I_L has a ripple and the ripple signal is multiplied by the R-value. For the 5kW ESI control circuit R-value is set to 30 in order to keep the low ripple signal in the control circuit. For attenuating the equivalent switching frequency ripple a low pass filter LPF_2 should be employed in the main control loop. The cut-off frequency is designed around 400Hz, which should be a higher frequency of the six times of the mains frequency (300Hz or 360Hz) and reduce 140kHz ripple to sufficient value.

For controlling the DC-link voltage, U_C, a PI-type controller is employed and connected in parallel with the main control loop. The gate signals Tg_1 and Tg_2 are determined by intersecting the control signals and a triangle waveform.

V. NUMERICAL SIMULATIONS

In this section the circuit operation and the control scheme are verified by using digital simulations produced by the software package PSIM version 6.1. The input phase current waveforms are shown in **Fig.4**. By applying the active damping control, the resonant current peaks occurring after the commutation of the diode bridge rectifier are reduced in amplitude as can be seen in Fig.4(a) and (b). **Fig.5** shows the output voltage U_O and the DC-link voltage U_C. It can be seen that the DC-link voltage is successfully controlled to the low value of 70V_{dc} and the output voltage ripple is small due to the almost constant DC current.

The simulation result of the differential mode filter performance is depicted in **Fig.6**. The expected simulation result shows that the designed filters for ESI can fulfill CISPR 22-class A limit.

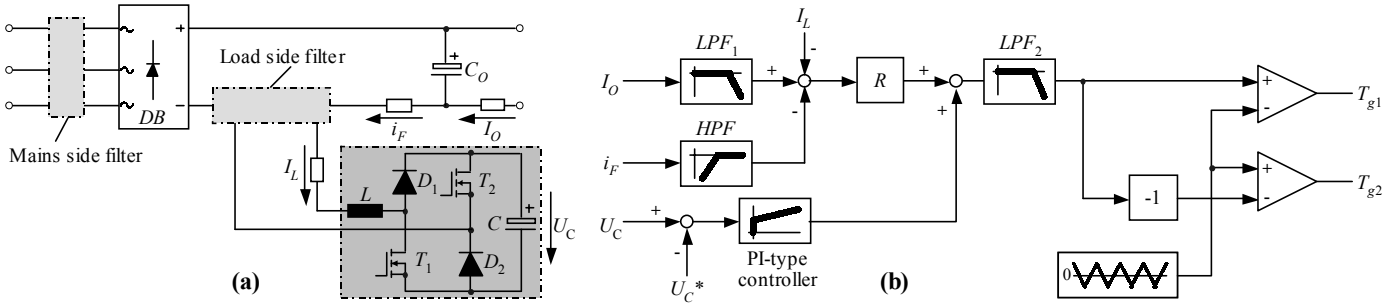


Fig. 3: Current and voltage sensing **(a)** and control block diagram with PWM control **(b)** of the ESI.

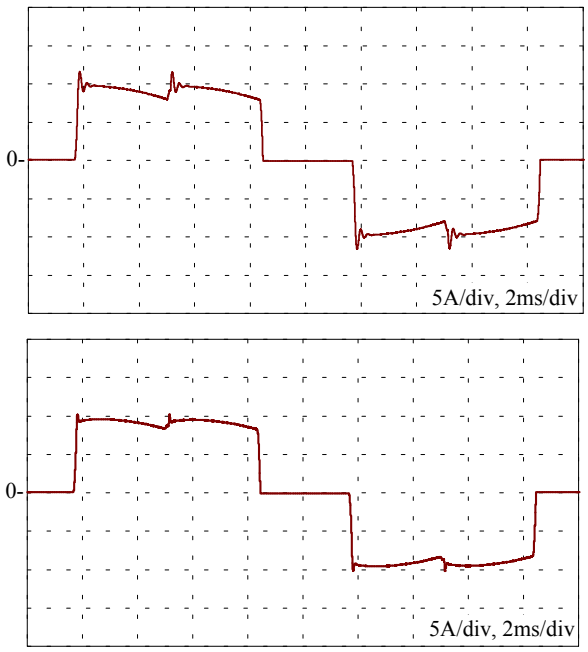


Fig.4: Simulated input current waveforms without active damping control **(a)**, with active damping control **(b)** for the nominal operating condition of 5kW.

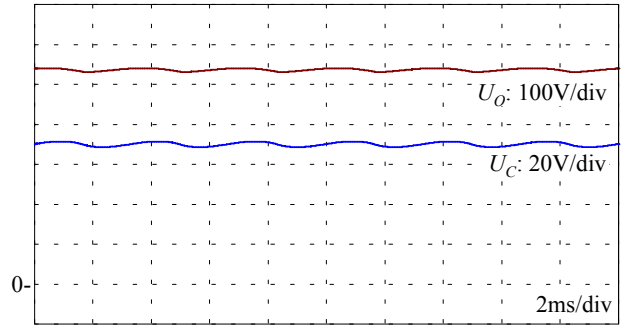


Fig.5: Simulated output voltage U_O and DC-link voltage U_C waveforms at the nominal operating condition of 5kW.

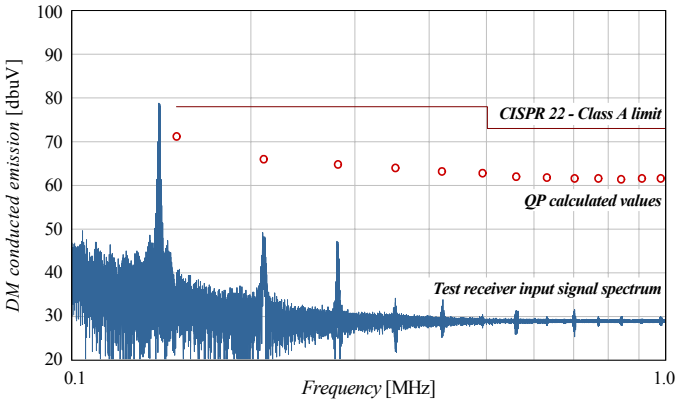


Fig.6: Expected differential mode filtering result with the designed filters at the nominal condition. Shown: CISPR 22 – Class A limit line; Input signal spectrum for the test receiver, and; calculated quasi-peak measurement values for the critical frequencies.

VI. Experimental Results

In this section the experimental results from the steady state and dynamic operation of a prototype and the distribution of the losses are introduced.

The photograph of the complete 5kW three-phase rectifier including ESI is shown in **Fig.7**. The prototype includes the three-phase diode bridge, EMI filters, output capacitor and pre-charge relays and resistors, ESI circuit, and the control and protection electronics. Due to the use of low voltage components the realization effort is low, the physical size is small (10.5cm×10.1cm×6cm), and a high power density of 7.9kW/dm^3 is obtained.

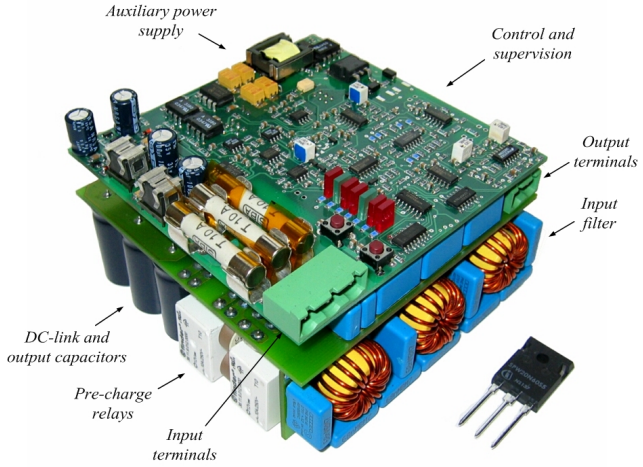


Fig.7: Photograph of the complete 5kW rectifier prototype (includes ESI, diode bridge, output capacitor, EMI filters, control circuits). Power density: 7.9kW/dm^3, size 10.5cm×10.1cm×6.0cm (4.1″×4.0″×2.6″), weight: 560g (19.8 ounces).

A. Steady State Operation

The measured input current for the cases where active damping is turned off and turned on is shown in **Fig.8.** As compared to the input current waveform without the active damping control (Fig.8(a)), the resonances of the input current are clearly reduced (Fig.8(b)). The experimental results show that the input current waveforms are in close correspondence to the simulation result in Fig.4. The impedance of the mains causes the slight differences between the simulation and experimental results concerning the resonant frequency and the rising and falling edge di/dt of the input current. The input current spectrum of the ESI using the active damping control is depicted in **Fig.9** and it can be seen that the 5th, 7th and higher frequency components of the input current are reduced compared to the theoretical levels of a standard bridge rectifier. The THD of the input current is 28.2% at the nominal operating point. As shown in **Fig.10** the designed prototype can operate under light load condition without any problem.

The DC-link voltage can be set and controlled at 70V$_{dc}$ as shown in **Fig.11**. Therefore, it is verified that the proposed control scheme is able to securely control the DC-link voltage. **Fig.12** shows the experimental waveforms of the output voltages. In Fig.12(a) the ESI does not operate and a high output voltage ripple is generated. On the other hand, by

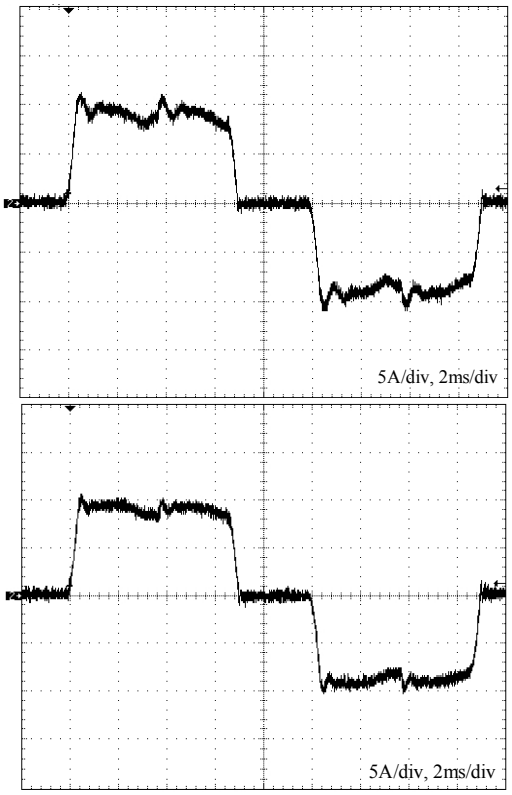


Fig.8: Measured input current waveforms without resonant current control **(a)**, with resonant current control **(b)** for the nominal operating condition of 5kW.

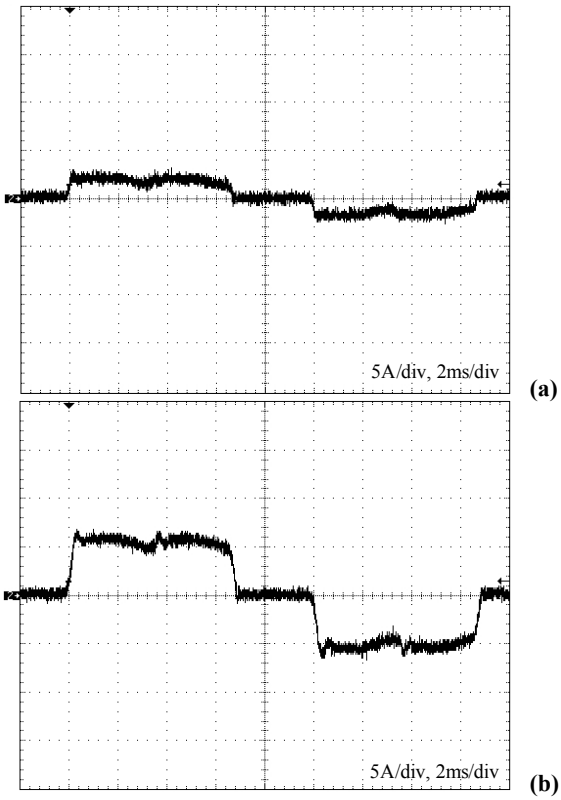


Fig.10: Measured input current waveforms under light load condition at P_O=1kW **(a)** and P_O=3kW **(b)**. Operating condition: U_{IN}=400V_{ac} / 50Hz, and f_s=70kHz.

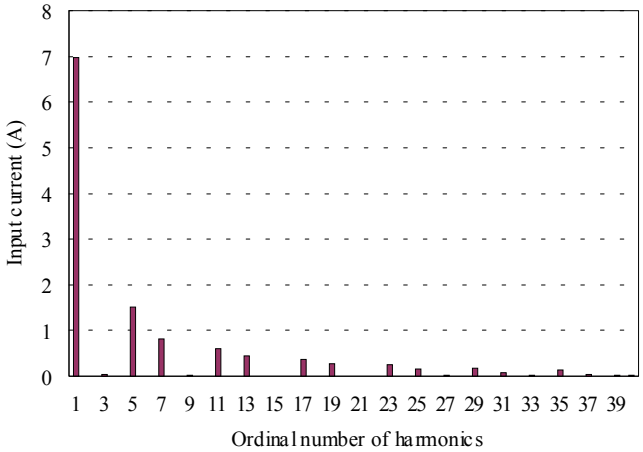


Fig.9: Measured input current spectrum at the nominal condition. The THD: 28.2%.

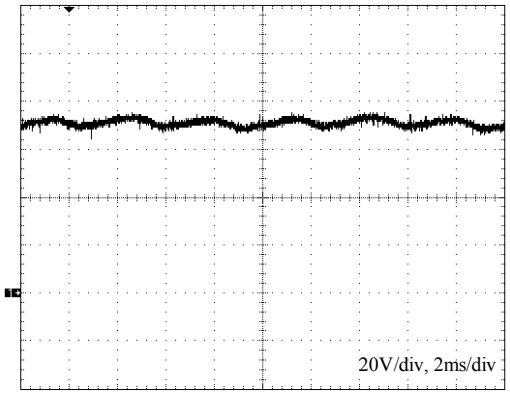


Fig.11: Measured DC-link voltage waveform at the nominal condition. Average value is 70V_{dc}.

operating the ESI the output voltage ripple is greatly reduced as can be seen in Fig.12(b).

The system efficiency and the power factor as a function of the output power are depicted in **Fig.13** and **Fig.14**. It should be pointed out that the measured efficiency includes the losses in the three-phase diode bridge, the output capacitor, EMI filters, control board, and fan. These results show that high efficiency is kept and the power factor is improved over the whole range of operating points. The efficiency and the power factor at the nominal operating point (U_{IN} =400V_{ac} / 50Hz, P_O =5kW, f_s=70kHz) are 98.6% and 0.956 respectively.

The distribution of the losses in the whole system is shown in **Fig.15**. The switching losses are derived from actual device measurements taken from the prototype and the losses of the other components are analytically calculated. The total loss of the whole system is 62.6W and each loss component is relatively low compared to the loss of the diode bridge. The total loss in the ESI, which includes the MOSFETs, the Schottky diodes, the inductors, and DC-link capacitor is 24.8W and approximately equal to the loss of the diode bridge. This calculation result clearly shows that the low losses are due to the use of low voltage components in the ESI.

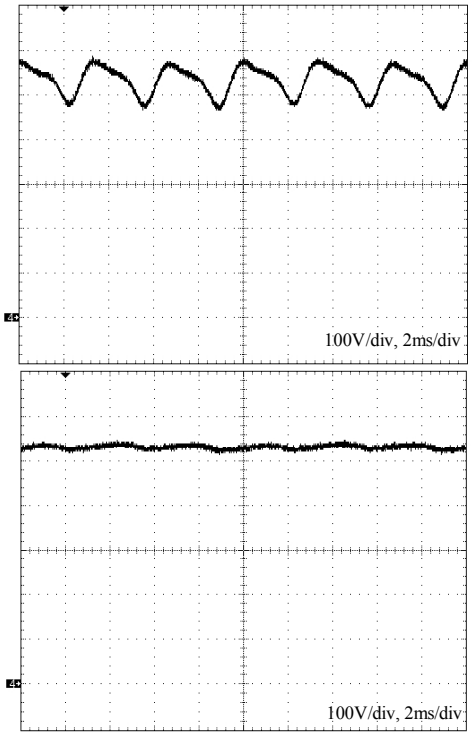


Fig.12: Measured output voltages without operation of the ESI **(a)** and with operation of the ESI **(b)** at the nominal condition using a resistive load.

B. Dynamic Operation

The start-up and the shut-down behavior of the ESI are given in **Fig.16**. For the ESI start-up case the input voltage is already applied, the load current is flowing and control circuit is keeping the transistors turned on (U_C=0V). The control circuit then starts switching the transistors and the DC-link voltage U_C changes from zero to 70V_{dc} without any large overshoot (Fig.16(a)). The waveforms of the input current i_a and output voltage U_O are immediately improved once U_C is charged.

When no load is connected to the output, U_C can not be charged because no current flows in the ESI. Once the load current flows, U_C can be charged and the ESI is able to operate. Under no-load conditions the DC-link capacitor voltage, U_C, can be charged up during a pre-charge operation if a large output capacitor is employed because the voltages on the capacitors depend on the ratio of the two capacitors. Under pre-charge the transistors are turned off and the DC-link capacitor and the output capacitor are connected in series with a resistor to limit the in-rush current. Consequently, the ESI can operate once U_C reaches the nominal voltage (cf. Fig. 11 in [1]). For the case of a large output capacitance the control circuit must start to operate by turning on the transistors when U_C reaches the nominal voltage.

During of the ESI shut-down phase of operation (Fig.16(b)) the duty cycle of T_1 and T_2 is gradually increased in order to avoid any step changes in the ESI current. Once U_C reduces to zero the transistors T_1 and T_2 are permanently turned on so that the DC-link capacitor is bypassed.

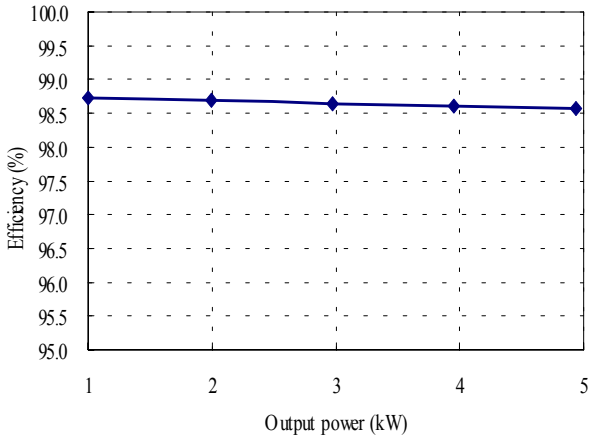


Fig.13: Measured efficiency in dependency on the output power. Operating conditions: U_{IN}=400V_{ac} / 50Hz, f_s=70kHz.

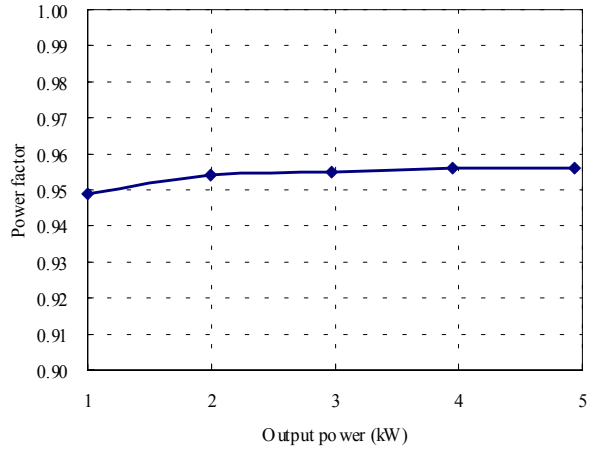


Fig.14: Measured power factor in dependency on the output power. Operating conditions: U_{IN}=400V_{ac} / 50Hz, f_s=70kHz.

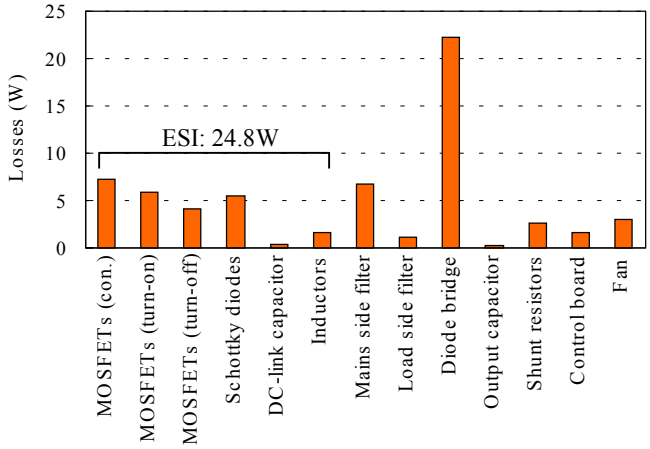


Fig.15: Distribution of system losses at the nominal condition of 5kW.

The dynamic operation during step load changes is shown in **Fig.17**. The load is changed from 3 to 100% of the nominal output power (see Fig.17(a)). The small oscillation of the DC-link voltage, which is approximately ±15V, occurs after the load condition is changed. However the peak voltage is 82V which is below the rated voltage of the DC-link capacitor (100V) and settles within 25ms. The final output

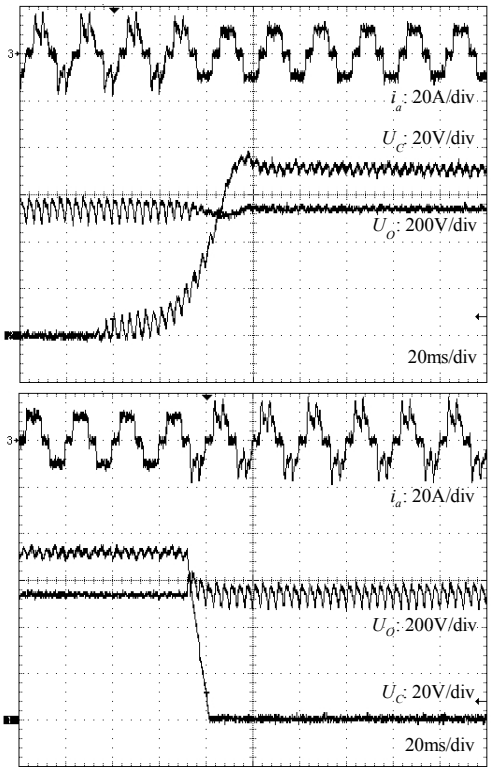


Fig.16: Measured dynamic behavior of input current i_a, DC-link voltage U_C, and output voltage U_O waveforms at start-up **(a)** and shut-down **(b)** at the nominal operating condition.

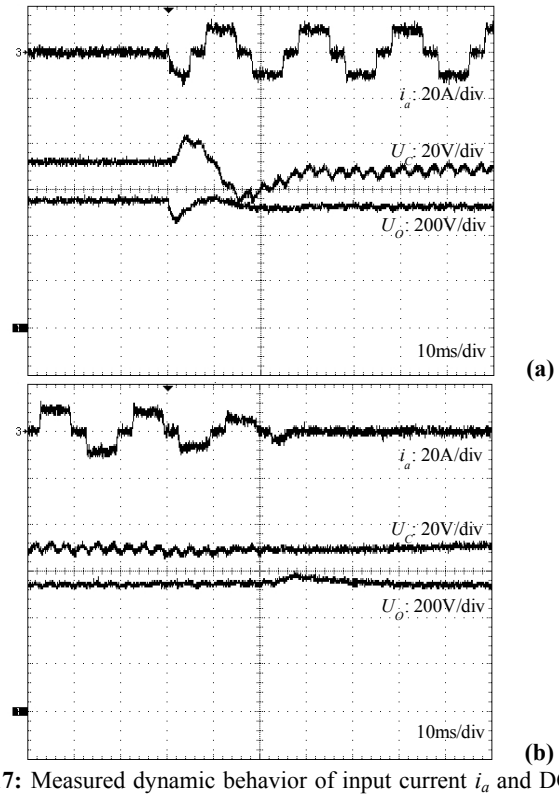


Fig. 17: Measured dynamic behavior of input current i_a and DC-link voltage U_C, and output voltage U_O at the changes from 3 to 100% **(a)** and from 100 to 3% **(b)** of the nominal output power.

voltage is lower than expected due to the high impedance of the test input voltage supply. This supply impedance also reduces the peak current of the input current waveforms when the ESI is not operating (see the first three cycles in Fig.16(a) or the end cycles in Fig.16(b)) compared to the level expected from using the small value of inductance in the rectifier.

When the load power is changed from 100 to 3% (Fig.17(b)) no large overshoot or undershoot of the voltages happens. In the time after the load drop the output voltage is larger than the peak of the input voltage and the DC-link voltage does not change because the DC-link capacitor is protected, by the diode bridge, from a reverse current. As the results verify, the ESI is able to operate under dynamically changing load conditions.

VII. Conclusions

The practical realization for the ESI has been introduced in this paper. The DC-link voltage control and active damping of the resonant currents have been proposed and verified by the numerical simulations. A 5kW prototype, which has a high power density of 7.9kW/dm^3 and a low realization effort, has been built and experimentally evaluated. The DC-link voltage is successfully controlled and resonances are reduced by the proposed control scheme. High efficiency of 98.6% and improved power factor of 0.956 at the nominal operating point are obtained with the prototype. In addition, the dynamic operation during start-up, shut-down, and load steps is successfully demonstrated. Furthermore, the EMI filtering concept and the advantages have been presented and numerically simulated. In future work, the experimental results for the EMI behavior will be verified and the volume and the efficiency of the ESI rectifier system will be analytically compared to a conventional diode bridge rectifier with a passive smoothing inductor.

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