Novel Hybrid 12-Pulse Boost-Type Rectifier with Controlled Output Voltage

KAZUAKI MINO, Student, IEEE

GUANGHAI GONG, Student, IEEE

JOHANN W. KOLAR, Senior Member, IEEE
Swiss Federal Institute of Technology (ETH) Zurich

Novel hybrid 12-pulse line interphase transformer (LIT) rectifier systems with integrated single-switch or two-switch boost-type output stage that ensure a constant output voltage independent of mains and load conditions are proposed for supplying actuators of future more electric aircraft. The principle of operation, the dimensioning, and the system control are discussed. The theoretical considerations are experimentally confirmed for a 10 kW laboratory prototype. Finally, the single- and the two-switch system are comparatively evaluated concerning the level of input current ripple, power factor, and overall efficiency.

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Authors' address: Swiss Federal Institute of Technology (ETH) Zurich, Power Electronic Systems Laboratory, Physikstr. 3, ETH Zentrum, ETL H23, CH-8092 Zurich, Switzerland, E-mail: (kolar@lem.ee.ethz.ch).

I. INTRODUCTION

For future more electric aircraft the conventional fly-by-wire hydraulic flight control surface will be partly replaced by power-by-wire electro-hydrostatic actuators (EHAs) that require less maintenance, have a higher efficiency, and are more fault tolerant. The EHA system consists of variable speed electric motors, fed by inverter systems, which are driving dedicated hydraulic pumps to provide local hydraulic power to the actuators. To supply an inverter's dc voltage link from the three-phase variable frequency and variable voltage aircraft electrical system, ac/dc rectifiers with a low effect on the mains are employed [1–4].

In [4] various rectifier concepts were compared for powering an EHA and it was identified that a passive 12-pulse rectifier system with line interphase transformer (LIT) is competitive with an active three-level pulsewidth modulated (PWM) rectifier where efficiency and power density are concerned. However, a remaining drawback of the passive system is the dependency of the output voltage on the mains voltage level, mains frequency, and the output power, especially if voltage and frequency of aircraft power system are varying over a wide range. Therefore, an extension of the passive 12-pulse LIT rectifier to a rectifier with a controlled output voltage was described in [4] and [8].

The hybrid 12-pulse LIT boost-type rectifier systems, the single-switch hybrid 12-pulse LIT rectifier (SSHR) (see Fig. 1(a)) and the two-switch hybrid 12-pulse LIT rectifier (TSHR), (see Fig. 1(b)) proposed in [4] and [8] are analyzed here in detail. In Section II the principle of operation of the SSHR and the TSHR is analyzed and the performance is shown by digital simulations. The dimensioning of the systems and the distribution of the losses between the main active and passive components is discussed in Section III. Furthermore, a low-cost zero sequence current control scheme ensuring an equal partitioning of the load to the individual systems of the TSHR is proposed. Experimental results of the TSHR are given in Section IV. In Section V the SSHR and the TSHR are comparatively evaluated considering their mains behavior and efficiency.

The following input voltage and input frequency range is assumed here:

$$U_N = 96\ \mathrm{V_{rms}} \ldots 132\ \mathrm{V_{rms}}$$

$$f_N = 400\ \mathrm{Hz} \ldots 800\ \mathrm{Hz}$$

where the nominal values are $U_{N,r} = 115\ \mathrm{V_{rms}}$ and $f_{N,r} = 400$ Hz, and the rated output power $P_{O,r}$, is 10 kW.

II. BASIC PRINCIPLE OF OPERATION

In this section the basic principle of operation of the SSHR and the TSHR is shown by using results

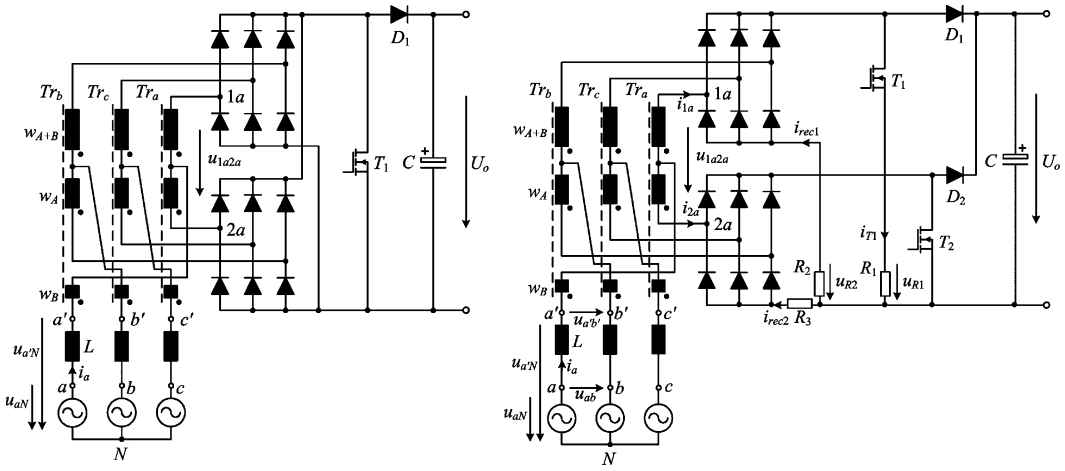

Fig. 1. Proposed three-phase hybrid 12-pulse boost-type rectifier systems. (a) Single-switch topology (SSHR). (b) Two-switch topology (TSHR).

from digital simulations produced by the simulation software SIMPLORER 6.0.

A. Single-Switch Hybrid 12-Pulse LIT Rectifier

The topology of the SSHR (see Fig. 1(a)) integrates a single-switch boost converter and a 12-pulse rectifier stage in order to achieve controllability of the output voltage. The output voltage of the system can be derived as [5, 8]

$$U_{\mathrm{O}} = \frac{1.52\hat{u}_a}{1 - D_{u1}} \tag{1}$$

where $\hat{u}_a$ is the amplitude of the mains phase voltage and D_{u1} denotes the duty cycle of the power transistor T_1. In Fig. 2(a) the results of a digital simulation of the system input phase currents are shown. They show an overall sinusoidal shape and they contain high frequency switching current ripples. The mains phase voltage u_{aN} and the corresponding input phase voltage $u_{a'N}$ between a' and N are depicted in Fig. 2(b). The mains phase voltage u_{aN} and the corresponding LIT voltage u_{1a2a} between $1a$ and $2a$ are shown in Fig. 2(c). The voltages $u_{a'N}$ and u_{1a2a} exhibit the typical shapes of a passive 12-pulse rectifier [5, 8] but are chopped with switching frequency.

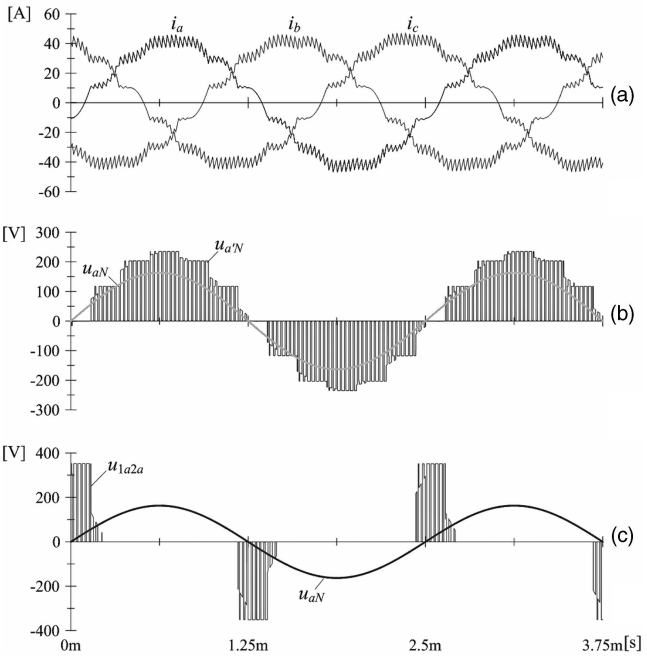

Fig. 2. Simulation of SSHR (see Fig. 1(a)). (a) Time behavior of input phase currents i_a, i_b, and i_c. (b) Mains phase voltage u_{aN} and corresponding current forming input phase voltage $u_{a'N}$. (c) Mains phase voltage u_{aN} and corresponding LIT voltage u_{1a2a}. Simulation parameters: U_N = 115 V_{rms}, f_N = 400 Hz, U_{O} = 350 V, P_{O} = 10 kW, switching frequency f_P = 33 kHz, D_{u1} = 0.3.

B. Two-Switch Hybrid 12-Pulse LIT Rectifier

1) *Basic Principle of Operation*: The topology of the TSHR is depicted in Fig. 1(b) where the power transistors T_1 and T_2 are operating with equal duty cycles in an interleaved manner in order to reduce the switching frequency ripple of the input currents.

The output voltage U_{O} of the system can be obtained in analogy to (1) as [5, 8]

$$U_{\mathrm{O}} = \frac{1.52\hat{u}_a}{1 - D_{u2}} \tag{2}$$

where D_{u2} is the duty cycle of the power transistors T_1 and T_2.

Fig. 3 shows the results of a digital simulation of the TSHR system. The input phase currents i_a, i_b, i_c are depicted in Fig. 3(a); the mains phase voltage u_{aN} and the corresponding input phase voltage $u_{a'N}$ and the LIT voltage u_{1a2a} are shown in Figs. 3(b) and (c).

As compared with the SSHR (see Fig. 2(a)) the switching frequency input current ripple amplitude is considerably reduced due to the (partial) cancellation of the harmonics of $u_{a'N}$. On the other hand, the LIT

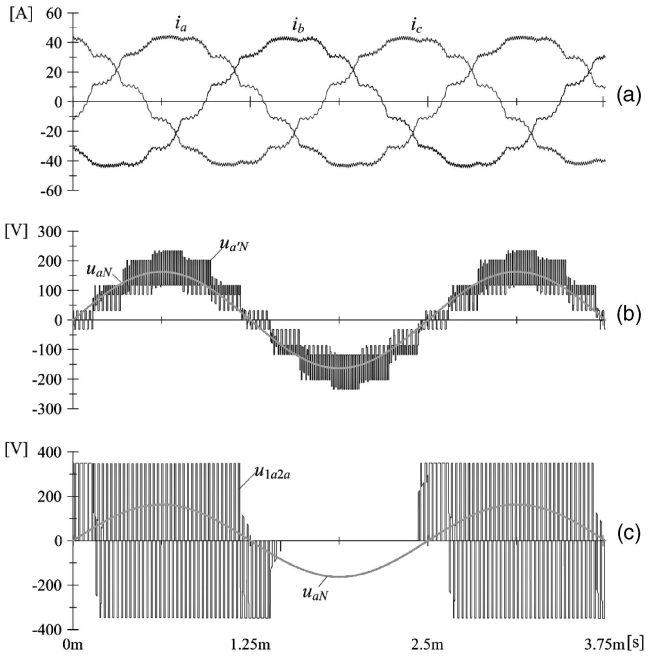

Fig. 3. Simulation of TSHR (see Fig. 1(b)). (a) Time behavior of input phase currents i_a, i_b, and i_c. (b) Mains phase voltage u_{aN} and corresponding current forming input phase voltage $u_{a'N}$. (c) Mains phase voltage u_{aN} and corresponding LIT voltage u_{1a2a}. Simulation parameters as for Fig. 2, $D_{u2} = 0.3$.

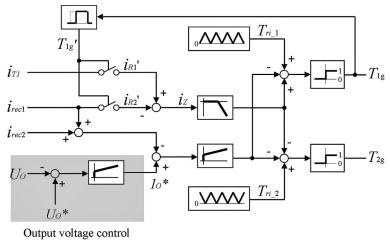

Fig. 4. Block diagram of TSHR control comprising zero sequence current control based on current measurement by shunt resistors (see Fig. 1(b)).

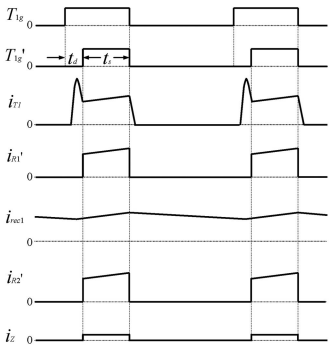

Fig. 5. Time behavior of key waveforms of TSHR zero sequence current control according to Fig. 4.

voltage u_{1a2a} (see Fig. 3(c)) is being chopped at twice switching frequency when the LIT secondary winding currents i_{1a} and i_{2a} are both positive and chopped at the switching frequency when only i_{1a} or i_{2a} is positive. The non-zero LIT voltage now extends over a half mains period and this results in increased LIT iron losses.

2) *Control of Zero Sequence Current*: Any slight difference between the duty cycles of the power transistors T_1 and T_2 would result in a zero sequence current flowing between the two rectifier bridges via the LIT. Accordingly, the currents in the two partial systems would not be balanced and this would cause higher current stresses on the power components and a low frequency distortion of the input phase currents.

Therefore, a zero sequence current control ensuring equal current partitioning has to be employed. The simplest way to achieve this is to directly measure the zero sequence current i_0, by summing the input phase currents of diode bridge 1 or diode bridge 2, $i_0 = 1/3(i_{1a} + i_{1b} + i_{1c}) = -1/3 \cdot (i_{2a} + i_{2b} + i_{2c})$, with a through-hole current transducer and then adjusting the duty cycles by negative feedback in order to eliminate i_0.

Alternatively, a zero sequence current control as shown in Fig. 4 could be implemented, which allows the detection of i_0 with a lower cost since the current measurement uses shunt resistors (see Fig. 1(b)). Corresponding key waveforms are depicted in Fig. 5. When the voltages u_{R1} and u_{R2} across the shunt resistors R_1 and R_2, which represent the transistor current i_{T1} and rectifier current i_{rec1} respectively, are identical (within the turn-on period of the metal-oxide-semiconductor field-effect-transistor (MOSFET) T_1) no zero sequence current i_0 is present in the system.

Accordingly, i_0 can be detected as difference of i_{T1} and i_{rec1}. In the control circuit the shunt voltages u_{R1} and u_{R2} are added in a period t_s, which is generated from the gate signal T_{g1} of T_1 and includes a delay time t_d in order to avoid the detection of a large current peak resulting from the reverse recovery of diode D_1. For a positive average value of signal i_Z, a zero sequence current is flowing in T_1 from the drain to source. In this case the control circuit reduces the duty cycle of T_1 and increases the duty cycle of T_2 to generate a zero sequence voltage component between the inputs of diode bridges, thus reducing the zero sequence current.

As an alternative to providing a control loop, the occurrence of a zero sequence current i_0 also could be prevented by two additional diodes decoupling the boost output stages such as shown in Fig. 14 for two parallel connected three-phase single-switch discontinuous mode rectifiers. Due to the higher conduction losses and the higher realization effort this concept has not been analyzed in anymore detail here.

A simple cascade control is employed in the TSHR, as shown in Fig. 4, where the difference of the output voltage and reference voltage is regulated by a

PI controller. The output of the PI controller provides the reference value of the output current and then a current error signal is created by subtracting the sum of the two rectifier currents i_{rec1} and i_{rec2} sensed by the shunt resistors R_1 and R_3, respectively.

III. SYSTEM DIMENSIONING

The input inductors ($L = 188\ \mu$H) of the rectifiers have to be designed with respect to the admissible amplitude of the 11th and 13th harmonic of the input current [4, 8]. The switching frequency of the TSHR is selected as $f_P = 33$ kHz, in order to keep a peak-to-peak input current ripple lower than 10% of the fundamental current amplitude. For achieving the necessary $\pm 15°$ phase shift of the corresponding input phase currents of diode bridge 1 and 2 (i_{1a} and i_{2a}) an LIT turns ratio of

$$W_B/W_A = 0.366 \tag{3}$$

is required [6]. From this the amplitudes of the fundamentals of i_{1a} and i_{2a} are [6]

$$\hat{i}_{1a} = \hat{i}_{2a} = 0.518\hat{i}_a. \tag{4}$$

As compared with the SSHR, the TSHR current stresses on the boost stage power semiconductors (T_1, T_2 and D_1, D_2) are advantageously cut in half. The dependency of the measured switching loss characteristics, resulting for employing a CoolMOS power transistor (600V/47A, SPW47N60C3, Infineon) in combination with an ultrafast recovery diode (600V/30A, DSPEP 30-60BR, IXYS), is depicted in Fig. 6. According to Fig. 6 the power transistor switching losses can be calculated as

$$P_S = f_P(k_1 I_{\text{rec,rms}}^2 + k_2 I_{\text{rec,avg}}) \tag{5}$$

(see [9]) where $I_{\text{rec,rms}}$ and $I_{\text{rec,avg}}$ are denoting the rms and the average value of the output current of one diode bridge. Assuming, in a first approximation, a continuous sinusoidal shape of the diode bridge input phase currents [6], the values for $I_{\text{rec,rms}}$ and $I_{\text{rec,avg}}$ are

$$I_{\text{rec,rms}} = \hat{i}_{1a}\left(\frac{3}{\pi}\int_{1/3\pi}^{2/3\pi}\sin^2\omega t\, d\omega t\right)^{1/2} = 0.956\hat{i}_{1a} \tag{6}$$

$$I_{\text{rec,avg}} = \frac{3\hat{i}_{1a}}{\pi}\int_{1/3\pi}^{2/3\pi}\sin\omega t\, d\omega t = 0.955\hat{i}_{1a}. \tag{7}$$

According to Fig. 6, we have for the transistor turn-on losses $k_1 = 0.4943\ \mu\text{Ws/A}^2$ and $k_2 = 13.33\ \mu$Ws/A, and for the transistor turn-off losses $k_1 = 0.6114\ \mu\text{Ws/A}^2$ and $k_2 = 1.469\ \mu$Ws/A; the diode reverse recovery losses are characterized by $k_1 = 0.1486\ \mu\text{Ws/A}^2$ and $k_2 = 4.789\ \mu$Ws/A.

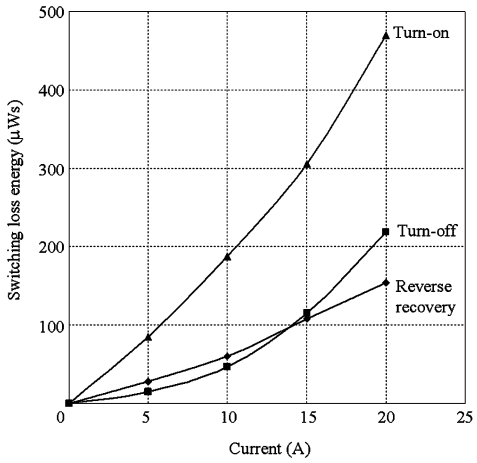

Fig. 6. Dependency of switching losses of a CoolMOS power transistor (600V/47A, SPW47N60C3, Infineon) in combination with an ultrafast recovery diode (600V/30A, DSPEP 30-60BR, IXYS). Parameters: switching voltage $U_O = 350$ V, turn-on gate resistor $R_{g(\text{on})} = 5\ \Omega$, turn-off gate resistor $R_{g(\text{off})} = 2.5\ \Omega$.

The conduction losses of the power transistors and the diodes can be calculated as

$$P_{\text{con},T1} = I_{\text{rec,rms}}^2 R_{\text{ON}} D_{u2} \tag{8}$$

and

$$P_{\text{con},D1} = U_F I_{\text{rec,avg}}(1 - D_{u2}). \tag{9}$$

With reference to the data sheet the power MOSFET's (SPW47N60C3) on-resistance R_{ON} is 0.133 Ω and the diode's (DSPEP 30-60BR) forward voltage U_F is 1.75 V for a junction temperature of 125°C. The maximum rms input current occurs at $U_N = 96$ V, $f_N = 800$ Hz, and $P_O = 10$ kW, where the efficiency is 90% considering the power losses in the active part and the phase displacement φ of mains current fundamental, and the mains voltage is $\cos\varphi = 0.837$ (see [8, Fig. 5 and 6]).

The calculated maximum losses in the active part of the TSHR are listed in Table I. There the maximum temperature difference between the MOSFET junction and case is 34.8°C and for the power diodes it is 42.9°C considering a heat sink temperature of 85°C.

In the SSHR, the two power MOSFETs and the two diodes are connected in parallel to accommodate the higher current stresses. Therefore, both systems show equal realization effort concerning the power semiconductors. The main components of the TSHR are listed in Table II and a 10 kW TSHR laboratory prototype is shown in Fig. 7.

IV. EXPERIMENTAL RESULTS

A 10 kW prototype of the TSHR has been developed for verifying the theoretical analysis. The input current waveforms, the zero sequence current time behavior, and the input current spectrums are shown in Fig. 8. When no zero sequence

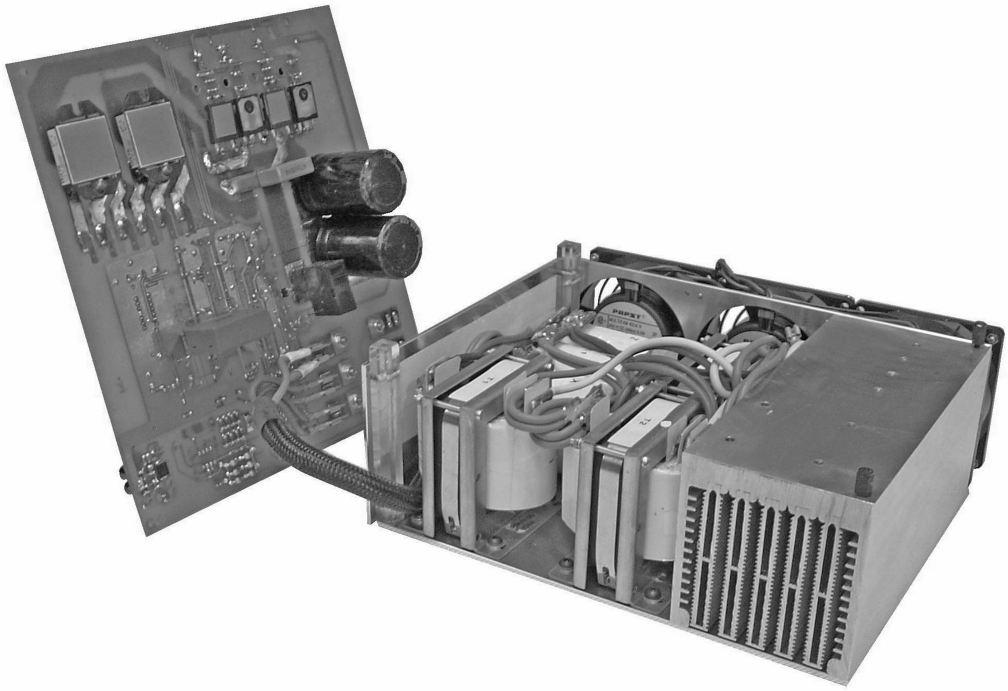

Fig. 7. Prototype of 10 kW TSHR; overall dimensions: $24.0 \times 22.9 \times 11.7$ cm^3 and weight of 8.2 kg.

TABLE 1
Maximum Losses of TSHR Boost Stage Power Semiconductors Occurring for U_N = 96 V, f_N = 800 Hz, U_O = 350 V, P_O = 10 kW, f_P = 33 kHz

MOSFET	Conduction losses Turn-on losses Turn-off losses	67 W 30 W 19 W	116 W
Diode	Conduction losses Reverse recovery losses	29 W 10 W	39 W
Total power semiconductor losses			310 W

TABLE II
List of Components Employed in TSHR

Component	Symbol	Type
Input inductors	L	Value: 188 μH Core: S3U 48b Material: Trafoperm N2/0.1 mm
Input transformer	Tr_a, Tr_b, Tr_b	W_A: 21 turns, W_B: 8 turns Value: L_{WA+B} = 66 mH, L_{WA} = 35.4 mH, L_{WB} = 4.74 mH Core: 2 × SM 65 Material: Trafoperm N2/0.1 mm
Diode bridge		2 × VUE 35-06NO7, IXYS
MOSFET	T_1, T_2	600 V/47 A, SPW47N60C3, Infineon
Output diode	D_1, D_2	600 V/30 A, DSPEP 30-60BR, IXYS
Output capacitor	C	2 × 560 μF/400 VDC, Rubycon

current control is used, the zero sequence current is very obvious in Fig. 8(a) and the input currents contain 3rd, 5th, and 7th harmonics (Fig. 8(d)). The implementation of zero sequence current control with either a current transducer, Fig. 8(b), or current shunts Fig. 8(c), reduces the zero sequence current to almost zero. The measured waveforms have good correspondence with the simulation results and the zero sequence current is successfully controlled by the proposed method as shown in Fig. 8(c). The system behavior for employing a zero sequence current control relying on a current transducer is depicted in Figs. 8(b) and (e). For both concepts the zero sequence current is eliminated and the input currents show about equal total harmonic distortion (THD) values (see Fig. 8(e) and Fig. 8(f)). In case no zero sequence current control would be provided a low frequency distortion of the input current would occur.

The measured input inductor voltage and the LIT voltage of the TSHR (see Fig. 9) are again in close correspondence to the simulated waveforms (see Fig. 3(b) and (c)). The dependency of efficiency η and the power factor λ for the TSHR on the output power are depicted in Fig. 10. For the nominal operating point (U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW) the efficiency is 95.0% and the power factor is 0.95. The output voltage is controlled to U_O = 350 V and is independent of the operating condition. As no input filter has been considered, the input current ripple amplitude is comparable to the fundamental amplitude at low output power levels and this results in a relatively low power factor for this condition. The low power factor at high

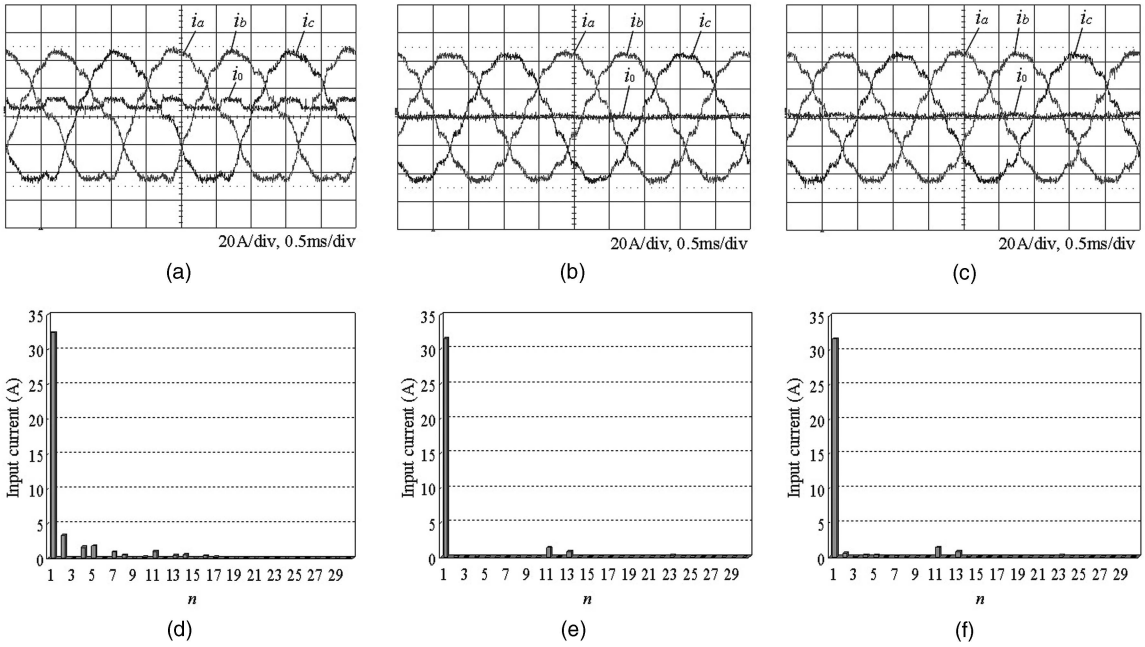

Fig. 8. Measured input current waveforms i_a, i_b, i_c, zero sequence current i_0 and input current harmonics (n denotes ordinal number of harmonics); (a) and (d) without zero sequence current control; (b) and (e): as (a) and (d) but employing zero sequence current control where i_0 is measured using a through-hole current transducer LA 55-P (50A, LEM Components); (c) and (f): as (a) and (d) but with proposed zero sequence current control employing shunt resistors for zero sequence current determination. Operating parameters: U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW, f_P = 33 kHz; THD of input current: (d) 13.7%; (e) 5.2%; (f) 5.7%.

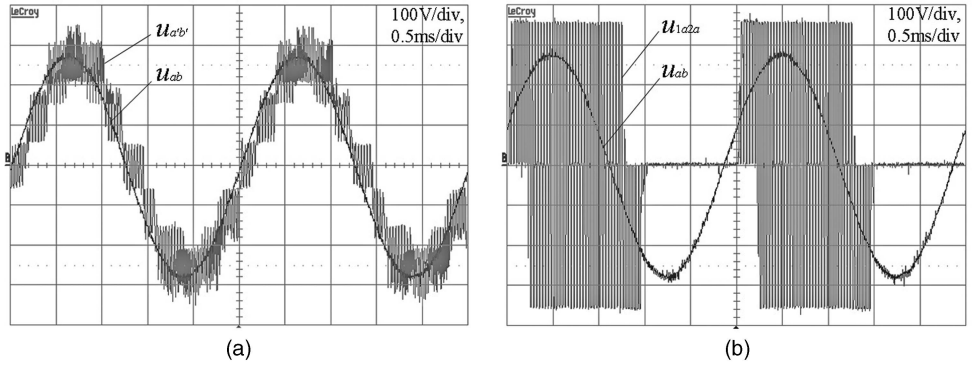

Fig. 9. Measured mains line-to-line voltage u_{ab} and LIT input line-to-line voltage $u_{a'b'}$ (see (a)). (b) Voltages u_{ab} and u_{1a2b} across windings W_{A+B} and W_A of LIT of TSHR. Operating conditions: U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW, f_P = 33 kHz.

output power and high mains frequency is due to the phase displacement between the input current and input voltage resulting from the voltage drop across the input inductors [4]. One has to point out that the system fulfills the requirements relating to low frequency input current harmonics [8] within the whole operating range.

V. COMPARATIVE EVALUATION OF SSHR AND TSHR

The distribution of the total losses between the main power components of the SSHR and the TSHR is depicted in Fig. 11. Due to the higher frequency of the input current ripple the SSHR shows higher iron losses in the input inductors. On the other hand, higher LIT iron losses occur for the TSHR as discussed in Section IIB (see Fig. 2(c) and Fig. 3(c)). In the case where the switching frequency of the SSHR would be doubled (f_P = 66 kHz), the main high frequency input current ripple components would occur at the same frequency and the input current ripple amplitude would be reduced and/or both systems would show about equal electromagnetic interference (EMI) filtering effort. However, the switching losses of the SSHR (which does not require a zero sequence current control and employs only a single gate drive circuit) would be doubled and/or a slight reduction of the converter efficiency would have to be accepted (see Fig. 11).

In Fig. 12, the input current spectrum of the SSHR is depicted for f_p = 33 kHz (see Fig. 12(a)) and

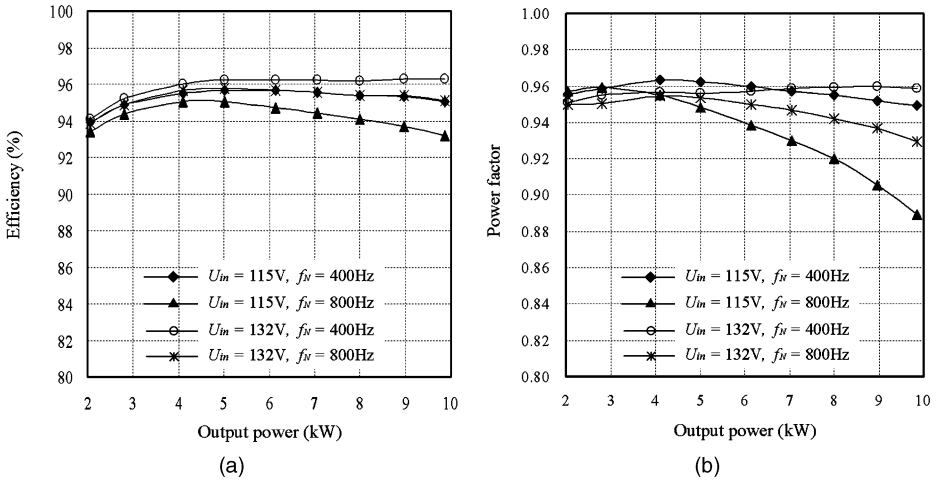

Fig. 10. Measured efficiency (a) and power factor (b) of TSHR in dependency on output power for different input voltages and frequencies. Operating conditions: U_O = 350 V, P_O = 10 kW, and f_P = 33 kHz.

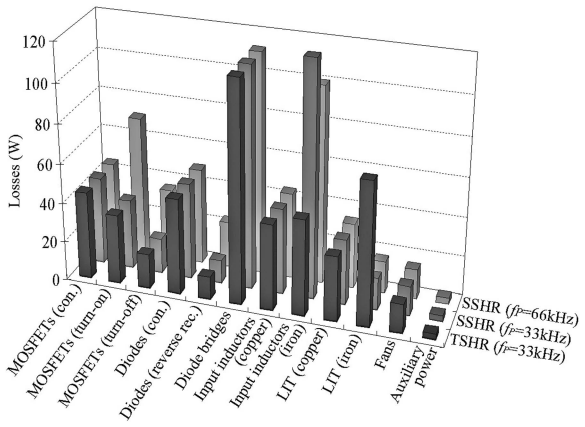

Fig. 11. Calculated distribution of losses of TSHR for switching frequency of f_P = 33 kHz and of SSHR for f_P = 33 kHz and f_P = 66 kHz. Assumed operating conditions: U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW. *Remark:* For calculating input inductor and the LIT winding losses high frequency effects (skin and proximity effect) were neglected as both windings are realized with copper foils. Losses of employed magnetic material determined by measurements and found considerably different to data provided by core manufacturer. Total calculated losses in very good correspondence with measured system efficiency.

f_p = 66 kHz (see Fig. 12(b)); and the spectrum of the TSHR is shown for f_p = 33 kHz (see Fig. 12(c)). The input current harmonics of the TSHR, around 33 kHz, are significantly reduced as compared with the SSHR, but cannot be cancelled completely due to difference of the input inductor voltage $u_{a'a}$ for the turn-on periods of T_1 and T_2 (see Fig. 13). The calculation of the voltage waveforms depicted in Fig. 13 is with reference to the voltage envelopes being presented for the passive 12-pulse rectifier [6, eq. (6)–(10)] and neglecting the diode and transistor forward voltage drops and the LIT leakage inductance.

The total losses, the maximum input current ripple, and the system efficiency are detailed in Table III. In summary, the TSHR has advantages over the SSHR concerning switching frequency input current ripple and efficiency and/or input filter and heatsink volume and therefore has to be preferred for high power density applications.

VI. FUTURE WORK

In the next step of the research the thermal behavior of the TSHR will be modeled for large

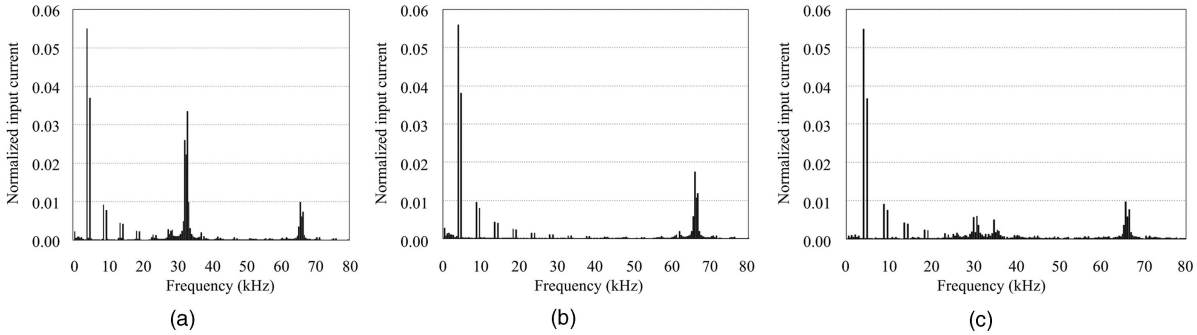

Fig. 12. Digital simulation of input current spectrum of SSHR for switching frequency of f_p = 33 kHz (see (a)) and f_p = 66 kHz (see (b)). Furthermore shown: input current spectrum of TSHR for f_p = 33 kHz (see (c)). Assumed operating conditions: U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW.

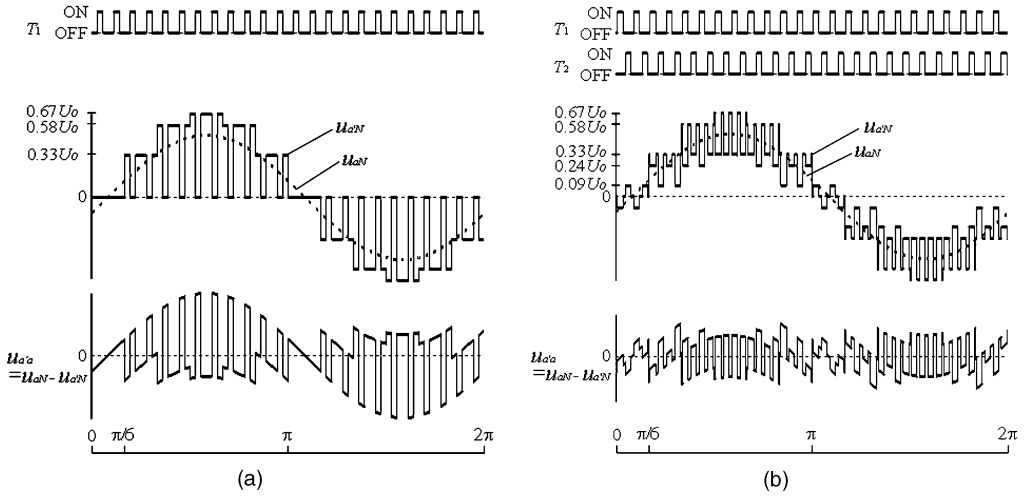

Fig. 13. Calculated time behavior of mains phase voltage u_{aN}, input phase voltage $u_{a'N}$, and input inductor voltage $u_{a'a}$ of SSHR (a) and TSHR (b).

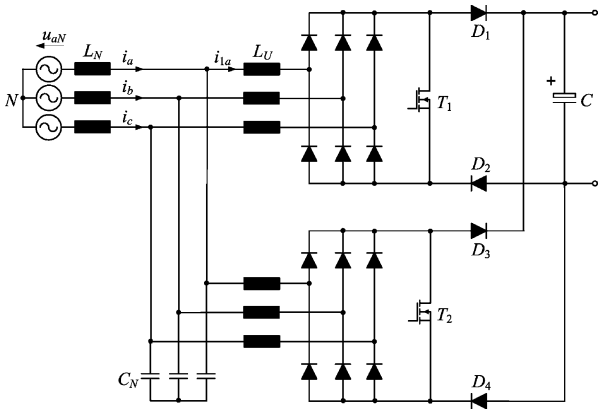

Fig. 14. Parallel connection of two three-phase single-switch discontinuous mode boost rectifiers.

TABLE III
Simulated Maximum Peak-to-Peak Input Current Ripple with Dependency on Switching Frequency and Calculated Total Losses and Efficiency for SSHR and TSHR

System	Max. Input Current Ripple [A]	Total Losses [W]	Efficiency [%]
SSHR f_P = 33 kHz	8.2	502	95.2
f_P = 66 kHz	4.3	548	94.8
TSHR f_P = 33 kHz	2.3	488	95.4

Note: Assumed operating parameters: U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW.

peak to low average load operation as is typical for EHA systems. Furthermore, the TSHR will be evaluated against a parallel connection of two single-switch discontinuous-mode boost-type rectifier systems (TSDCMR, see [10]–[12]) operating in an interleaved manner (see Fig. 14) that shows a comparably low realization and control effort. The results of a first numerical analysis for the TSDCMR are illustrated in Fig. 15 and Fig. 16. The input current spectrum of the TSDCMR exhibits a 5th and 7th harmonic (see Fig. 15(a), Fig. 16) which constitutes a significant drawback as both harmonics should remain below 0.02 p.u. as required by aircraft harmonic standards. In [13], it has been shown for a single-switch discontinuous-mode boost-type rectifier that the magnitudes of 5th and 7th harmonics can be balanced and reduced if a large step-up voltage ratio and a modulated duty cycle are used. Therefore, also for the TSDCMR, even with a modulated duty cycle, the harmonic currents cannot be eliminated. This is in contrast to the TSHR which can be made to have sinusoidal input currents by modulating the duty cycle with a triangular waveform that has a frequency of six times the input voltage frequency. The operating performance of the TSHR with this modified control will be presented in a future publication. A further disadvantage of the TSDCMR is that a multi-stage EMI input filter is required for attenuating the high frequency components of the input current ripple resulting from the discontinuous input current shape (see Fig. 15(b)). The losses of the main power components, the current stresses of the power semiconductors, the measured conducted electromagnetic emissions, and size and weight of the TSDCMR including the EMI will be discussed in detail in a future publication.

VII. CONCLUSIONS

In this paper a novel SSHR and a TSHR system with a regulated output voltage are proposed and comparatively evaluated. Furthermore, results of measurements on a 10 kW prototype of the TSHR are given where the theoretical considerations and a novel control concept ensuring an equal distribution of the input current to the individual TSHR output stages are verified.

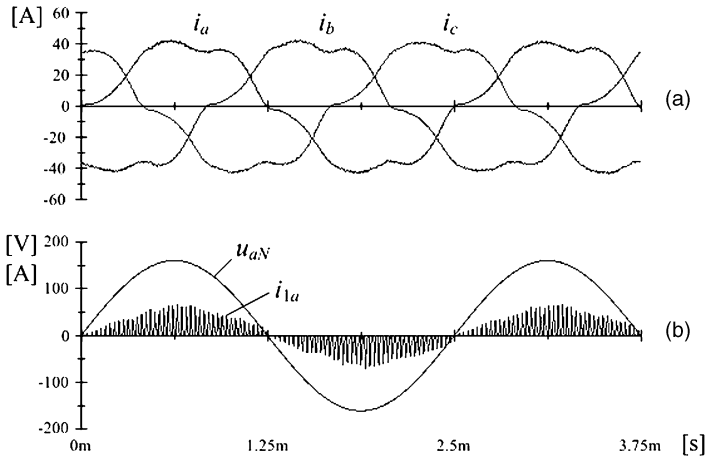

Fig. 15. Simulated time behavior of input phase currents i_a, i_b and i_c (see (a)), input voltage u_{aN} and input current of one bridge i_{1a} (see (b)) of parallel connection of two three-phase single-switch discontinuous mode boost rectifiers operating in interleaved manner (see Fig. 14). Simulation parameters: U_N = 115 V, f_N = 400 Hz, U_O = 350 V, P_O = 10 kW, f_p = 33 kHz with constant duty cycle D = 0.17, L_N = 188 μH, L_U = 15 μH, C_N = 2 μF, and C = 1 mF. For the sake of simplicity only single-stage LC low-pass input filter is considered.

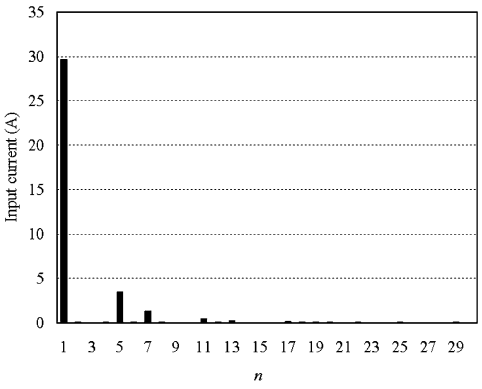

Fig. 16. Simulated input current spectrum (n denotes ordinal number of the harmonics) of parallel connection of two three-phase single-switch discontinuous mode boost rectifiers operating in interleaved manner. Simulation parameters: as for Fig. 15. *Remark:* Lower amplitude of fundamental as compared with measured spectrum of TSHR of equal output power (see Fig. 8) due to neglecting system losses. Amplitude of 5th harmonic of input current could be reduced, but at cost of increased amplitude of 7th harmonic, by varying duty cycle of switches with six times mains frequency. Amplitudes of both harmonics heavily dependent on ratio of output dc voltage and mains voltage amplitude [10].

When a high power density is required, the TSHR has a slight advantage over the SSHR but this is at the cost of a higher realization effort. The prototype of the TSHR shows high efficiency and high power factor over a wide operating range of voltage and frequency. Accordingly, the system is an attractive candidate for future more electric aircraft applications.

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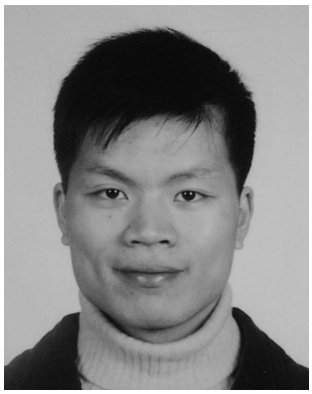
Kazuaki Mino was born in Tokyo, Japan, in 1968. He received the B.E. and M.E. degrees in electronics engineering from Tokyo Denki University, Tokyo, Japan in 1992 and 1994, respectively. Since 2004, he has been a Ph.D. student at Power Electronic Systems Laboratory (PES) in Swiss Federal Institute of Technology (ETH) Zurich.

In 1994, he joined Electronics Technology Laboratory in Fuji Electric Advanced Technology Co. Ltd., Tokyo, Japan. He has been working in the research and development of ac-ac converters (matrix converter, induction heating), PFC circuits and dc-dc converters.

His current research is focused on hybrid 12-pulse rectifier and Electronic Smoothing Inductor for high power density rectifiers. He is a member of the Institute of Electrical Engineers of Japan (IEEJ).



Guanghai Gong was born in Zhejiang, China, on March 23, 1977. He received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, China, in 1999 and 2002, respectively. Since June 1, 2002, he has been a Ph.D. student at Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich.

His research interests include switched-mode power amplifier, soft-switched dc/dc converter, and ac-dc converter for aircraft application.

Johann W. Kolar (M'89–SM'04) studied industrial electronics at the University of Technology Vienna, Austria, where he also received the Ph.D. degree (summa cum laude).

Since 1984 he has been with the University of Technology in Vienna, and has been teaching and working in research in close collaboration with the industry in the fields of high performance drives, high frequency inverter systems for process technology and uninterruptible power supplies. He has proposed numerous novel converter topologies, e.g., the VIENNA Rectifier and the Three-Phase ac-ac Sparse Matrix Converter concept. He has published over 150 scientific papers in international journals and conference proceedings and has filed more than 50 patents. He was appointed professor and head of the Power Electronics Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

Dr. Kolar's current focus of research is on novel ac-ac and ac-dc converter topologies with low effects on the mains, e.g., for power supply of telecommunication systems, more electric aircraft applications and distributed power systems in connection with fuel cells. A further main area of research is the realization of ultra-compact intelligent converter modules employing latest power semiconductor technology (SiC) and novel concepts for cooling and EMI filtering. He is a member of the IEEJ and of the technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 through 2000 he has been serving as an associate editor of the *IEEE Transactions on Industrial Electronics* and since 2001 as an associate editor of *IEEE Transactions on Power Electronics*.