

# Novel Hybrid 12-Pulse Line Interphase Transformer Boost-Type Rectifier with Controlled Output Voltage and Sinusoidal Utility Currents

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A novel injection scheme to improve input current harmonics of hybrid 12-pulse line interphase transformer rectifier with controlled output voltage by two-switch boost-type output stage is presented in this paper. A theoretical derivation of the modulation for achieving purely sinusoidal input currents is introduced. Finally, the proposed scheme is verified by numerical simulations.

**Keywords :** 12-pulse hybrid rectifier, sinusoidal input current, controlled output voltage, aircraft applications.

## 1. Introduction

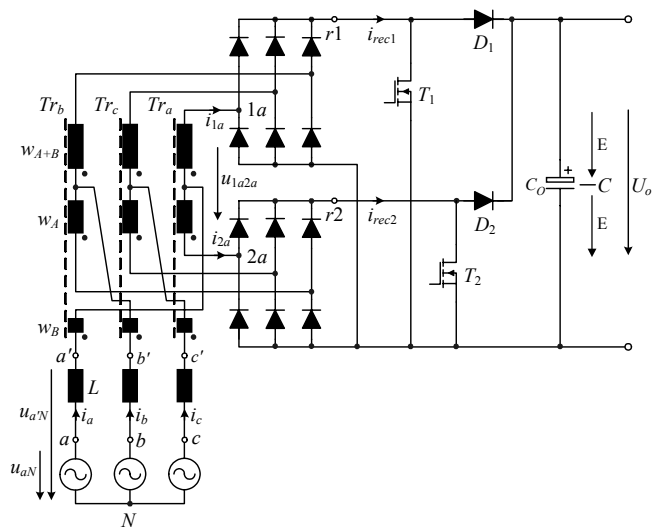
Various 12-pulse passive rectifier concepts which comprise isolated and/or non-isolated phase shifting transformers, diodes, and inductors have been proposed in the literature<sup>(4)</sup>. The passive rectifiers are advantageous concerning efficiency, low complexity, EMC, and reliability. Furthermore, for high input frequency applications like aircrafts and micro turbine systems the magnetic components are showing only a low volume.

For future More-Electric-Aircraft the conventional fly-by-wire hydraulic flight control surface actuation will be partly replaced by power-by-wire electro-hydrostatic actuators (EHAs)<sup>(1)-(3)</sup>. Various rectifier concepts were compared for powering an EHA and it was identified that a passive 12-pulse rectifier system with line interphase transformer (LIT)<sup>(9)(10)</sup> is competitive with an active three-level PWM rectifier concerning efficiency and power density<sup>(6)</sup>. However, a drawback of the passive system is the dependency of the output voltage on the mains voltage level, mains frequency and the output power, especially if voltage and frequency of the power source show large tolerances. In order to avoid this drawback, hybrid 12-pulse rectifiers with controlled output voltage (**Fig.1**) have been proposed<sup>(5)(6)</sup> and analytically and experimentally evaluated<sup>(7)</sup>.

A remaining disadvantage of the proposed hybrid rectifiers compared to active PWM rectifiers is the staircase shape of the input currents which cannot be eliminated by the input EMI filter and results in low frequency mains

current harmonics. Several topologies which can improve the input current quality by current injection have been proposed for multi-pulse rectifiers<sup>(12)-(17)</sup> with impressed DC output current. However, no solution has been proposed so far for voltage-type systems, i.e. for rectifiers with impressed DC output voltage.

In this paper a novel control schemes for improving the input current quality and/or for lowering the amplitudes of low frequency current harmonics of a hybrid voltage-type 12-pulse LIT rectifier is presented. The system is formed by combining a 12-pulse passive rectifier and a DC/DC boost converter which ensures controlled output voltage. In **section 2** theoretical derivation of the optimum functions to achieve purely sinusoidal input current are shown. The proposed control scheme is verified and compared to conventional constant duty cycle control by numerical simulations in **section 3**.



**Fig.1:** Two-switch hybrid 12-pulse LIT rectifier with controlled output voltage.

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## 2. Derivation of the Modulation Functions for Achieving Purely Sinusoidal Input Currents

For passive operation, continuous input current shape and constant output voltage  $U_o$  of the rectifier system the LIT input voltages  $u_{a'N}$ ,  $u_{b'N}$ ,  $u_{c'N}$  are exhibiting a staircase shape. There, the different voltage levels are directly determined by  $U_o$  and the LIT turns ratios. Accordingly, a purely sinusoidal LIT input voltage shape and/or a related space vector

$$\underline{u}' = \hat{u}' (\cos \varphi_N + j \sin \varphi_N) \quad (1)$$

( $\varphi_N = \omega_N t$ , where  $\omega_N$  is the mains angular frequency and  $\varphi_N$  is the phase of the mains current space vector  $\underline{i}_N$ ) could be achieved in the average over a pulse period by proper modulation of the rectifier bridge output voltages  $u_{T1}$  and  $u_{T2}$ . This would result in a purely sinusoidal current drawn from the mains, i.e. the low frequency harmonics of the input current would be eliminated.

For the calculation of the corresponding time behavior of  $u_{T1}$  and  $u_{T2}$  the considerations can be restricted to a  $30^\circ$ -wide interval of the mains period due to the 12-pulse property of the circuit, e.g. only  $\varphi_N = (+15^\circ, -15^\circ)$  is considered in the following. The (purely sinusoidal) mains current  $\underline{i}_N$  is splitted into two current space vectors  $\underline{i}_1$  and  $\underline{i}_2$  which are displaced in phase by  $\pm 15^\circ$  (with reference to  $\underline{i}_N$ ) and are occurring at the LIT outputs. Accordingly, we have for the input voltage space vectors of the diode bridges in the  $\varphi_N$  interval considered

$$\begin{aligned} \underline{u}_1 &= \frac{2}{3} \underline{u}_1 \\ \underline{u}_2 &= \frac{2}{3} \underline{u}_2 \end{aligned} \quad (2)$$

( $i_{1a}, i_{2a} > 0, i_{1b}, i_{2b}, i_{1c}, i_{2c} < 0$ ) where  $u_1$  and  $u_2$  are denominating the local average values of  $u_{T1}$  and  $u_{T2}$ . This results in a LTI input voltage space vector

$$\underline{u}' = \underline{u}_2 - (\underline{u}_2 - \underline{u}_1) \left( \frac{w_A}{2w_A + w_B} \right) + \underline{u}_{wB} \quad (3)$$

( $w_B/w_A = \sqrt{(1-\sqrt{3}/2)} \approx 0.366$ ) where  $\underline{u}_{wB}$  is the space vector of the voltages occurring across the windings  $w_B$  of the LIT which are related to the voltage difference ( $\underline{u}_2 - \underline{u}_1$ ) being present across  $w_A$  and  $w_{A+B}$  by

$$\underline{u}_{wB} = (\underline{u}_2 - \underline{u}_1) \left( \frac{w_B}{2w_A + w_B} \right) e^{j \frac{2\pi}{3}} \quad (4)$$

There, the cyclic changing of the phases has been considered by a phase shift of  $+120^\circ$ . Combining (1)-(4) results in

$$u_1 = \frac{3}{2} \hat{u}' (\cos \varphi_N - (2 + \sqrt{3}) \sin \varphi_N) \quad (5)$$

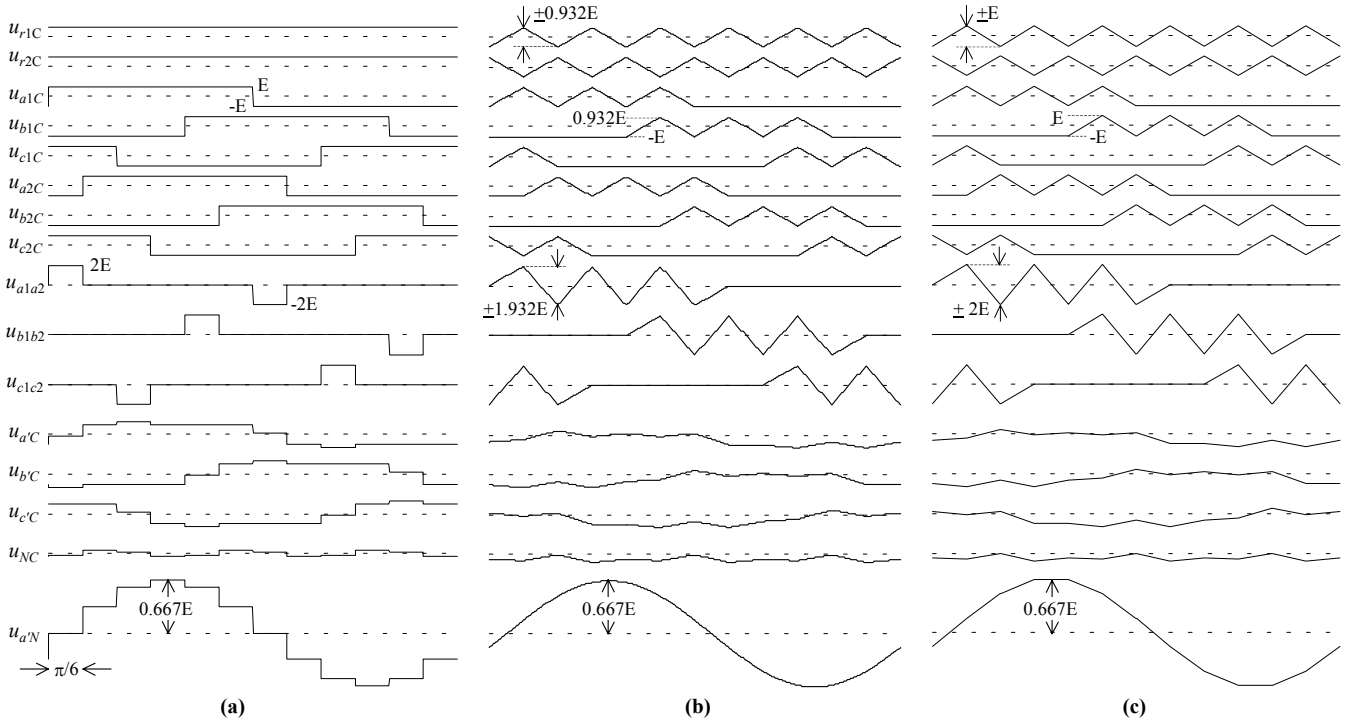
$$u_2 = \frac{3}{2} \hat{u}' (\cos \varphi_N + (2 + \sqrt{3}) \sin \varphi_N)$$

with

$$u_1 = (1 - d_1) U_o \quad (6)$$

$$u_2 = (1 - d_2) U_o$$

( $d_1$  and  $d_2$  are the local duty cycles of the power transistors). As can be seen from a graphical representation of  $u_1$  and  $u_2$  and/or from  $u_{2, \varphi_N = -15^\circ} = u_{1, \varphi_N = +15^\circ} = 0$ ,  $u_{2, \varphi_N = 0^\circ} = u_{1, \varphi_N = 0^\circ} = 1.5 \hat{u}'$ , and  $u_{2, \varphi_N = +15^\circ} = u_{1, \varphi_N = -15^\circ} \approx 2.9 \hat{u}'$  the actual shape of  $u_1$  and  $u_2$  can be approximated linearly with sufficient accuracy using



**Fig.2:** Simulated operating behavior of the voltage-type hybrid 12-pulse rectifier for (a) constant duty cycle, (b) optimum modulation to achieve purely sinusoidal input current, and (c) triangular modulation, i.e. triangular approximation of the optimum modulation functions.

$$u_1 = 3\hat{u}' \left( \frac{1}{2} - \frac{6}{\pi} \varphi_N \right)$$

$$u_1 = 3\hat{u}' \left( \frac{1}{2} + \frac{6}{\pi} \varphi_N \right) \quad (7)$$

what results in a triangular shape of  $u_1$  and  $u_2$  over the mains period ( $u_1$  shows a phase shift of  $180^\circ$  with respect to  $u_2$ ). Considering (8) in section 3.3 and  $\hat{u}' \approx \hat{u}_a$  the global average value of the duty cycle of  $T_1$  and  $T_2$  has to be selected as  $D_{avg}=0.5$  corresponding to an output voltage of  $U_o \approx 3\hat{u}_a$ .

### 3. Numerical simulation

In this section, the proposed modulation scheme is verified by numerical simulations and compared to constant duty cycle operation.

**3.1 Simulated Operating Conditions** For easily generating the modulation functions, triangular waveforms are used in the numerical simulations as approximation of the actual time behavior of the modulation functions. The following parameters are defined with reference to aircraft applications:

Input phase voltage:	$U_N = 115\text{Vrms}$
Input frequency:	$f_N = 400\text{Hz}$
Nominal output power:	$P_O = 10\text{kW}$
Switching frequency:	$f_S = 33\text{kHz}$

**TABLE 1** lists the rectifier circuit parameters. The inductance of the input inductors is selected with respect to the admissible amplitudes of the 11<sup>th</sup> and 13<sup>th</sup> input current harmonics at constant duty cycle or passive operation<sup>(5)(6)</sup> (power transistors  $T_1$  and  $T_2$  remaining in the turn-off state). The switching frequency is defined such that the peak-to-peak input current ripple is kept below 10% of the fundamental current amplitude<sup>(6)(7)</sup>. The turns ratio of the LIT is defined for achieving the necessary  $\pm 15^\circ$  phase shift of  $i_{1a}$  and  $i_{2a}$ . The power transistors  $T_1$  and  $T_2$  are driven in an interleaved manner in order to reduce the switching frequency input current ripple.

The simulation results are shown in **Fig.2** where the local average value of discontinuous quantities is shown instead of the actual shape in order to clearly represent the system operating behavior.

**TABLE 1:** Circuit parameters of the two-switch hybrid 12-pluse LIT rectifier with controlled output voltage.

Component	Symbol	Parameter
Input inductor	$L$	188 $\mu\text{H}$
LIT	$Tr_a, Tr_b, Tr_c$	$w_A/w_B=0.366$
Output capacitor	$C_O$	1mF

**3.2 Comparison of Low-Order Input Current Harmonics** The simulated input current waveforms and the corresponding low-order input current harmonics resulting for constant duty cycle and the variable duty cycle operation are shown in **Fig.3** and **Fig.4**. It has to be noted that the duty cycles of  $T_1$  and  $T_2$  are inverted waveforms of  $u_{r1C}$  and  $u_{r2C}$  (see Fig2(c)) because high (low) duty cycle results in a low (high) local average value of voltage  $u_{r1}$

and/or  $u_{r2}$ .

By employing the 6<sup>th</sup> harmonic modulation, i.e. by triangular shaping of the local average value of the rectifier stage output voltages, the input current waveforms are improved to almost purely sinusoidal shapes (cf. Fig.3 (a) and (b)) and/or the low-order harmonic components are significantly reduced (cf. Fig.4(a) and (b)). The THD of the input current is improved from 6.8% to 0.8%.

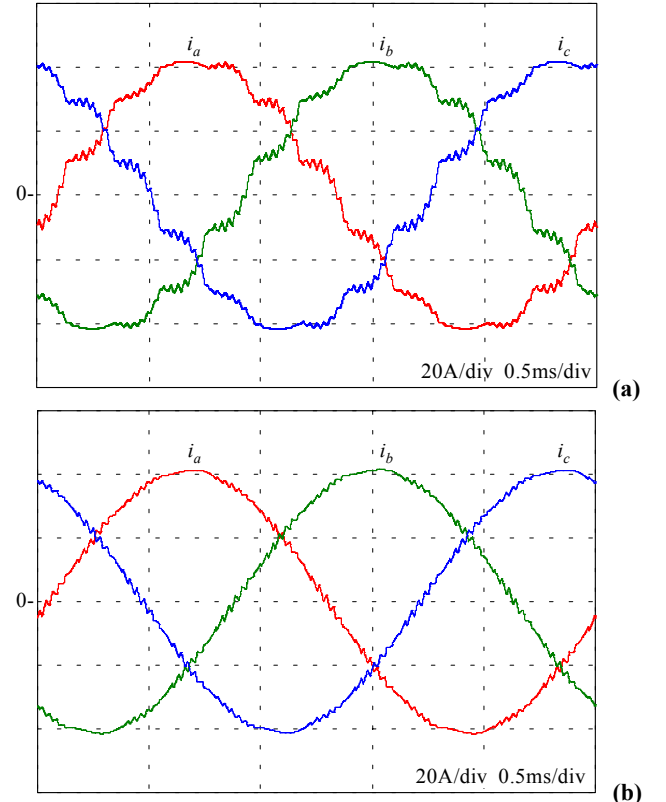
### 3.3 Comparisons of Current and Voltage Stresses

The output currents of the diode bridges  $i_{rec1}$  and  $i_{rec2}$  are depicted in **Fig.5**. The current stresses resulting for the constant duty cycle and the triangular modulation are approximately equal. The selected turns ratio of the LIT results in an equal distribution of the input phase currents, e.g. of  $i_a$  to the inputs of the diode bridges  $i_{1a}$  and  $i_{2a}$  with phase shift of  $\pm 15^\circ$ . Therefore, the improved input current waveforms causes a slight difference of  $i_{rec1}$  and  $i_{rec2}$  waveforms for both control schemes (see Fig5(a) and (b)). However, the varying duty cycles do not cause significant influence on the AC side and rectifier current stresses.

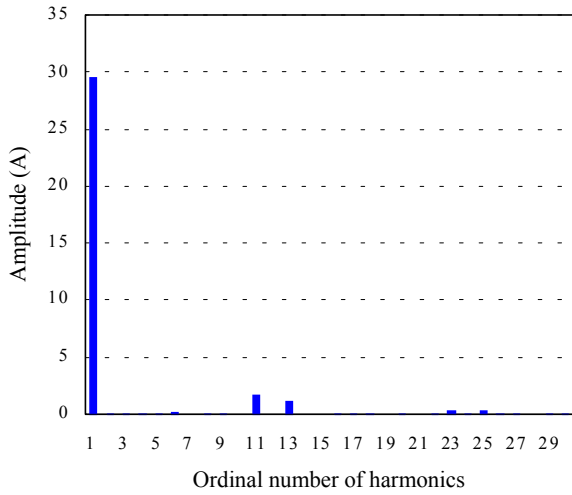
Since the average duty cycle of both control schemes are equal, also the output voltages are equal. The output voltage can be expressed as <sup>(5)(7)</sup>

$$U_o = \frac{1.52\hat{u}_a}{1 - D_{avg}} \quad (8)$$

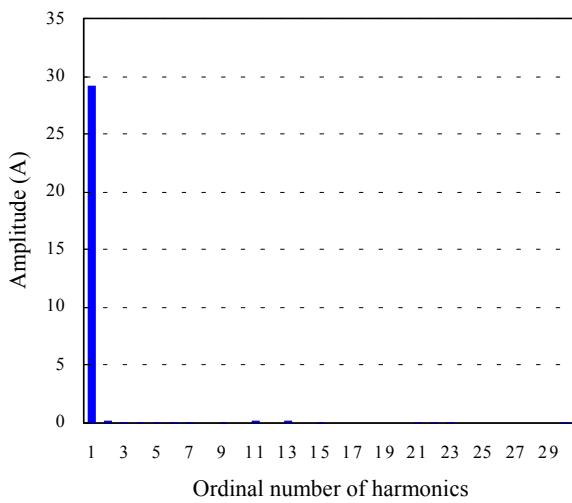
where  $\hat{u}_a$  and  $D_{avg}$  denote the amplitude of input phase



**Fig.3:** Simulated input current waveforms for constant duty cycle control (a) and variable duty cycle control, i.e. triangular shape of the local average value of the rectifier stage output voltages (b) at  $D_{avg}=50\%$ .

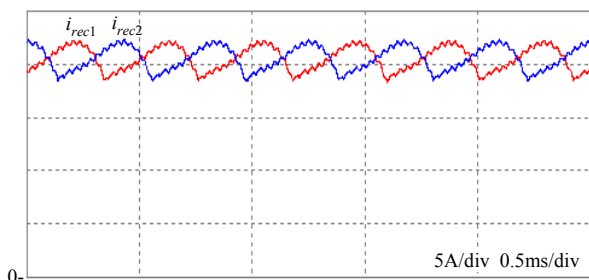


(a)

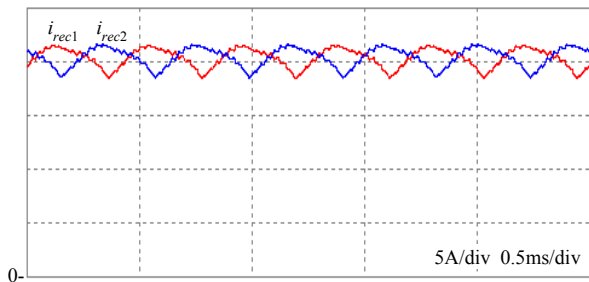


(b)

**Fig.4:** Simulated low-order harmonics of the input current; (a) and (b) as in Fig.3.



(a)



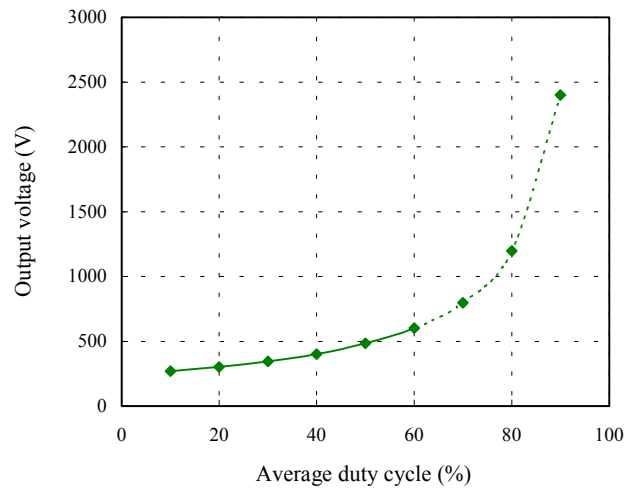
(b)

**Fig.5:** Simulated output currents of the diode bridges of the 12-pulse hybrid rectifier system; (a) and (b) as in Fig.3.

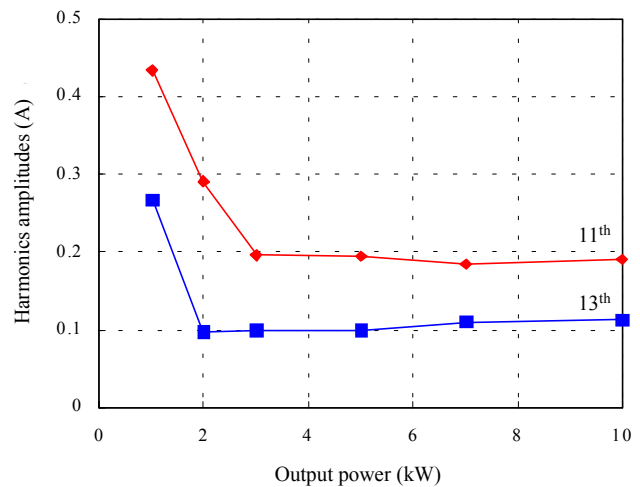
voltage and the average duty cycle. It is noted that the conduction voltage drops on the semiconductors and the inductors are neglected and no leakage inductance is considered and ideal coupling of the LIT windings is assumed. Equation (8) is identical with the simulation result shown in Fig.6 and valid for both control schemes. The resulting output voltage immediately determines the blocking voltage stress on the power semiconductors.

### 3.4 Dependency of Input Current Harmonics and Output Voltage on Output Power and Average Duty Cycle

The simulated dependency of the amplitude of the 11<sup>th</sup> and 13<sup>th</sup> input current harmonic on the output power is depicted in Fig.7. The 11<sup>th</sup> and 13<sup>th</sup> input current harmonics increase in the range of low output power ( $P_o < 3\text{kW}$ ). In this output power range the input currents to the diode bridges are discontinuous, which causes a low-frequency distortion of phase voltages at the input of the LTI (e.g. of



**Fig.6:** Simulated output voltage resulting in dependency on average duty cycle for 10kW output power.



**Fig.7:** Simulated amplitudes of the 11<sup>th</sup> and 13<sup>th</sup> input current harmonics in dependency on the output power for modulating the duty cycle with six times the input frequency; average duty cycle  $D_{avg} = 50\%$ .

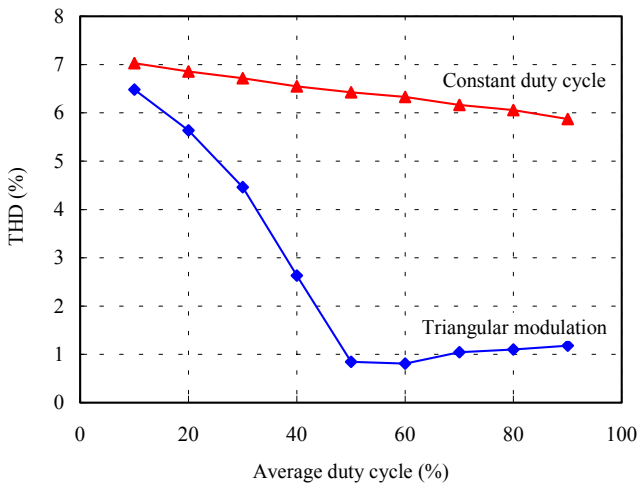
voltage  $u_{a'n}$ ). However, the proposed control scheme ensures low 11<sup>th</sup> and 13<sup>th</sup> input current harmonics within a wide operating power range.

The dependency of the THD on the average duty cycle is illustrated in Fig.8. The average duty cycle of the optimum modulation, which varies from 0 to 100%, is 50%. Since the modulation and/or duty cycle range is 0 to 100% the optimum modulation to improve the input current can only be realized for  $D_{avg}=50\%$ . For  $D_{avg}<50\%$  the duty cycle variation is within the range 0 to  $2D_{avg}$  and from  $2D_{avg}-100\%$  to 100% within the range  $D_{avg}>50\%$ . Despite this a low THD is achieved within the whole operating range as compared to constant duty cycle control (see Fig.8). The THD in the range  $D_{avg}>50\%$  is lower compared to the range  $D_{avg}<50\%$  due to the high output voltage.

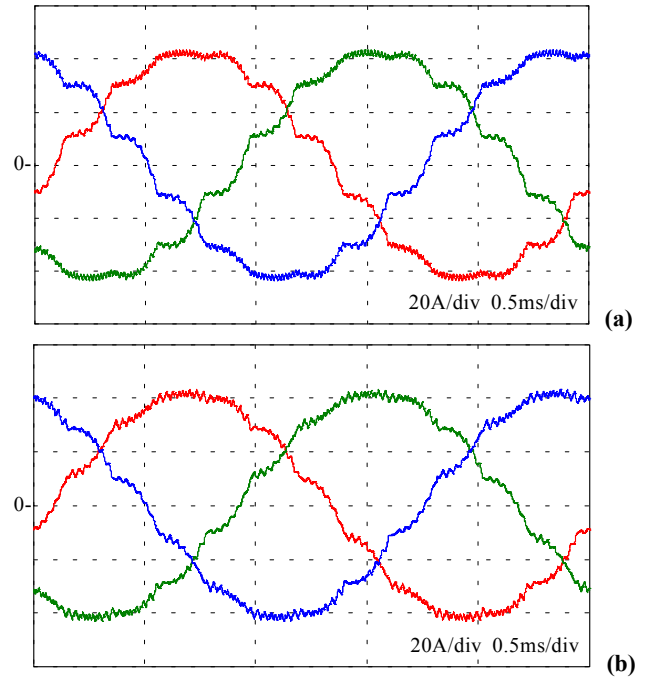
**3.5 Comparisons of High-Order Input Current Harmonics and Output Voltage Ripple** For  $D_{avg}=50\%$  the output voltage is around 480V<sub>dc</sub>. Therefore, for employing 600V power semiconductors the voltage margin would not be sufficient, especially if input voltage tolerances would be considered.

With respect to future more electronic aircraft applications the output voltage has to be set to 350Vdc<sup>(5)(7)</sup> and/or  $D_{avg}=30\%$  has to be selected. The input current waveforms and the current spectrum for  $D_{avg}=30\%$  are shown in Fig.9 and Fig.10 respectively. The switching frequency current ripple resulting for constant duty cycle operation is relatively low due to the interleaved switching of  $T_1$  and  $T_2$ <sup>(5)(7)</sup>. The switching frequency current ripple resulting for triangular modulation is higher due to the different duty cycles of  $T_1$  and  $T_2$  what makes the interleaving less effective.

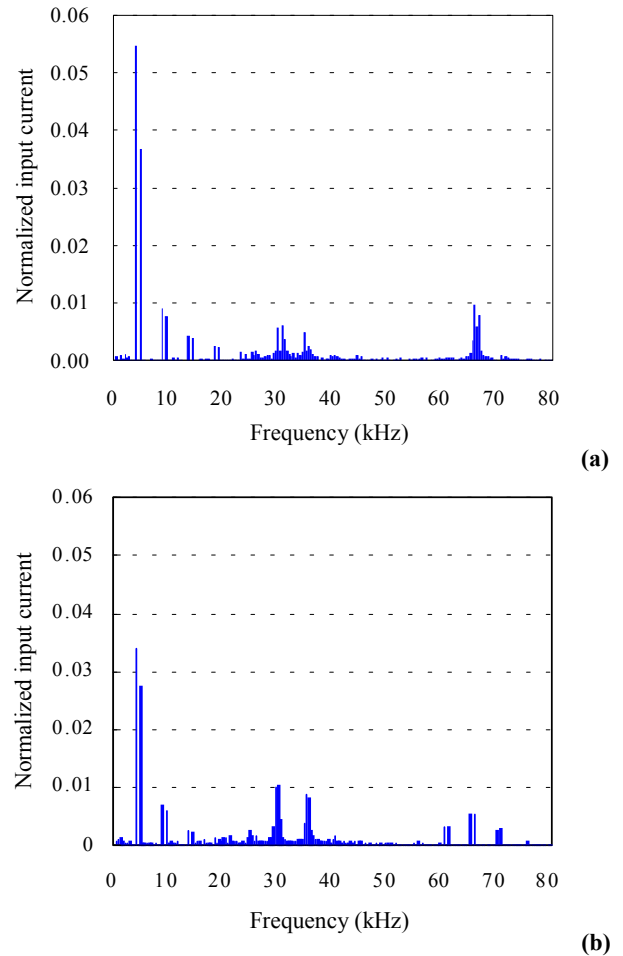
In case of  $D_{avg}=50\%$  with triangular modulation, the switching frequency current ripple is lower compared to constant duty cycle operation (cf. Fig.11 (a) and (b)) because  $T_1$  and  $T_2$  are alternatively turned on in both control schemes and the pulse width of the gate signals with the



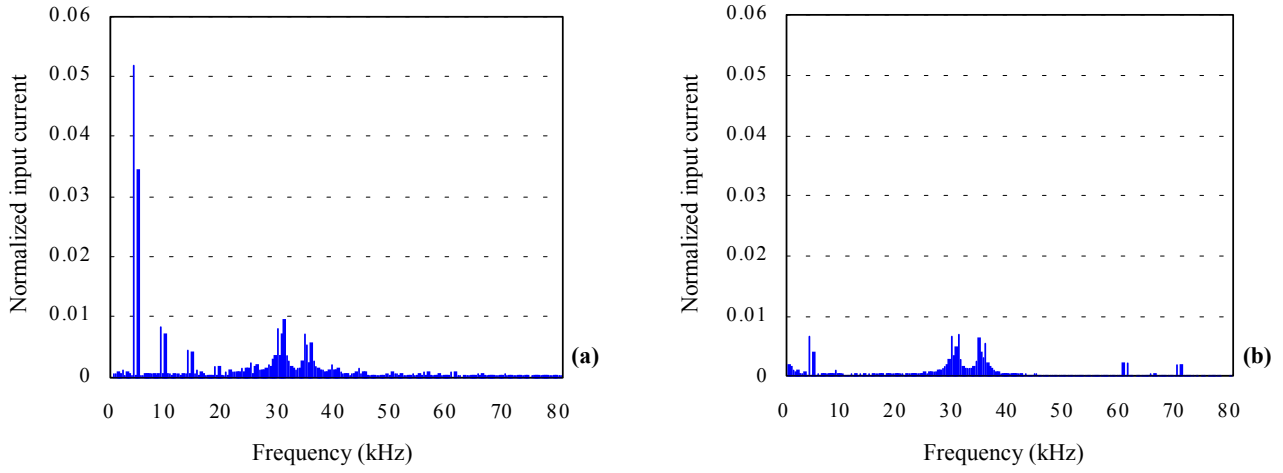
**Fig.8:** Simulated dependency of the THD on the average duty cycle for constant duty cycle (equal to the average duty cycle) and variable duty cycle according to triangular shape of the local average value of the rectifier stage output voltages (cf. Fig.2); output power: 10kW.



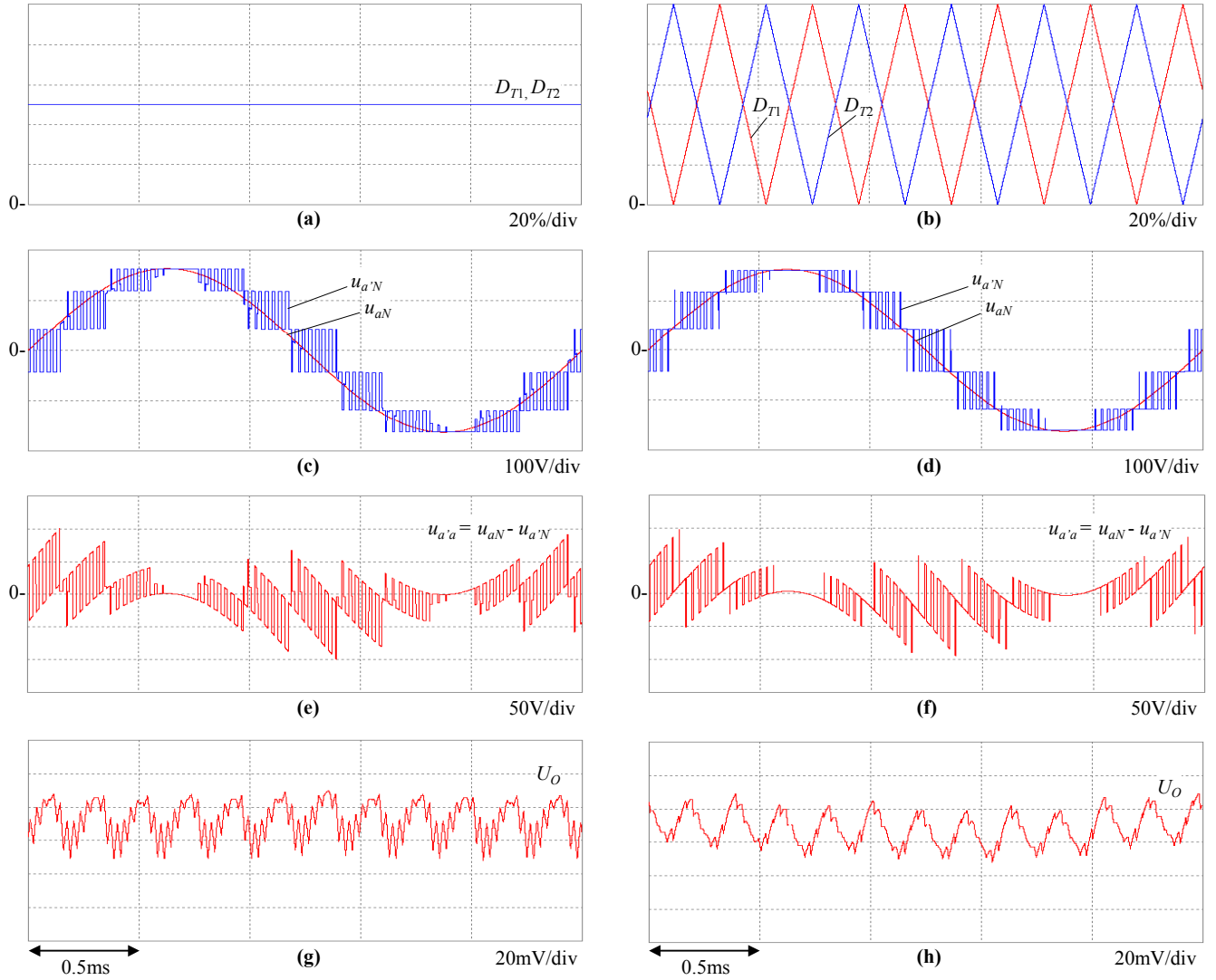
**Fig.9:** Simulated input current waveforms for constant duty cycle (a) and triangular modulation and/or variable duty cycle (b) at average duty cycle  $D_{avg}=30\%$ .



**Fig.10:** Simulated input current spectrum; (a) and (b) as for Fig.9.



**Fig.11:** Simulated high-order harmonics of the input current for constant duty cycle **(a)** and variable duty cycle / triangular modulation **(b)** at  $D_{avg}=50\%$ .



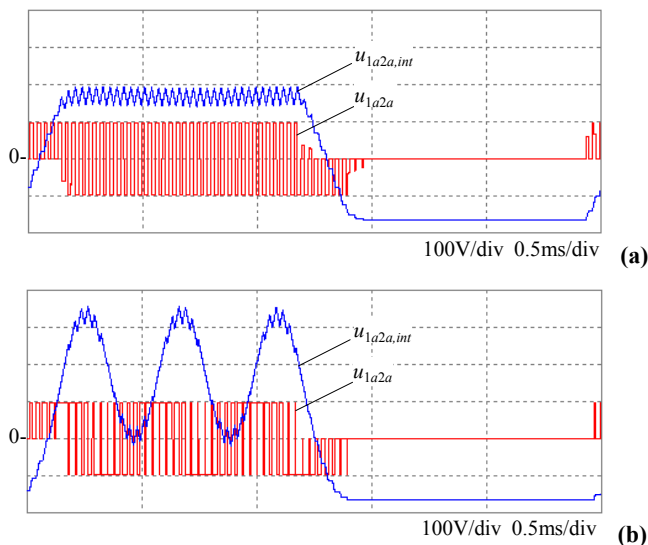
**Fig.12:** Simulated operating behavior for constant duty cycles  $D_{T1}$  and  $D_{T2}$  **(a)**, **(c)**, **(e)**, and **(g)** and variable duty cycles  $D_{T1}$  and  $D_{T2}$  and/or triangular modulation **(b)**, **(d)**, **(f)**, and **(h)**; **(c)**, **(d)**: input phase voltage  $u_{aN}$  and corresponding input phase voltage  $u_{a'N}$  between  $N$  and  $a'$ ; **(e)**, **(f)**: input inductor voltage  $u_{a'a}$ ; **(g)**, **(h)**: output voltage  $U_O$ ; Simulation condition:  $D_{avg}=50\%$  and 10kW output power.

triangular modulation can gradually change. **Fig.12** shows characteristic voltage shapes for constant duty cycle (a) and the triangular modulation (b). The amplitude of each generated voltage is theoretically equal. However, the pulse width of the inductor voltage  $u_{a'a}$  for triangular modulation is smaller compared to the case of constant duty cycle when high amplitude of  $u_{a'a}$  are generated (cf. Fig.12(e) and (f)). This causes lower switching frequency current ripple and lower output voltage  $U_O$  of high frequency components (cf. Fig.12(g) and (h)). It is noted that the phase angle and the frequency of the modulation should be adjusted and synchronized to the input current. Any difference in phase angle or frequency would cause low frequency output voltage ripple.

**3.6 Comparison of Magnet Components** The LIT voltage  $u_{1a2a}$  and the integrated LIT voltage  $u_{1a2a,int}$  are depicted in **Fig.13**.  $u_{1a2a}$  and  $u_{1a2a,int}$  are varying over a half output period<sup>(7)</sup>. As compared to the constant duty cycle control, the peak amplitude of  $u_{1a2a,int}$  resulting for triangular modulation is two times higher (cf. Fig.13(a) and (b)). Furthermore,  $u_{1a2a,int}$  oscillates with the frequency of the triangular modulation, i.e. with six times the mains period within a  $150^\circ$ -wide interval. This causes higher maximum flux density, volume, and core loss of the LIT. On the other hand, the inductance of the input inductors which is selected for compliance to limits given for the amplitudes of the 11<sup>th</sup> and 13<sup>th</sup> current harmonics<sup>(5)(6)</sup> can be significantly reduced for the proposed modulation scheme. E.g., for  $D_{avg}=30\%$  the inductance could be reduced from  $188\mu\text{H}$  to  $55\mu\text{H}$  for same low-order input current harmonics what results in a significant reduction of the inductor weight and volume.

#### 4. Conclusions

A novel 6<sup>th</sup> harmonic modulation scheme for hybrid 12-pulse voltage-type line interphase transformer (LIT)



**Fig.13:** Simulated LIT voltage  $u_{1a2a}$  and integrated voltage  $u_{1a2a,int}$  of  $u_{1a2a}$  for constant duty cycle (a) and variable duty cycle / triangular modulation (b) at  $D_{avg}=50\%$ .

rectifiers has been proposed in this paper. The optimum function for achieving purely sinusoidal input currents is theoretically derived. The circuit operation and performance for the proposed control scheme are analyzed and compared to constant duty cycle control by the numerical simulations. This shows that low-order input current harmonics can be significantly reduced. By applying the proposed modulation scheme, the volume of the LIT will be increased compared to the conventional constant duty cycle scheme. However, the inductance and volume of the input inductors can be significantly reduced. This leaves room for a minimization of the overall system volume and/or efficiency. In summary, almost purely sinusoidal input currents can be realized using the proposed control scheme without increasing the number of the main components.

In further work the proposed control scheme will be evaluated experimentally for a 10kW prototype of the hybrid rectifier. Furthermore, the application of a modulation of the output quantity of the rectifier stages will be studied also for current-type multi-pulse passive rectifier systems.

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