Novel Hybrid 12-Pulse Line Interphase Transformer Boost-Type Rectifier with Controlled Output Voltage

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***Abstract*—This paper describes two novel hybrid 12-pulse line interphase transformer rectifier systems with integrated single-switch or two-switch boost-type output stage. The boost stage allows to control the output voltage to a constant value independent of line voltage or output power variations. In combination with low complexity and/or high reliability the hybrid rectifier concept therefore is of potential interest for supplying electrically powered actuators of future More-Electric-Aircrafts. The principle of operation and the dimensioning of the systems are discussed. Furthermore, a control concept guaranteeing a symmetric distribution of the load current to the individual systems of the two-switch topology is proposed. The theoretical considerations are experimentally confirmed for a 10kW laboratory prototype. Finally, the single- and the two-switch system are comparatively evaluated concerning input current ripple, power factor, and overall efficiency.**

Keywords: 12-pulse hybrid rectifier; more-electric-aircraft

I INTRODUCTION

For future More-Electric-Aircrafts the conventional fly-by-wire hydraulic flight control surface will be partly replaced by power-by-wire electro-hydrostatic actuators (EHA) showing lower maintenance effort, higher efficiency, and larger fault tolerance. There, variable speed electric motors fed by inverter systems are driving dedicated hydraulic pumps which are locally providing the hydraulic power to the actuators. For supplying an inverter DC voltage link from the three-phase variable frequency and variable voltage aircraft electrical system, AC/DC converters with low effects on the mains are employed [1-4].

In [4] rectifier concepts have been compared for powering a EHA where a passive 12-pulse rectifier system with line interphase transformer (LIT) was identified as competitive to active three-level PWM rectifier concepts concerning efficiency and power density. However, a remaining drawback of the passive system is the dependency of the output voltage on the mains voltage level, the mains frequency and the output power, especially if voltage and frequency aircraft power system are varying in a wide range. Therefore, an extension of the passive 12-pulse LIT rectifier to controlled output voltage was described in [4, 8].

In this paper, the hybrid 12-pulse LIT boost-type rectifier systems proposed in [4,8], i.e. the single-switch hybrid 12-pulse line interphase transformer rectifier (SSHR, cf. **Fig.1**(a)) and the two-switch hybrid 12-pulse line interphase transformer rectifier (TSHR, cf. Fig.1(b)) are analyzed in detail. In **Section II** the principle of operation of the SSHR and the TSHR is analyzed and shown by digital simulations. The dimensioning of the systems and the distribution of the losses to the main active and passive components is discussed in **Section III.** Furthermore, a low-cost zero sequence current control scheme ensuring an equal partitioning of the load to the individual systems of the TSHR is proposed. Results of an experimental analysis of the TSHR are given in **section IV**. In **section V** the SSHR and the

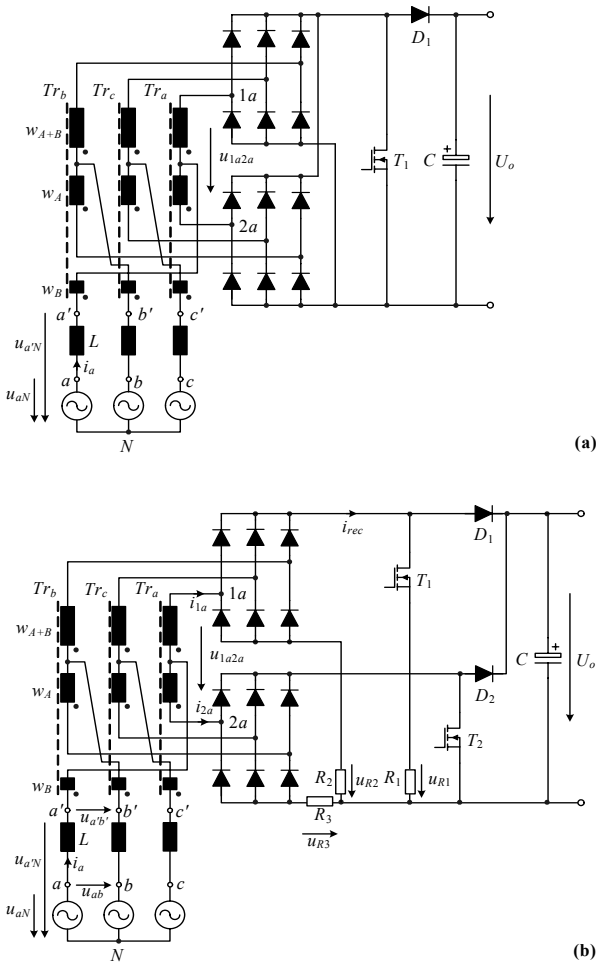

Fig.1: Proposed three-phase hybrid 12-pulse boost-type rectifier systems **(a)** single-switch topology (SSHR); **(b)** two-switch topology (TSHR).

TSHR are comparatively evaluated concerning mains behaviour and efficiency.

For all further considerations in this paper, the following input voltage and input frequency range is assumed:

$$U_N = 96\text{V}_{\text{rms}} \ldots 132\text{V}_{\text{rms}}$$
$$f_N = 400\text{Hz} \ldots 800\text{Hz}.$$

There, the nominal values are $U_{N,r} = 115\text{V}_{\text{rms}}$ and $f_{N,r} = 400\text{Hz}$; furthermore,

$$P_{O,r} = 10\text{kW}$$

is defined as rated output power.

II Basic Principle of Operation

In the following the basic principle of operation of the SSHR and the TSHR is shown by results of digital simulations.

A Single-switch hybrid 12-pulse line interphase transformer rectifier

The topology of the SSHR (cf. Fig.1(a)) integrates a single-switch boost converter and a 12-pulse rectifier stage in order to achieve a controllability of the output voltage. The output voltage of the system can be derived as [5,8]

$$U_o = \frac{1.52\hat{u}_a}{1 - D_{u1}}. \qquad (1)$$

where, $\hat{u}_a$ is the amplitude of the mains phase voltage and D_{u1} denotes the duty cycle of the power transistor T_1.

In **Fig.2**(a), the results of a numerical simulation of the system input phase currents are shown. The mains phase voltage u_{aN} and the corresponding input phase voltage $u_{a'N}$ between a' and N are depicted in Fig.2(b). The mains phase voltage u_{aN} and the corresponding LIT voltage u_{1a2a} between $1a$ and $2a$ are shown in Fig.2(c). The voltages $u_{a'N}$ and u_{1a2a} exhibit the typical shapes of a passive 12-pulse rectifier [5, 8] but are chopped with switching frequency.

B Two-switch hybrid 12-pulse line interphase transformer rectifier

1) Basic principle of operation

The topology of the TSHR is depicted in Fig.1(b) where the power transistors T_1 and T_2 are operating with equal duty cycles in interleaved manner in order to reduce the switching frequency ripple of the input currents.

The output voltage U_o of the system can be obtained in analogy to (1) as [5,8]

$$U_o = \frac{1.52\hat{u}_a}{1 - D_{u2}} \qquad (2)$$

where D_{u2} is the duty cycle of the power transistors T_1 and T_2.

Fig.3 shows the results of a digital simulation of the system. The input phase currents i_a, i_b, i_c are depicted in Fig.3(a); characteristic voltages, i.e. the mains phase voltage u_{aN} and the corresponding input phase voltage $u_{a'N}$ and the LIT voltage u_{1a2a} are shown in Figs.3(b) and (c).

As compared to the SSHR (cf. Fig.2(a)) the switching frequency input current ripple amplitude is considerably reduced due to the (partial) cancellation of the harmonics of $u_{a'N}$. On the other hand, the LIT

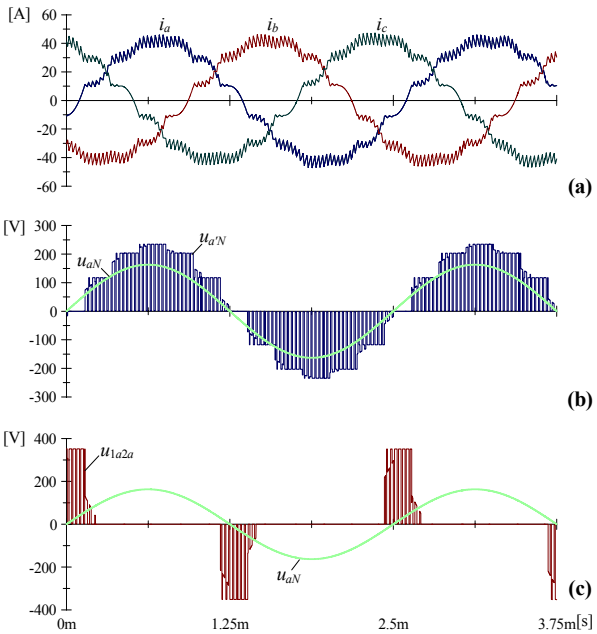

Fig.2: Simulation of the SSHR (cf. Fig.1(a)); **(a)** time behavior of the input phase currents i_a, i_b and i_c; **(b)** mains phase voltage u_{aN} and corresponding current forming input phase voltage $u_{a'N}$.; **(c)** mains phase voltage u_{aN} and corresponding LIT voltage u_{1a2a}. Simulation parameters: U_N=115V$_{\text{rms}}$, f_N=400Hz; U_O=350V, P_O=10kW, switching frequency f_P=33kHz, D_{u1}=0.3.

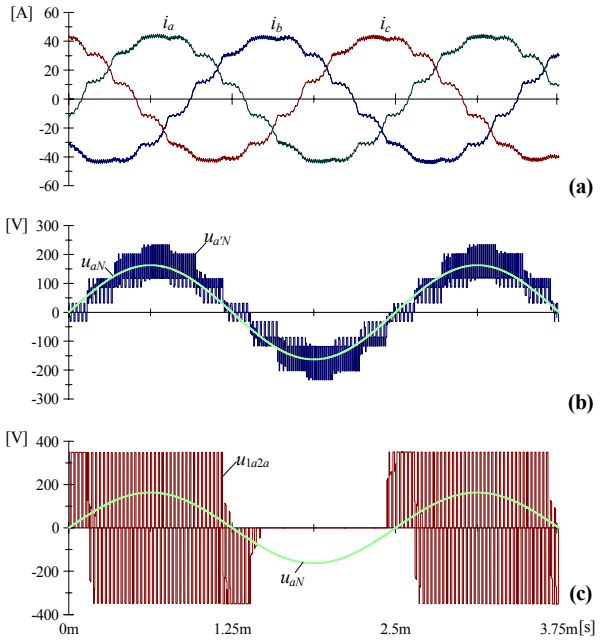

Fig.3: Simulation of the TSHR (cf. Fig.1(b)); **(a)** time behavior of input phase currents i_a, i_b and i_c; **(b)** mains phase voltage u_{aN} and corresponding current forming input phase voltage $u_{a'N}$; **(c)** mains phase voltage u_{aN} and corresponding LIT voltage u_{1a2a}. Simulation parameters as for Fig.2, D_{u2}=0.3.

voltage u_{1a2a} (cf. Fig.3(c)) being chopped with switching frequency now extends over a half mains period what results in increased LIT iron losses.

2) Control of zero sequence current

A slight difference of the duty cycles of the power transistors T_1 and T_2 would result in a zero sequence current flowing between the two rectifier bridges via the LIT. Accordingly, the currents in the two partial systems would not be balanced what would cause higher current stresses on the power components and a low frequency distortion of the input phase currents.

Therefore, a zero sequence current control ensuring an equal current partitioning has to be employed. There, the simplest way is to directly measure the zero sequence current i_0, i.e. the sum of the input phase currents of diode bridge 1 or diode bridge 2, $i_0=1/3(i_{1a}+i_{1b}+i_{1c})=-1/3(i_{2a}+i_{2b}+i_{2c})$, using a through-hole current transducer and to adjust the duty cycles by negative feedback in order to eliminate i_0.

Alternatively, a zero sequence current control according to **Fig.4** could be implemented which allows to detect i_0 at lower costs based on a current measurement with shunt resistors (cf. Fig.1(b)). Corresponding key waveforms are depicted in **Fig.5**. When the voltages u_{R1} and u_{R2} across the shunt resistors R_1 and R_2 are identical within the turn-on period of the MOSFET T_1, no zero sequence current i_0 is present in the system.

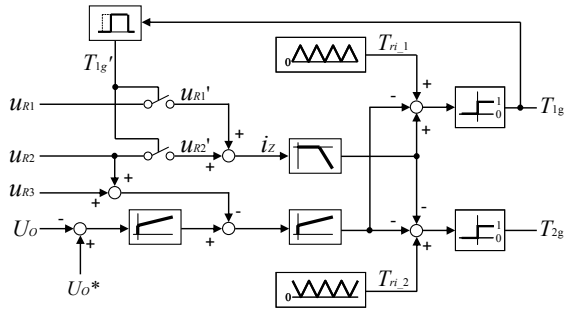

Fig.4: Block diagram of the TSHR control comprising a zero sequence current control based on current measurement by shunt resistors (cf. Fig.1(b)).

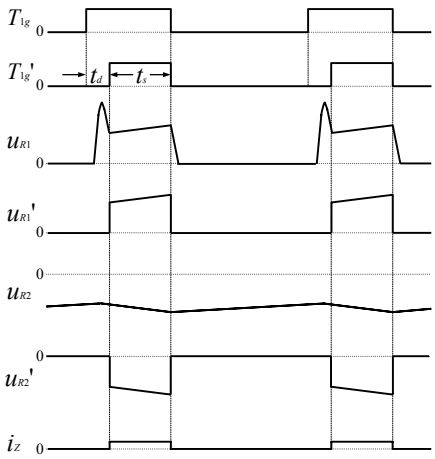

Fig.5: Time behavior of key waveforms of the TSHR zero sequence current control according to Fig.4.

Accordingly, i_0 can be detected as difference of u_{R1} and u_{R2}. In the control circuit the shunt voltages u_{R1} and u_{R2} are added in a period t_s which is generated from the gate signal T_{g1} of T_1 considering a delay time t_d in order to avoid the detection of a large current peak resulting from the reverse recovery of diode D_1. For positive average value of signal i_Z, a zero sequence current is flowing in T_1 from drain to source. In this case the control circuit reduces the duty cycle of T_1 and increases the duty cycle of T_2 what generates a zero sequence voltage component between the inputs of diode bridges reducing the zero sequence current.

Remark: Alternative to providing a control loop, the occurrence of a zero sequence current i_0 also could be prevented by two additional diodes decoupling the boost output stages like shown in Fig.14 for two parallel connected three-phase single-switch discontinuous mode rectifiers. Due to the higher conduction losses and the higher realization effort this concept has not been analyzed in more detail in this paper.

III SYTEM DIMENSIONING

The input inductors (L=188µH) of the rectifiers have to be designed with respect to the admissible amplitude of the 11th and 13th harmonic of the input current [4, 8]. The switching frequency of the TSHR is selected as f_P=33kHz, in order to keep a peak-to-peak input current ripple lower than 10% of the fundamental current amplitude. For achieving the necessary $\pm 15^o$ phase shift of corresponding input phase currents of diode bridge 1 and 2 (e.g. of i_{1a} and i_{2a}) an LIT turns ratio of

$$W_B/W_A = 0.366 \tag{3}$$

is required [6]. We then have for the amplitudes of the fundamentals of i_{1a} and i_{2a} [6]

$$\hat{i}_{1a} = \hat{i}_{2a} = 0.518\hat{i}_a\,. \tag{4}$$

As compared to the SSHR, for the TSHR the current stresses on the boost stage power semiconductors (T_1, T_2 and D_1, D_2) are advantageously cut in half. The dependency of the measured switching loss characteristics resulting for employing a CoolMOS power transistor (600V/47A, SPW47N60C3, Infineon) in combination with an ultra fast recovery diode (600V/30A, DSPEP 30-60BR, IXYS) is depicted in **Fig.6**. According to Fig.6 the power transistor switching losses can be calculated as

$$P_S = f_P(k_1 I^2_{rec,rms} + k_2 I_{rec,avg}) \tag{5}$$

(cf. [9]) where $I_{rec,rms}$ and $I_{rec,avg}$ are denoting the RMS and the average value of the output current of one diode bridge. Assuming in a first approximation a continuous sinusoidal shape of the diode bridge input phase currents [6], we have for $I_{\mathrm{rec},rms}$ and $I_{\mathrm{rec},avg}$

$$I_{rec,rms} = \hat{i}_{1a}\left(\frac{3}{\pi}\int_{\pi/3}^{2\pi/3}\sin^2 t\,dt\right)^{\frac{1}{2}} = 0.956\hat{i}_{1a} \tag{6}$$

$$I_{rec,avg} = \frac{3\hat{i}_{1a}}{\pi}\int_{\pi/3}^{2\pi/3}\sin t\,dt = 0.955\hat{i}_{1a}\,, \tag{7}$$

and, according to Fig.6, for the transistor turn-on losses k_1=0.4943µWs/A^2, k_2=13.33µWs/A and for the transistor turn-off losses k_1=0.6114µWs/A^2, k_2= 1.469µWs/A; the diode reverse recovery losses are characterized by k_1=0.1486µWs/A^2 and k_2= 4.789µWs/A.

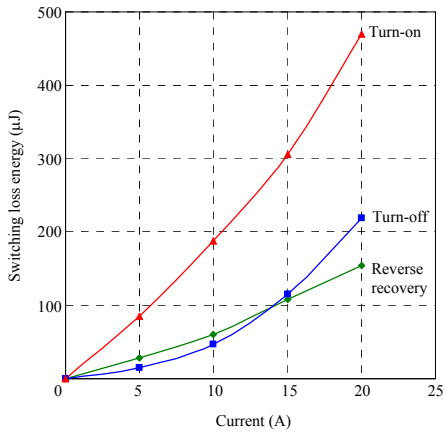

Fig. 6: Dependency of the switching losses of a CoolMOS power transistor (600V/47A, SPW47N60C3, Infineon) in combination with an ultra fast recovery diode (600V/30A, DSPEP 30-60BR, IXYS). Parameters: Switching voltage U_O=350V, turn-on gate resistor $R_{g(on)}$=5Ω, turn-off gate resistor $R_{g(off)}$=2.5Ω.

The conduction losses of the power transistors and the diodes can be calculated as

$$P_{con,T1} = I^2_{rec,rms} R_{ON} D_{u2} \tag{8}$$

and

$$P_{con,D1} = U_F I_{rec,ave} (1 - D_{u2}) . \tag{9}$$

With reference to the data sheet we have for the power MOSFET (SPW47N60C3) R_{ON}=0.133Ω and for the diode (DSPEP 30-60BR) U_F=1.75V at a junction temperature of 125°C. The maximum RMS input current occurs at U_N=96V, f_N=800Hz, and P_O=10kW where the efficiency is 90% considering the power losses in the active part and the phase displacement φ of mains current fundamental and the mains voltage (cosφ=0.837, cf. Fig.5, 6 in [8]).

The calculated maximum losses in the active part of the TSHR are listed in **TABLE I**. There, the maximum temperature difference of MOSFET junction and case is 34.8°C and for the power diodes 42.9°C what is admissible for a heat sink temperature of 85°C.

TABLE I - Maximum Losses of the TSHR boost stage power semiconductors occurring for U_N =96V, f_N=800Hz, U_O=350V, P_O=10kW, f_P=33kHz.

MOSFET	Conduction losses	67W	116W
	Turn-on losses	30W	
	Turn-off losses	19W	
Diode	Conduction losses	29W	39W
	Reverse recovery losses	10W	
Total power semiconductor losses			310W

In the SSHR, the two power MOSFETs and the two diodes are connected in parallel to accommodate the higher current stresses. Therefore, both systems show equal realization effort concerning the power semiconductors. The main components of the TSHR are listed in **TABLE II** and a 10kW TSHR laboratory prototype is shown in **Fig 7**.

TABLE II - List of components employed in the TSHR.

Component	Symbol	Type
Input inductors	L	Value: 188µH Core: S3U 48b Material: Trafoperm N2/0.1mm
Input transformer	Tr_a, Tr_b, Tr_b	W_A: 21 turns, W_B: 8 turns Value: L_{WA+B} = 66mH, L_{WA} = 35.4mH, L_{WB} = 4.74mH Core: 2 × SM 65 Material: Trafoperm N2/0.1mm
Diode bridge		2 × VUE 35-06NO7, IXYS
MOSFET	T_1, T_2	600V/47A, SPW47N60C3, Infineon
Output diode	D_1, D_2	600V/30A, DSPEP 30-60BR, IXYS
Output capacitor	C	2 × 560µF/400 VDC, Rubycon

Fig.7: Prototype of a 10kW TSHR; overall dimensions: 24.0×22.9×11.7cm^3

IV Experimental Analysis

A 10kW prototype of the TSHR has been developed for verifying the theoretical analysis. The input current waveforms, the zero sequence current time behaviour and the input current spectrums are shown in **Fig.8**. The measured waveforms are in good correspondence with the simulation results and the zero sequence current is successfully controlled by the proposed method as shown in Fig.8(c). The system behaviour for employing a zero sequence current control relying on a current transducer is depicted in Figs.8(b) and (e). For both concepts the zero sequence current is eliminated and the input currents shows about equal THD values (cf. Fig.8(e) and Fig.8(f)). In case no zero sequence current control would be provided a low frequency distortion of the input current would occur.

The measured input inductor voltage and the LIT voltage of the TSHR (cf. **Fig.9**) are again in close correspondence to the simulated waveforms (cf. Figs.3(b) and (c)). The efficiency η and the power factor λ of the TSHR are depicted in **Fig.10** in dependency on the output power. For the nominal operating point (U_N=115V, f_N=400Hz, U_O=350V, P_O=10kW) we have η=95.0% and λ=0.95. The output voltage is controlled

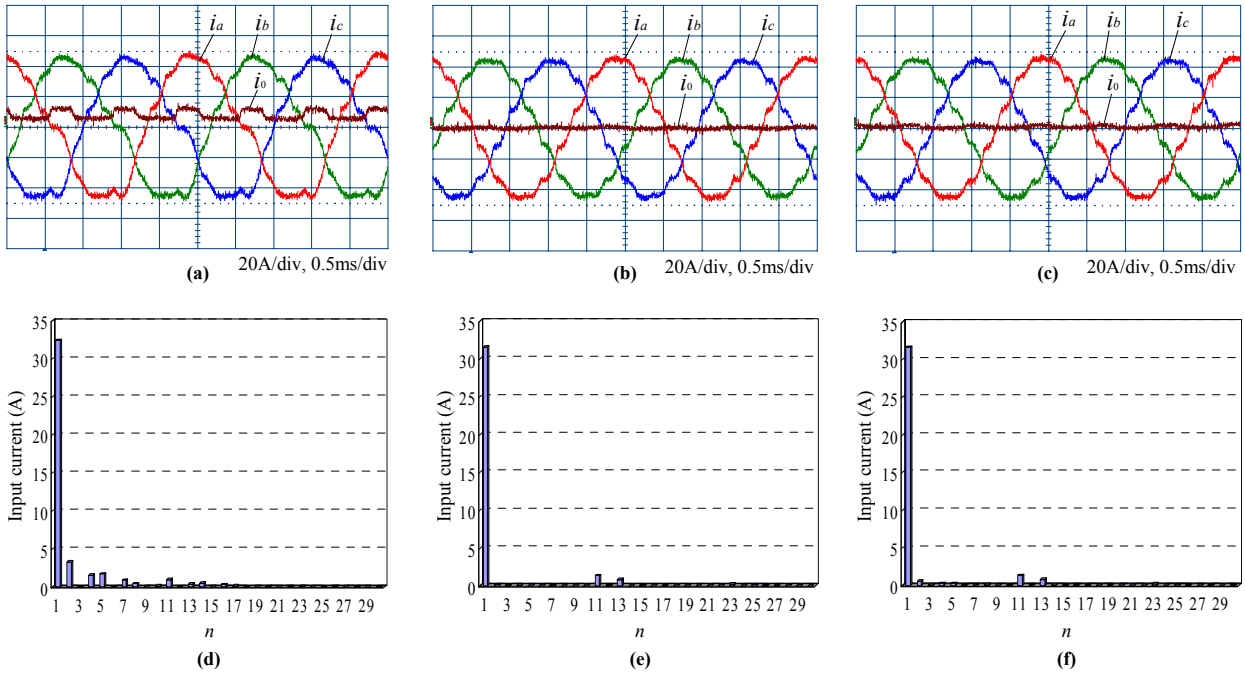

Fig.8: Measured input current waveforms i_a, i_b, i_c, zero sequence current i_0 and input current harmonics (n denotes the ordinal number of the harmonics); **(a)** and **(d)** without zero sequence current control; **(b)** and **(e)**: as (a) and (d) but employing a zero sequence current control where i_0 is measured using a through-hole current transducer LA 55-P (50A, LEM Components); **(c)** and **(f)**: as (a) and (d) but with proposed zero sequence current control employing shunt resistors for zero sequence current determination. Operating parameters: U_N=115V, f_N=400Hz, U_O=350V, P_{out}=10kW, f_P=33kHz; THD of the input current: (d) 13.7%; (e) 5.2%; (f) 5.7%.

to U_O=350V independent of the operating condition. As no input filter has been considered, the input current ripple amplitude is comparable to the fundamental amplitude for low output power resulting in a relatively low power factor. The low power factor at high output power and high mains frequency is due to the phase

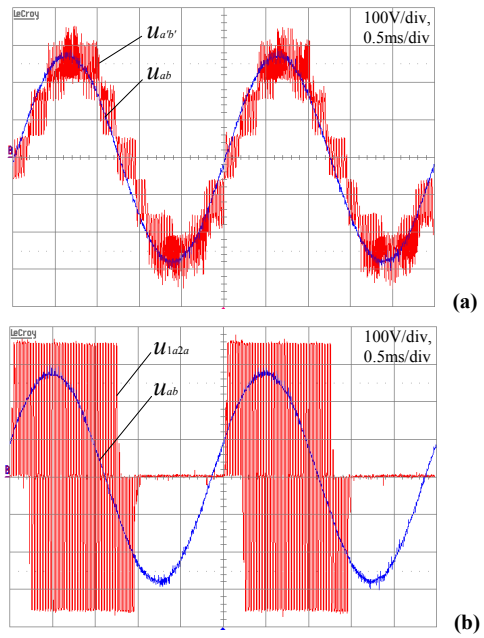

Fig.9: Measured mains line-to-line voltage u_{ab} and LIT input line-to-line voltage $u_{a'b'}$ (cf. **(a)**); **(b)**: voltages u_{ab} and u_{1a2b} across the windings W_{A+B} and W_A of the LIT of the TSHR. Operating conditions: U_N=115V, f_N=400Hz, U_O=350V, P_O=10kW, f_P=33kHz.

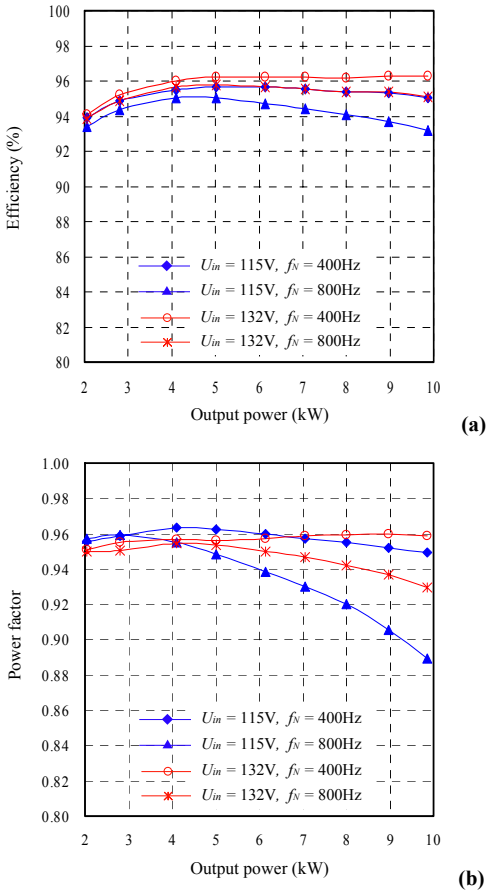

Fig.10: Measured efficiency **(a)** and power factor **(b)** of the TSHR in dependency on the output power for different input voltages and frequencies. Operating conditions: U_O=350V, P_O=10kW, and f_P=33kHz.

displacement of input current and input voltage resulting from the voltage drop across the input inductors [4]. One has to point out that the system fulfills the requirements concerning low frequency input current harmonics [8] within the whole operating range.

V COMPARATIVE EVALUATION OF SSHR AND TSHR

The distribution of the total losses to the main power components of the SSHR and the TSHR is depicted in **Fig.11**. Due to the higher frequency of the input current ripple the SSHR shows higher iron losses of the input inductors. On the other hand, higher LIT iron losses do occur for the TSHR as discussed in Section II.B (cf. Fig.2(c) and Fig.3(c)). In case the switching frequency of the SSHR would be doubled (f_P=66kHz) the main high frequency input current ripple components would occur at the same frequency and the input current ripple amplitude would be reduced and/or both systems would show about equal EMI filtering effort. However, also the switching losses of the SSHR (which does not require a zero sequence current control and employs only a single gate drive circuit) would be doubled and/or a slight reduction of the converter efficiency would have to be accepted (cf. Fig.11).

In **Fig.12**, the input current spectrum of the SSHR is depicted for f_p=33kHz (cf. Fig.12(a)) and f_p=66kHz (cf. Fig.12(b)); furthermore, the spectrum of the TSHR is shown for f_p=33kHz (cf. Fig.12(c)). The input current harmonics of the TSHR around 33kHz are significantly reduced as compared to the SSHR, but cannot be cancelled completely due to difference of the input inductor voltage $u_{a'a}$ for the turn-on periods of T_1 and T_2 (cf. **Fig.13**). The calculation of the voltage waveforms depicted in Fig.13 is with reference to the voltage envelopes being present for the passive 12-pulse rectifier (equations (6)-(10) in [6]) and under neglection

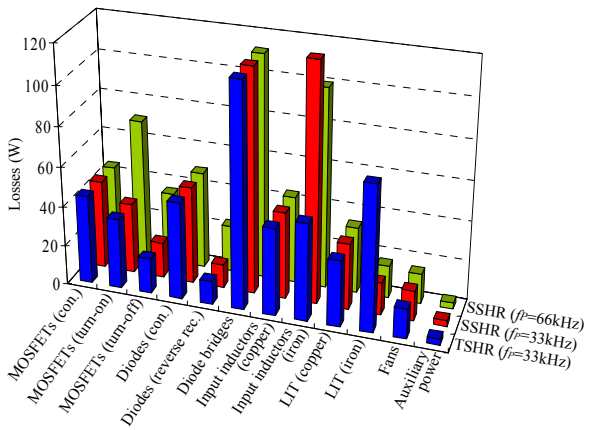

Fig.11: Calculated distribution of the losses of the TSHR for a switching frequency of f_P=33kHz and of the SSHR for f_P=33kHz and f_P=66kHz. Assumed operating conditions: U_N=115V, f_N=400Hz, U_O=350V, P_O=10kW. *Remark:* For calculating the input inductor and the LIT winding losses high frequency effects (skin and proximity effect) were neglected as both windings are realized with copper foils. The losses of the employed magnetic material were determined by measurements and were found considerably different to the data provided by the core manufacturer. The total calculated losses are in very good correspondence with the measured system efficiency.

of the diode and transistor forward voltage drops. Furthermore, the LIT leakage inductance has been neglected.

The total losses, the maximum input current ripple, and the system efficiency are detailed in **TABLE III**. In summary, the TSHR is advantageous over the SSHR concerning switching frequency input current ripple and efficiency and/or input filter and heatsink volume and therefore has to be preferred for high power density applications.

TABLE III - Simulated maximum peak-to-peak input current ripple in dependency on the switching frequency and calculated total losses and efficiency for the SSHR and the TSHR. Assumed operating parameters: U_N=115V, f_N=400Hz, U_O=350V, P_O=10kW.

System		Max. input current ripple [A]	Total losses [W]	Efficiency [%]
SSHR	f_P=33kHz	8.2	502	95.2
	f_P=66kHz	4.3	548	94.8
TSHR	f_P=33kHz	2.3	488	95.4

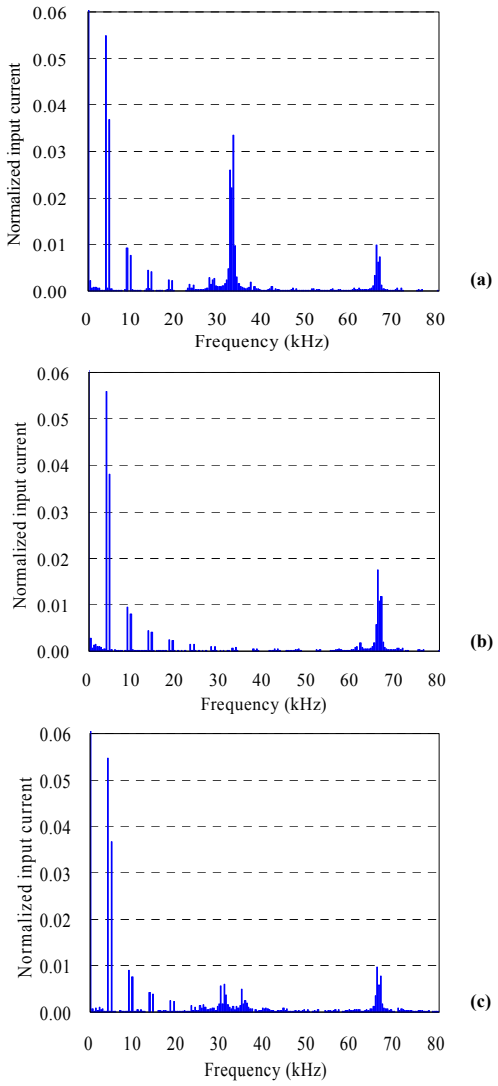

Fig12: Digital simulation of the input current spectrum of the SSHR for a switching frequency of f_p=33kHz (cf. **(a)**) and f_p=66kHz (cf. **(b)**); Furthermore shown: Input current spectrum of the TSHR for f_p=33kHz (cf. **(c)**). Assumed operating conditions: U_N=115V, f_N=400Hz, U_O=350V, P_O=10kW.

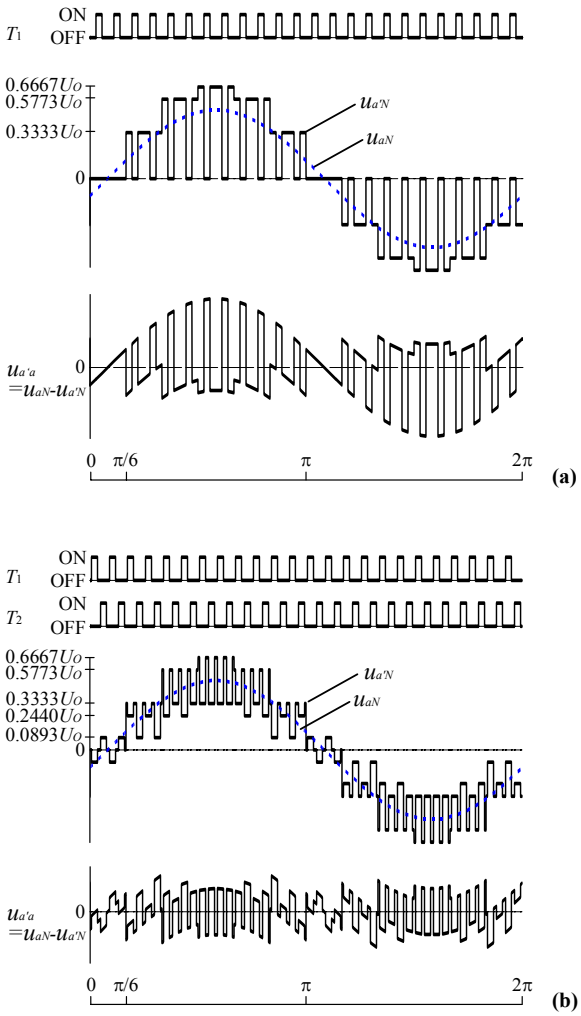

Fig13: Calculated time behaviour of the input phase voltage u_{aN}, input phase voltage $u_{a'N}$, and the input inductor voltage $u_{a'a}$ of the SSHR **(a)** and the TSHR **(b)**.

VI Conclusions

In this paper a novel single-switch and a two-switch hybrid 12-pulse LIT rectifier system with controlled output voltage are proposed and comparatively evaluated. Furthermore, results of measurements on a 10kW prototype of the TSHR are given where the theoretical considerations and a novel control concept ensuring an equal distribution of the input current to the individual TSHR output stages are verified.

Aiming for high power density the TSHR is slightly advantageous over the SSHR at the costs of a higher realization effort. The prototype of the TSHR shows high efficiency and high power factor in a wide operating range. Accordingly, the system is an attractive candidate for future More-Electric-Aircraft applications.

In a next step the thermal behaviour of the TSHR will be modelled for large peak to low average load operation as typically given for EHA systems. Furthermore, the TSHR will be evaluated against a parallel connection of two single-switch discontinuous-mode boost-type rectifier systems (TSDCMR, cf. [10,11]) operating in interleaved manner (cf. **Fig.14**) which shows a comparably low realization and control effort. The results of a first numerical analysis for the TSDCMR are illustrated in **Fig.15** and **Fig.16**. Contrary to the TSHR, the input current spectrum of the TSDCMR exhibits a 5th and 7th harmonic (cf. Fig.15(a), Fig.16) which constitutes a significant drawback as both harmonics should remain below 0.02p.u. according to aircraft harmonic standards. Furthermore, a multi-stage EMI input filter is required for attenuating the high frequency components of the input current ripple resulting from the discontinuous input current shape (cf. Fig.15(b)). The losses of the main power components, the current stresses of the power semiconductors, the measured conducted electromagnetic emissions and size and weight of the TSDCMR including the EMI will be discussed in detail in a future publication.

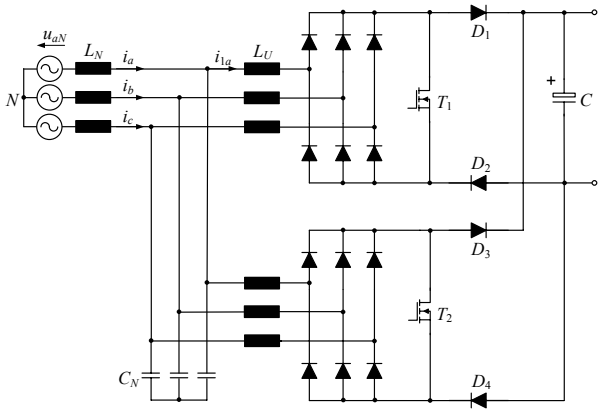

Fig.14: Parallel connection of two three-phase single-switch discontinuous mode boost rectifiers.

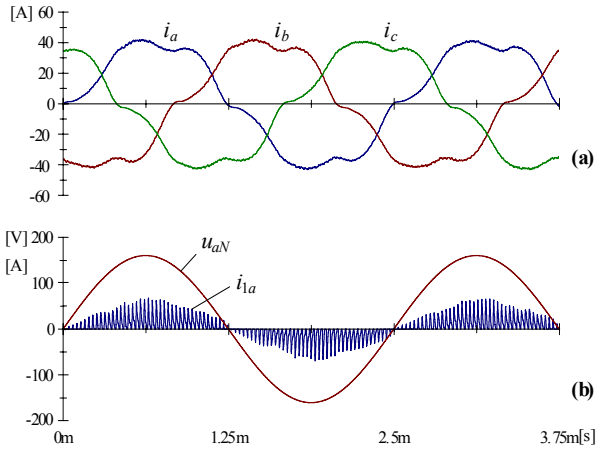

Fig.15: Simulated time behavior of input phase currents i_a, i_b and i_c (cf. **(a)**), input voltage u_{aN} and input current of one bridge i_{1a} (cf. **(b)**) of the parallel connection of two three-phase single-switch discontinuous mode boost rectifiers operating in interleaved manner (cf. Fig.14). Simulation parameters: U_N=115V, f_N=400Hz, U_O=350V, P_O=10kW, f_p=33kHz with constant duty cycle D=0.17, L_N=188µH, L_U=15µH, C_N=2µF and C=1mF. For the sake of simplicity only a single-stage LC low-pass input filter is considered.

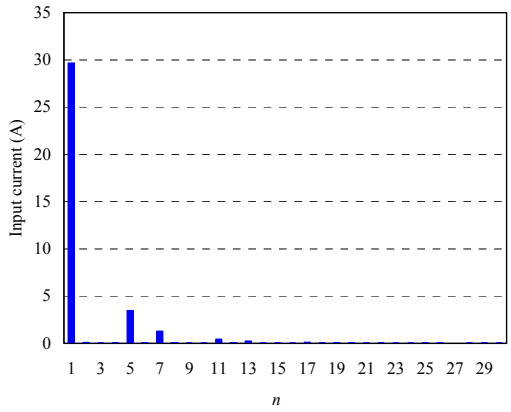

Fig16: Simulated input current spectrum (*n* denotes the ordinal number of the harmonics) of the parallel connection of two three-phase single-switch discontinuous mode boost rectifiers operating in interleaved manner. Simulation parameters: as for Fig.15; *Remark*: The lower amplitude of the fundamental as compared to the measured spectrum of the TSHR of equal output power (cf. Fig.8) is due to the neglection of system losses. The amplitude of the 5th harmonic of the input current could be reduced at the costs of an increased amplitude of the 7th harmonic by varying the duty-cycle of the switches with six times the mains frequency. The amplitudes of both harmonics are heavily dependent on the ratio of the output DC voltage and the mains voltage amplitude [10].

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