Steps Towards Prediction of Conducted Emission Levels of an RB-IGBT Indirect Matrix Converter

A. Müsing, M. L. Heldwein, T. Friedli and J. W. Kolar
Power Electronic Systems Laboratory,
ETH Zurich
Physikstrasse 3, 8092 Zurich, Switzerland

***Abstract*—Numerical prediction of conducted emissions has the potential to become an important utility in power converter design. Advance knowledge of the conducted emission and simulations of the EMC performance can help to reduce cost and time in the design process. This paper presents a detailed time-domain simulation of an Indirect Matrix Converter (IMC) for predicting common and differential mode conducted emissions. The simulation model includes the parasitic inductances and capacitances of the PCB layout, whose values are obtained using the Partial Element Equivalent Circuit (PEEC) method. The simulation also includes the EMC filter, the mains connection cable and a load model for which parameters and parasitics are obtained from measurements. The results of the simulation are compared with conducted emissions measurements of an existing IMC prototype.**

***Index Terms*—EMI modeling and simulation, parasitics extraction, PEEC.**

I. Introduction

The design of differential mode (DM) and common mode (CM) EMC input filters is a fundamental issue in converter design, since the filter strongly influences the converter's performance, for instance concerning power density or control dynamics. The filter design must ensure the compliancy with EMC standards, so that the converter can operate in a non-ideal environment with external disturbances, and to ensure it does not interfere with neighboring electronic equipment.

The conventional design procedure is to build a converter system, to measure the EM noise and conducted emission levels and perform design iterations for the input filter until its noise measurements fulfill the required EMC standard [1]. In the case of an adjustable speed drive (ASD) designed for the European market, the standard is EN 61800-3.

An alternative method of designing a filter is to simulate the converter behavior. This method permits a noise prediction without the need to build hardware. However, this method must include all relevant parameters in the system model. The importance of identifying and quantifying the parasitic impedances within a power converter system for EMC characterization has been highlighted in the literature [2]–[4]. The extraction of parasitic impedances for EMC modeling has been performed mainly for high-speed digital electronic circuits [5], [6], where operating frequencies are higher (> 1 GHz). Therefore, knowledge of the parasitic impedances is mandatory for the system to function correctly. Therefore, techniques for extracting impedances from circuit layouts already exist [6]. But these techniques are either based on approximate and inaccurate formulaes or require a lot of computational power. For parasitics extraction, the Partial Element Equivalent Circuit (PEEC) method emerged as a computational effective and accurate technique. Therefore, it makes sense to adapt this technique for power electronic systems, as in [4], in order to perform the cited tasks and to use them to optimize PCB layouts before their manufacturing. Methods which employ the impedance measurements of existing hardware prototypes [3] are possible as well. This leads to precise results, but has the disadvantage of requiring a prototype or even a series of prototypes. Therefore, the main objective of this work is to evaluate and define mathematical tools to predict the conducted emission (CE) levels of a complex power converter system prior to the construction of a prototype.

This paper presents a detailed time-domain (TD) simulation of the CE of a reverse blocking IGBT based Indirect Matrix Converter (RB-IGBT IMC) shown in **Fig. 1**. The calculated CE levels are compared with noise measurements obtained from an existing converter and filter system [7], shown in **Fig. 2**. The work demonstrates a first step towards "virtual prototyping" of such a converter in order to reduce design costs.

II. The Hardware / Experimental Setup

The analyzed system employs an Indirect Matrix Converter topology with Reverse Blocking (RB)-IGBTs at the input stage and conventional IGBTs at the output, where two switches and fast recovery freewheeling diodes are included into a single power module for each output phase, respectively. For more details of the converter structure, see **Table I** and [7]. A block diagram of the whole converter structure is depicted in **Fig. 3**, which is also used in the experimental verification of the

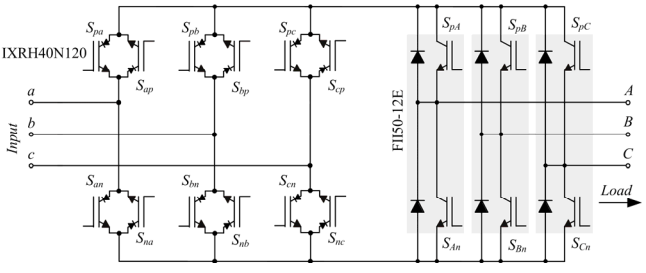


Fig. 1. Schematic of the IMC power circuit. The input stage utilizes IGBTs with reverse blocking capability.

Fig. 2. Photograph of the analyzed RB-IGBT indirect matrix converter (Dimensions: 76 mm x 120 mm x 260 mm).

performed simulation. This work aims at the prediction of CE measurements from a typical measurement setup, where a quasi-peak (QP) detector is employed as specified in CISPR 16. The prediction is separated into common mode (CM) and differential (DM) mode noise [8], since this brings important information for the design of EMC filters and, in a second step, possibility of improvement of the power circuit layout and the environment of the power components. Finally, the predicted results are compared with experimental results.

In order to remove all possible external noise sources, the load machine was replaced by a three-phase passive RL load, and the built-in auxiliary power supply was replaced by an external voltage source. Thus, the only non-modeled HF noise sources are the digital signal processing board and the internal gate drive power supplies. The latter is a self oscillating half bridge operating at a switching frequency of 80 kHz. A voltage measurement at the gate drive isolating transformers revealed a high frequency oscillation with strong components of 3.9 MHz and 7 MHz, which may influence the matching between CE simulation and measurement in this frequency range.

III. Converter Modeling

In principle, a frequency domain (FD) simulation of the converter is possible as well as a TD simulation. Actually, the FD simulation needs less computation power than a TD simulation [9] and might ease the incorporation of frequency dependent impedances. In this work, TD modeling has been chosen, because modeling

TABLE I

Specific Data of the Exerimental Setup

Input RMS phase voltage	3 x 230 V
Mains frequency	50 Hz
IMC switching frequency	12.5 kHz / 25 kHz
Output frequency	40 Hz
Real output power	2.1 kW
Load resistance	L = 12 Ω
Load inductance	25 mH

the complicated IMC structure and the complex control scheme represents less effort in TD. The computation task is therefore heavy in CPU and memory usage, because the simulation time steps must be in the range of nanoseconds to get accurate results up to high frequencies. A Simplorer circuit simulation run with a 10 ns time-step requires 4 hours for one mains period on a desktop PC with 1 GB of RAM and a 3 GHz CPU. The trend of increasing computation power will diminish the computation time in future, so that even more detailed circuit simulation models can be calculated in reasonable time.

Besides the power circuit, the simulation includes a detailed model for the EMC filter, for the employed load and for the power cable connecting the LISN and the filter. A block diagram of the whole simulation model is shown in **Fig. 3**. The modeling procedure of the single blocks will be given in the following. The EMC simulation model would be more manageable without the filter and cable model. However, these components were already integrated in the existing prototype and could not be removed for the measurement.

To predict the CE levels precisely, the simulation must include appropriate semiconductor models (Section III.C) and all significant parasitic circuit impedances [2]. They are mainly caused by stray inductances of the printed circuit board (PCB), parasitic capacitances to protective earth (PE) and non-ideal behavior of filter components. These impedances lead to low impedance high-frequency paths and unbalances among current paths, resulting in DM and CM noise and DM/CM noise transformation.

For the parasitics extraction of the circuit layout, the Partial Equivalent Electric Circuit method is used. This is discussed in Section III.D. For complex flat structures as on PCBs, the PEEC method performs much better than finite element methods as PEEC does not need a discretization of the three-dimensional free space – only the

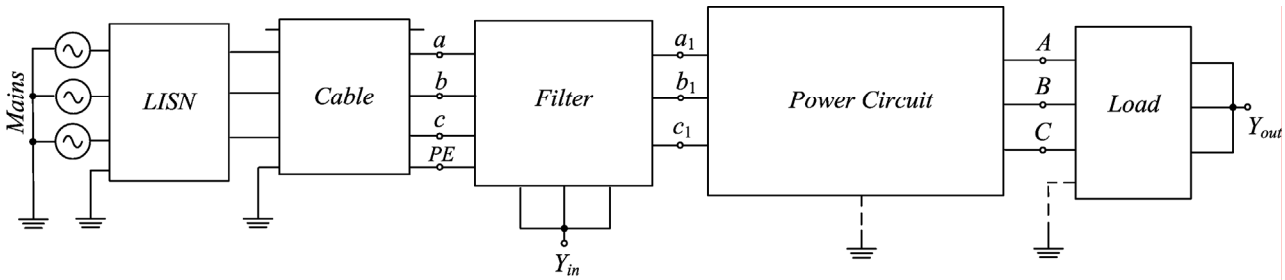


Fig. 3. Block diagram of the IMC prototype and model. The DM and CM noise measurement is performed at a 50 Ω resistance to ground inside the Line Impedance Stabilization Network (LISN). The source for EMI noise is the switching Power Circuit. The DM noise propagates through the filter and the cable towards the LISN, while the CM noise is caused by step voltage changes across parasitic impedances.The CM noise propagates mainly through parasitic impedances to protective earth (indicated by dashed lines).

TABLE II
CABLE PARAMETERS

L [µH/m]	M [µH/m]	R [mΩ/m]	$C_{c,1}$ [pF/m]	$C_{c,2}$ [pF/m]
1.32	0.60	11.9	93.7	7.47

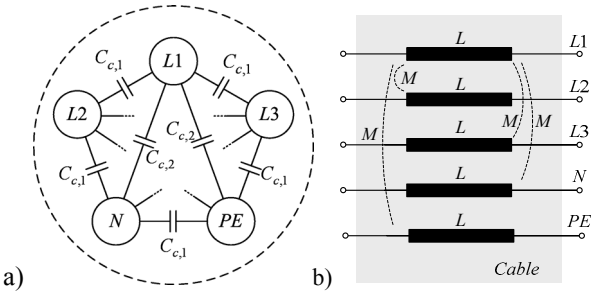


Fig. 4. Input unshielded cable model: a) Per unit length capacitive network model for the considered cable. Two different capacitance values dependent on the mutual distance of the wires are obtained from measurements (Table II). Only two out of five $C_{c,2}$ capacitors are shown. b) Per unit length inductive network model for the considered cable. The picture shows only the mutual magnetic couplings M of phase $L1$.

copper PCB tracks need to be included into the model [2]. The parasitic values of passive components, especially of those in the EMC filter, are obtained from impedance measurements.

A. Modeling of the Supply Cable

The modeling of the unshielded input supply cable of 3 meters length is of high importance, since it influences the high frequency (HF) behavior of the complete circuit. A cable with five conductors is employed for the measurements, and its simplified model is used here. The model considers self- and mutual inductances between conductors and also a capacitance matrix among all conductors. The model is based on "per unit length" parameters, which are shown in **Fig. 4**. A series of measurements were performed in order to obtain the parameters through a parameter identification routine. The final parameter values are presented in **Table II**. The circuit employed for the simulations used a four-stage lumped parameter model, since implementing a five-conductor transmission line would substantially increase the computational effort. A comparison between the measured impedances and simulated four-stage lumped

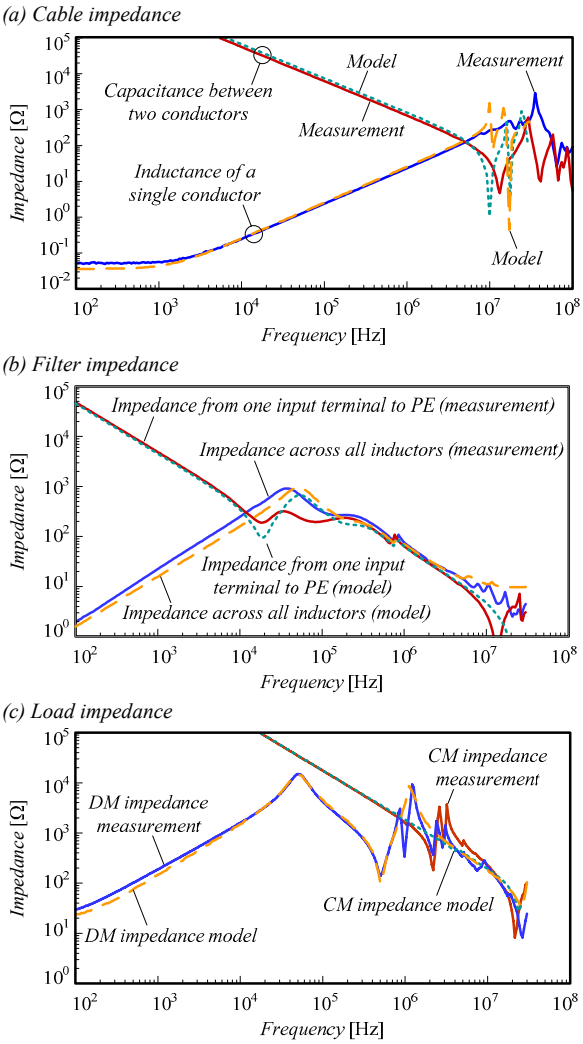


Fig. 6. Comparison between measured and modeled CM and DM impedances: (a) cable, (b) filter, (c) load impedance.

circuit is shown in **Fig. 6**(a), which shows excellent model accuracy up to 7 MHz.

B. Modeling of the Input Filter

The CM and DM input filters are modeled according to the individual models of each of its components. Capacitive and magnetic couplings among different components are not considered and this increases uncertainties in the simulation mainly in the HF range typically > 5 MHz [10].

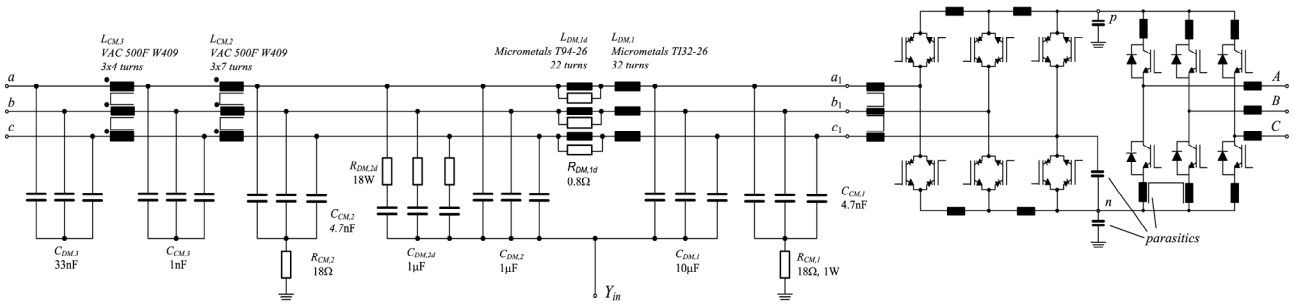


Fig. 5. Schematic of the EMI filter and the IMC power circuit. The EMI filter components were modeled with their first order parasitics (cf. Fig. 7), which are not shown in the figure for the sake of clearness. Furthermore, some of the parasitic impedances are indicated in the power circuit. Since the PCB layout topology is more complicated than this circuit diagram and there are numerous couplings existing, not all of the used parasitics and couplings are displayed.

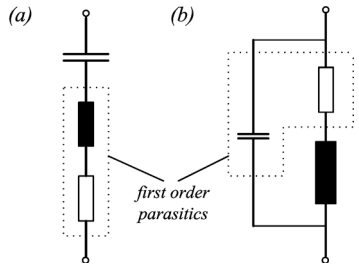


Fig. 7. First order parasitic model for (a) capacitors and (b) inductors. All passive components inside the EMI filter are modeled by this first order approximation, the parasitics values are obtained from measurements or calculations. Variation of cores' permeability with frequency is modeled as well.

Impedance measurements and calculations are used to create equivalent circuits for all filter components, which are modeled with their first order parasitics (**Fig. 7**), so that every filter inductor or capacitor in **Fig. 5** is composed of the main *L*/*C* component and additional parasitics. For the sake of clarity these parasitics are not shown in Fig. 5. Impedance measurements performed in the hardware are compared with the model simulation in **Fig. 6**(b), which shows the model validity up to 5 MHz.

C. Modeling of the Load

The load employed at the measurements is a three-phase *RL* network. In order to take its HF behavior into consideration a simplified model is derived based on two impedance measurements, one which basically shows the DM impedance (Z_{01}) and a second one, which shows the CM impedance (Z_{02}) as in **Fig. 8**(a). The load is assumed symmetrical; the derived model is depicted in **Fig. 8**(b). The measurement results are compared with the impedance calculation in **Fig. 6**(c), where it is seen that a good match is observed except for the HF resonances > 5 MHz. However, including parameters to improve the high-frequency response would substantially increase the models complexity.

D. Behavioral IGBT Modeling and Freewheeling Diode Reverse Recovery

Conducting an experimental evaluation as proposed in [11] provides a precise noise source model for switching power devices. In the present work, this experimental method is not used because the high number of switches (18) and switching states seen in the normal operation of the IMC would require a significant effort in the modeling procedure.

In this work the use of simulation tools is employed, since the models are based on experimental switching waveforms. There are several possibilities for the modeling of semiconductor devices: physical models or SPICE models of the devices would be the most accurate, but they lead to significant calculation times for a TD simulation. Furthermore, the lack of available datasheet information on the used RB-IGBTs (IXRH40N120 and FII50-12E), which is needed for an IGBT SPICE model, makes a simplified model reasonable and efficient for computer simulation.

In this study a first order behavioral IGBT model as proposed in [12] is used. This model is shown in **Fig. 9**. It consists of a few discrete devices and can be implemented easily in a circuit simulator. The IGBT switching edge is triggered due to changes in a time dependent conductivity $G(t)$ as depicted in **Fig. 9**(b). The values of v_{ss}, r_c, $C(u)$ and the time behavior $G(t)$ are determined by experimental measurements and subsequent fitting of the simulated behavior to the curves obtained by experiments. This IGBT model is sufficient to allow a reasonable simulation time and provides good results for the CE noise prediction. In the simulation, the IGBT model acts as a noise source and the observed voltage waveforms result from the interaction with the parasitic impedances.

The freewheeling diodes of the output stages are modeled using a detailed Simplorer diode model which includes the diode reverse recovery effect. The model reverse recovery time was set to t_{rr}=180 ns, according to datasheet information of the used diode. In comparison to a complex IGBT SPICE model, the diode model is simpler and does not appreciably increase the simulation time.

E. Parasitics Extraction and PEEC Modeling

The layout parasitics are extracted using the Partial Equivalent Element Circuit (PEEC) method [13], [14]. In the PEEC method, a conductor is discretized into many partial elements as shown in **Fig. 10**. The PEEC model creates matrices of partial inductances Lp_{ij}, partial coefficients of potential P_{ij} and node resistances R_m. From this, an equation system is generated which gives a full wave solution of the electrical field integral equation,

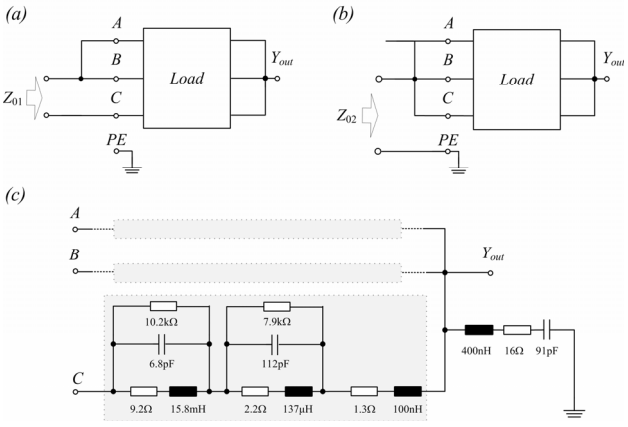


Fig. 8: Load impedance measurement setups: (a) DM impedance measurement, and (b) CM impedance measurement. (c) Load simulation model - only one of the three symmetric load phases is shown.

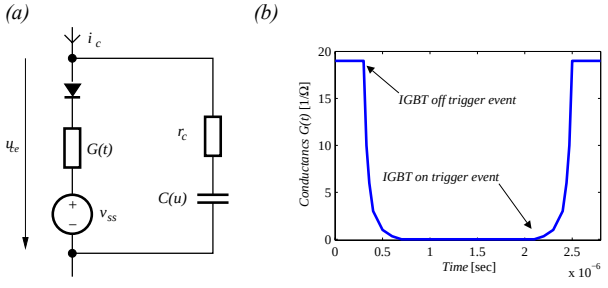


Fig. 9. (a) Behavioral IGBT model, details see [12] (b) the switching event is triggered by a time-dependent conductance $G(t)$.

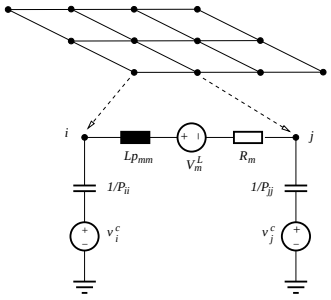


Fig. 10. Geometry discretization and PEEC model [13]. Here, only the self term of potential and inductance are displayed. The full matrix model also contains mutual couplings of the equivalent circuit elements.

including high frequency effects like skin and proximity effects. In general, a time-retarded simulation which considers the finite speed of electromagnetic waves is possible with the PEEC simulation method, too. To increase the calculation speed, a quasi-static model was chosen which implies an infinite fast velocity of the waves. However this is a valid approximation for the analyzed frequencies, which are lower than 30 MHz and circuit geometry layout smaller than 50 cm [15]. A Java

program was developed for the PCB parasitics extraction, which is able to import PCB geometries from a Gerber file format. In the graphical user interface, as seen in **Fig. 11**, one is able to set probes to arbitrary points of interest at which impedances and mutual couplings will be calculated.

Furthermore, the program connects adjacent conductors and builds a mesh for the PEEC solver. The generated mesh consists of many rectangular conductor cells and gives a good approximation of the actual PCB layout. In the case of the IMC, the conductor discretization was in magnitude of 2-3 mm. Therefore, the parasitics extraction has an adequate accuracy but, to keep the calculation effort manageable, the number of partial elements is limited to several thousands.

The result of the PEEC calculation is an impedance matrix

$$\underline{Z} = \begin{pmatrix} \underline{z}_{11} & \underline{z}_{12} & \underline{z}_{13} & \cdots \\ \underline{z}_{21} & \underline{z}_{22} & \underline{z}_{23} & \cdots \\ \underline{z}_{31} & \underline{z}_{32} & \underline{z}_{33} & \cdots \\ \cdots & \cdots & \cdots & \cdots \end{pmatrix}, \qquad (1.1)$$

in which the main diagonal describes the self-impedance between two probe points and the off-diagonal elements denote the coupling between separate current paths. Due to skin- and proximity effect, the exact solution of the impedance matrix is frequency dependent $\underline{Z} = \underline{Z}(\omega)$. The frequency-dependent real part $Re(\underline{Z}(\omega))$ is based on the electric resistance of the copper tracks on the PCB, which can be neglected in comparison to the on-resistance of the power switches. The remaining imaginary part (i.e. the inductive or capacitive behavior) $Im(\underline{Z})$ is only weakly influenced by skin- and proximity effect and can be modeled by a simple *CL*-network, as indicated in the power circuit schematics in Fig. 5. The skin-effect is considered in the way that PEEC impedance calculations were conducted at a high frequency (1 MHz), where the currents concentrate on the conductor edge. Dependent on the conductor geometry, the high frequeny inductance shifts in the range of typically 30 % in comparison to the low freqency value.

The PCB of the IMC is modeled as a 2.5-D-geometry, that means the copper layers have no discretization in the *z*-direction, but the positions of the layers in the PCB layer stack are included into the model. This simplification is possible because the copper layer thickness is negligible in comparison to the width of the current path. **Fig. 12** shows three layers of the IMC power circuit, from which the impedance matrix is extracted. With the calculated values of $\underline{Z}$, a simulation model of the IMC is created which includes the relevant PCB track inductances and capacitances.

In general, inductances are only reasonable for current loops. In a switching power electronics converter, the current paths are changing due to commutation and the actual current path is determined by the switch configuration. This is incorporated in the model in such a way that partial inductances and their mutual couplings are considered for every commutation path. The total loop inductance is then determined by

$$L_{tot} = \sum_{i,j} L_{ij}, \qquad (1.2)$$

where the diagonal elements L_{ii} are the self inductance terms and the off diagonal elements indicate the mutual inductance of different current paths. The determined impedance network, including the self- and mutual couplings (1.2), defines the total loop inductance of every current path during the circuit simulation.

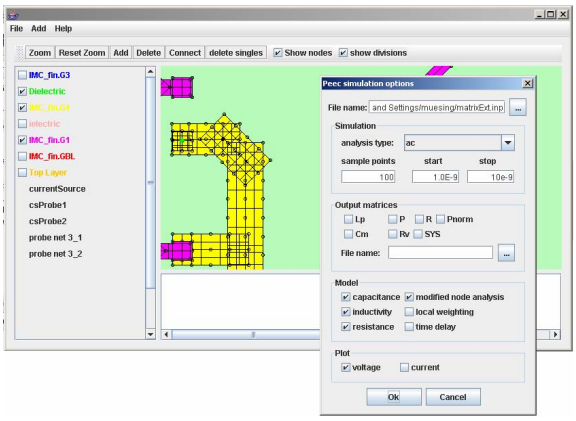


Fig. 11. Graphical user interface of the PCB layout extractor: The screenshot shows a pane of the IMC PCB with a rectangular conductor discretization and an input mask for the PEEC solver.

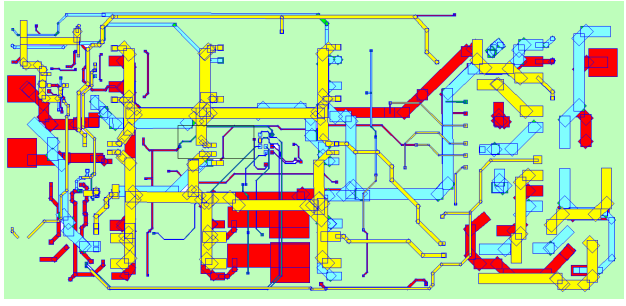


Fig. 12. PEEC model of the three power PCB layers of the 6-layer IMC printed circuit board.

TABLE III
MEASUREMENT EQUIPMENT EMPLOYED IN THE TEST SETUP

Qty.	Equipment	Specification
1	Test receiver	Rohde & Schwarz – ESPI 9 kHz … 3 GHz
2	LISN	Rohde & Schwarz – ESH3-Z5 Two-lines, V-network
1	LISN	Rohde & Schwarz – ESH2-Z5 Four-lines, V-network

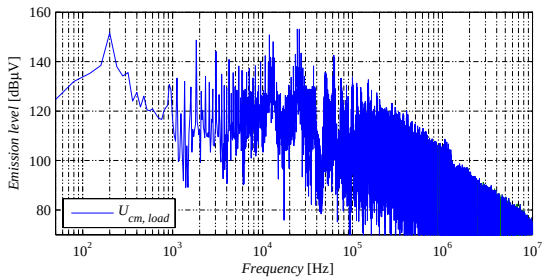
IV. Conducted Emission Measurements

For conventional EMC compliance testing DM and CM mode emissions cannot be separated. Therefore, a three-phase DM/CM noise separator [8] has been employed in order to allow an evaluation of both noise modes. The noise separator requires simultaneous access of all three LISN outputs. The tests with the IMC prototype supplying a three-phase *RL* star-connected load was performed with three individual LISNs (cf. **Table III**). An analog power amplifier with low inner impedance was used simulating the mains so that the conditions were close to the conditions assumed for the simulation of the system.

V. Simulation Results

As a first test of the accuracy of the computer simulation model, a comparison of the CM voltage spectrum measured between the load star point Y_{out} and the DM filter star point Y_{in} was conducted. The results are shown in **Fig. 13**. For lower frequencies, the two spectra coincide very well, except for minor differences, which originate from the finite measurement length of both, measurement and simulation. Fig. 13 shows the spectrum obtained by a Fast Fourier Transform (FFT) for a 50 Hz mains period. A longer simulation and measurement interval would potentially provide a better correlation of the low frequency curves because not all of the possible converter states resulting from the interaction of the 50 Hz mains period and the 40 Hz output period are included here. The appearance of the input stage switching frequency (12.5 kHz) and the output switching frequency (25 kHz) is obvious. The simulated and the measured levels are very close up to 2 MHz, where a slight peak is observed for the measurements, which is not seen in the simulation results. Besides the difficulties in accurately measuring the CM voltage in the hardware setup due to the large loop resulting from the geometrical distance of the probe and ground lines, a cause for this difference is probably the larger voltage spikes observed during the switching of the input stage of the IMC.

(a) Computer simulation



(b) Oscilloscope measurement

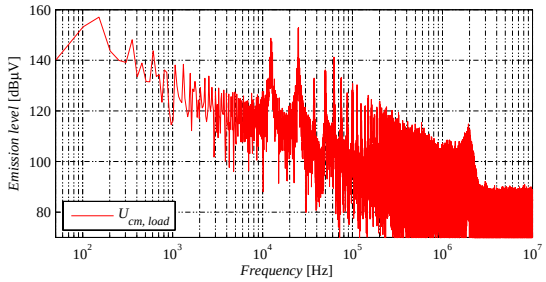


Fig. 13. Common mode spectrum measured between the load star point Y_{out} and the star point Y_{in} of the differential mode filter, see Fig. 3: a) computer simulation, b) result obtained from an oscilloscope measurement.

The comparison of measured and simulated waveforms is presented in **Fig. 14**, where the voltage across the "DC-link" of the IMC is shown. It is observed that the voltages follow a closely related pattern and the simulation is able to predict even secondary effects.

The predicted conducted emission levels are measured at a 50 Ω termination to PE at the LISN output. The common mode emission voltage is calculated by

$$u_{cm} = \frac{1}{3}(u_{A,LISN} + u_{B,LISN} + u_{C,LISN}), \tag{1.3}$$

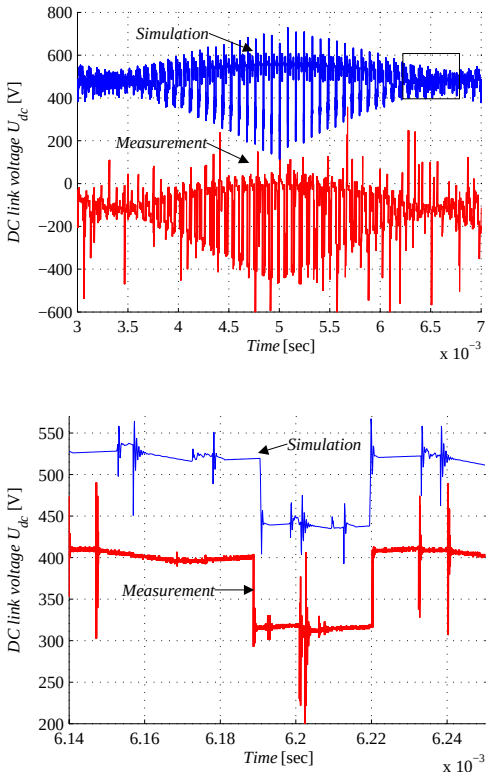


Fig. 14. Simulation and measurement of the DC link voltage between the nodes p and n (cf. Fig. 3). The lower picture shows a magnification of the framed area.

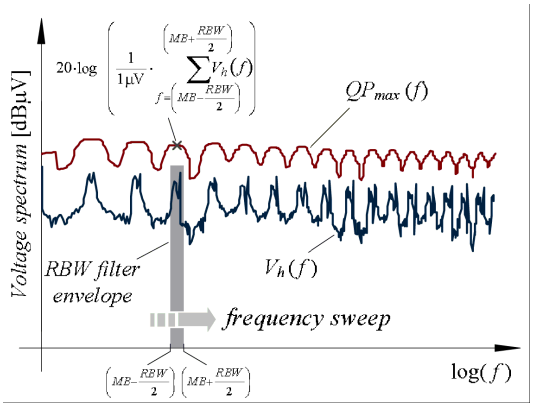


Fig. 15. Illustration for the performed quasi-peak measurement worst case approximation where $V_h(f)$ represents the input voltage of a test receiver and $QP_{max}(f)$ the maximum obtainable value for the QP measurement.

where $U_{i,LISN}$ are the measured voltages at the three LISN phase legs and

$$u_{dm} = \frac{1}{3}(2u_{A,LISN} - u_{B,LISN} - u_{C,LISN}) \tag{1.4}$$

is the calculated differential mode voltage for phase A. The subsequent FFT results in an emission spectrum according to Fig. 13.

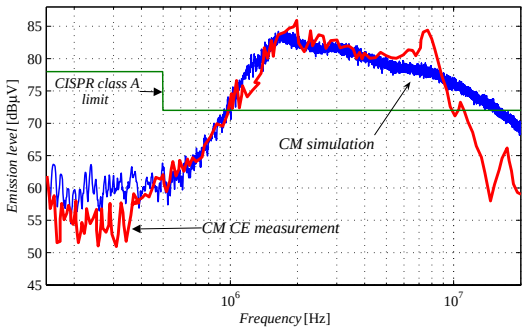
In order to test the performance of the simulation procedure, the standard CISPR 11 was chosen for establishing the performance requirements, where the frequency range of 0.15 MHz to 30 MHz is considered for class A equipment. The voltage measured at the resistor, representing the input of a test receiver, in the simulation is used to calculate a quasi-peak maximum value $QP_{max}(f)$. This is performed by linearly adding the values $V_h(f)$ of the spectral components positioned inside of the specified resolution bandwidth (RBW) as shown graphically in **Fig. 15**. By employing this procedure, one reduces the computational effort and the calculated emission level is slightly higher than the ones resulting from the exact calculation. The final result of the simulated CM and DM noise spectra, compiled according to the QP calculation of Fig. 15, is depicted in **Fig. 16** along with the obtained experimental results.

VI. Discussion

The CM and DM CE levels show a very good correlation between measurement and simulation up to 5 MHz, from where it is probable that the non-modeled capacitive and magnetic coupling among the filter components becomes significant [16].

In the low frequency range 200-300 kHz, the simulated CM emission is about 5 dB higher than the measured values. It turned out that the CE spectrum is very sensitive to the load impedance to ground, which is the main CM noise path in this case. The most probable reason is the difficulty of experimentally measuring the capacitive coupling between the power semiconductors and the heatsink. Other reasons are the inter-component couplings and the influence of the gate drive, which provides various paths for HF currents. Furthermore, the

(a) CM spectrum



(b) DM spectrum

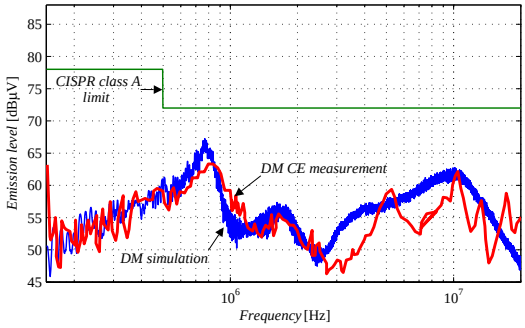


Fig. 16. Differential and common mode noise measurement and simulation. The simulated spectrum was compiled according to Fig. 15.

models used for the cable, filter and load become less accurate for high frequencies > 5 MHz. The inclusion of the input EMC filter in the experiments increases the uncertainties of the model, as it becomes highly dependent on the modeled impedances. In order to diminish uncertainties, the EMI filter should be removed in the next step of model validation.

VII. Conclusions/Outlook

Due to the improving simulation techniques and increasing computational power, the assistance of computer simulations in power converter design will definitely gain importance in the future. This paper demonstrated the first step in the EMI noise modeling and simulation for an RB-IGBT Indirect Matrix Converter.

The converter model included the most important layout parasitics of the IMC power circuit obtained using the PEEC method. Furthermore, detailed models for the power semiconductors, the supply cable, the load and the EMI filter were used, including first order parasitics obtained by impedance measurements and calculations. The prediction of DM and CM conducted emission levels shows good agreement with the measurement up to 5 MHz. This result is highlighting the feasibility of computer simulations to predict CE levels.

In order to increase the accuracy of the prediction, further steps seem to be required, namely: (*i*) the 3-D modeling of the power semiconductor modules and their interfaces; (*ii*) the 3-D modeling of the heatsink and especially its connections to protective earth, and (*iii*) the 3-D modeling of the EMC filter components and their mutual couplings. All these steps are to be taken in near future. In the ongoing research, the next steps will be to validate the model with more detailed measurements and

according comparisons to the simulation results. In particular, a step-by-step approach from an unpopulated PCB to a complete power converter will be accompanied by impedance measurements and corresponding simulations to prove the correctness of the submodels.

The model as presented in this work will be refined, including parasitics responsible for resonances in the very HF range. This step-by-step refinement of the simulation model is expected to shift the matching frequency of simulational results and CE measurement to higher frequencies. A detailed sensitivity analysis of the model parameters will give information where the model needs further extension and, contrarwise, where it can be simplified to speed-up the computation.

Except for the inclusion of permeable materials of inductor cores, the PEEC solver used in this work is able to calculate impedances and parasitic couplings for conductors of arbitrary geometries. Therefore it is able to generate the required simulation models and to replace the models obtained from impedance measurements by a pure computational approach.

In order to use the presented PEEC parasitics extraction method and simulation model as a standard package in the converter design process, the modeling requires some important improvements, for example the use of non-orthogonal volume elements in the PEEC method for an accurate, unified PCB discretization [17]. Furthermore, a closer integration of the parasitics extractor and the circuit simulator is desirable, because a manual integration of the parasitics network into the simulation model is a time-consuming and error-prone process.

The major advantage of the presented simulation model is that it is not restricted to the IMC. This simulation method will be able to assist in the development and the design of CM and DM filters for new converter systems of arbitrary types. The long term aim in this field is to combine thermal simulations, electromagnetic and circuit simulations. This combination is necessary for a valid model of a power converter, because the different physical domains have a strong influence on each other.

REFERENCES

[1] M. L. Heldwein, T. Nussbaumer and J. W. Kolar, "Differential Mode EMC Input Filter Design for Three-Phase AC-DC-AC Sparse Matrix PWM Converters", *Proceedings of the 35th IEEE Power Electronics Specialists Conference*, 2004, pp. 284-291.

[2] R. Pasterczyk, C. Martin, and J. Schanen, "Semiconductors and Power Layout: New Challenges for the Optimization of High Power Converter", *Proceedings of the 34th Power Electronics Specialist Conference*, vol. 1, 2003, pp. 101–106.

[3] L. Yang, F. C. Lee and W. G. Odendaal, "Measurement-Based Characterization Method for integrated Power Electronics Modules", *Proceedings of the 8th Applied Power Electronics Conference and Exposition*, vol. 1, 2003, pp. 490–496.

[4] P. Musznicki, J.-L. Schanen, B. Allard and P. Chrzan, "Accurate Modeling of Layout Parasitics to Forecast EMI Emitted from a DC-DC Converter", *35th Annual IEEE Power Electronics Specialists Conference*, vol. 1, 2004, pp. 278–283.

[5] J. Fan, J. Drewniak, H. Shi and J. Knighten, "DC Power-Bus Modeling and Design With a Mixed-Potential Integral-Equation Formulation and Circuit Extraction", *IEEE Transactions on Electromagnetic Compatibility*, vol. 43 (4), 2001, pp. 426–436.

[6] W. Kao, C. Lo, M. Basel and R. Singh, "Parasitic Extraction: Current State of the Art and Future Trends", *Proceedings of the IEEE*, vol. 89 (1), 2005, pp. 729–739.

[7] T. Friedli, M. L. Heldwein, F. Giezendanner and J. W. Kolar, "A High Efficiency Indirect Matrix Converter Utilizing RB-IGBTs", *Proceedings of the 37th Power Electronics Specialists Conference*, 2006, pp. 1199-1205.

[8] M. L. Heldwein, T. Nussbaumer, F. Beck and J. W. Kolar, "Novel Three-Phase CM/DM Conducted Emission Separator", *Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition"*, vol. 2, 2005, pp. 797-802.

[9] J.-S. Lai, X. Huang, E. Pepa, S. Chen and T. Nehl, "Inverter EMI Modeling and Simulation Methodologies", *IEEE Transactions on Industrial Electronics*, vol. 53 (3), 2006 pp. 736–744.

[10] E. Hoene, A. Lissner, S. Weber, S. Guttowski, W. John and H. Reichl, "Simulating Electromagnetic Interactions in High Power Density Converters", *Proceedings of the 36th Power Electronics Specialists Conference*, 2005, pp. 1665-1670.

[11] Q. Liu, F. Wang and D. Boroyevich, "Conducted EMI Noise Prediction and Characterization for Multi-Terminal Behavioal (MTB) Equivalent EMI Noise Source Model", *Proceedings of the 37th Power Electronics Specialists Conference*, 2006, pp. 415–421.

[12] J. Tichenor, S. Sudhoff and J. Drewniak, "Behavioral IGBT Modeling for Predicting High Frequency Effects in Motor Drives", *IEEE Transactions on Power Electronics*, vol. 15 (2) pp. 354-360.

[13] J. Ekman, "Electromagnetic Modeling Using the Partial Equivalent Circuit Method", Ph.D. thesis, *EISLAB, Luleå University of Technology, Sweden,* (2003).

[14] A. E. Ruehli, "Equivalent Circuit Models for Three-Dimensional Multiconductor Systems", *IEEE Transactions on Microwave Theory and Techniques*, vol. 22 (3), 1974, pp. 216–221.

[15] A. E. Ruehli and E. Chiprout, "The Importance of Retardation in PEEC Models for Electrical Interconnect and Package (EIP) Applications", *Electrical Performance of Electronic Packaging*, 1995, pp. 232-234.

[16] S. Wang, F. C. Lee, D. Y. Chen and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance", *IEEE Transactions on Power Electronics*, vol. 19 (3), 2004, pp. 869- 877.

[17] A. E. Ruehli, G. Antonini, J. Esch, J. Ekman, A. Mayo and A. Orlandi, "Nonorthogonal PEEC Formulation for Time- and Frequency-Domain EM and Circuit Modeling", *IEEE Transactions on Electromagnetic Compatibility*, vol. 45 (2), 2003, pp. 167–176.