A New 3-phase Buck-Boost Unity Power Factor Rectifier with Two Independently Controlled DC Outputs

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***Abstract* -- A new 3-phase buck-boost unity power factor rectifier consisting of a 3-phase bridge buck PFC rectifier and two boost dc-dc converters connected in series is proposed for an industrial application where two independent output voltages need to be controlled. This paper presents the proposed topology and the requirements for this application. The proposed and alternative topologies are briefly compared. Through this comparison, it is shown that the proposed topology offers the best solution in terms of simplicity and functionality. The operation of the new topology is described in detail and then the control strategy including PWM calculations to obtain the best performance is given. The validity of the theory and practicality of the new rectifier system is confirmed through simulation and experimental results obtained from a 5 kW prototype.**

I. INTRODUCTION

A new 3-phase PFC topology with two independent dc outputs [1], shown in Fig. 1, has been developed for an industrial application where two independent high-power heater loads require regulation. The voltages applied to the loads need to be controlled independently since the heaters are employed in different stages of a continuous drying process. The topology consists of a 3-phase bridge-type buck PFC rectifier with an ac ripple current and EMI filter, a dc inductor L_{DC}, and two boost dc-dc converters (Conv.-1 and -2) connected in series. The requirements for the converter system in the particular heating application are as follows:

1. Control range of the output voltage (U_1 and U_2) must be from zero to a value higher than the peak of the utility voltage.
2. Zero output voltage condition for both boost converters can occur at the same time.
3. Simultaneously a zero output voltage and a non-zero output voltage can occur in the respective dc-dc converters.
4. Entirely independent control of the two output voltages is needed.
5. A Unity-PWM-Index (UPI) condition (i.e. a non-switching condition) is preferred for one dc-dc converter when the required output voltage is lower than the utility voltage.
6. A UPI condition is preferred for one dc-dc converter when the other converter is producing zero output voltage.
7. Minimize the number of passive components.

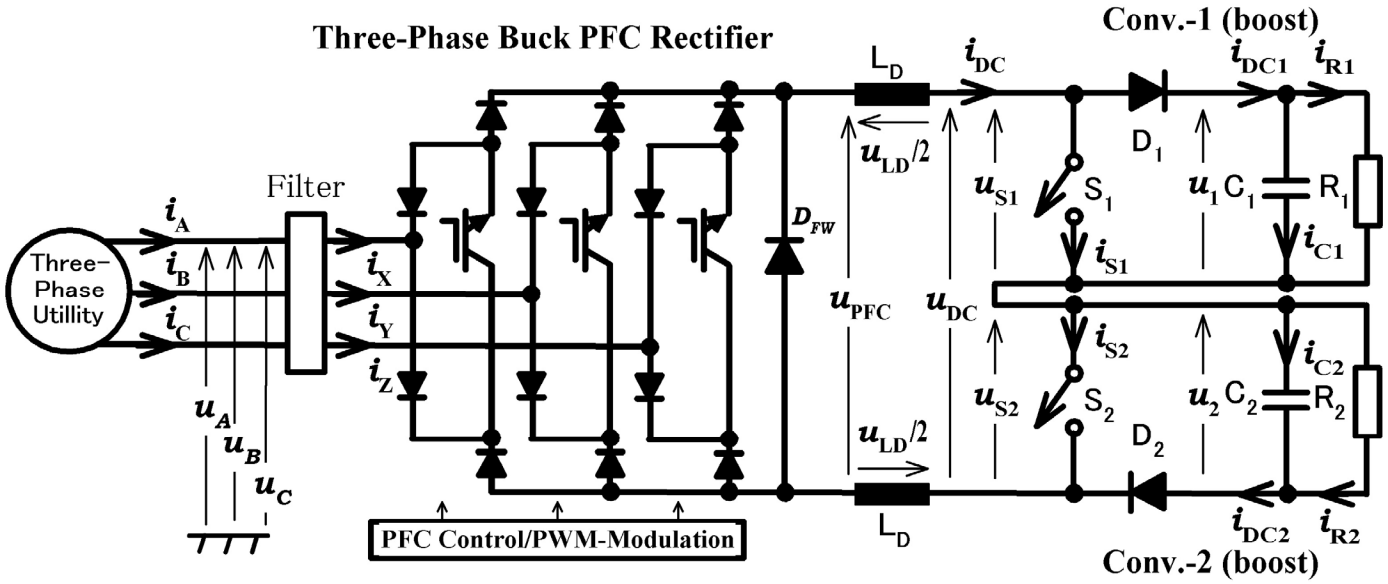


Figure 1. Proposed Topology Consisting of 3-Phase Buck PFC and Two Boost DC-DC Converters Connected Directly in Series. ("Buck+Series-Boost")

II. COMPARISONS OF POSSIBLE TOPOLOGIES

Although there are several candidate topologies [2] to satisfy the requirement in this application, a 3-phase PFC rectifier and dc-dc converter cascade system (for example, as in [3]) is desirable since both the PFC and the dc-dc converter are well developed. By using this choice, only the combination of a "3-phase buck PFC and cascaded two boost dc-dc converters directly connected in series" ("Buck+Series-Boost," Fig. 1) and a "3-phase boost PFC and cascaded two buck dc-dc converters connected in parallel" ("Boost+Parallel-Buck," Fig. 2) satisfy the major requirements. However, the "Boost+Parallel-Buck" topology realizes UPI operation only when the output voltages are greater than the utility voltage and thus, this topology is not considered further.

The conventional buck-boost type DC-DC converter (single-switch topology) has also been omitted because the main current flowing through the inductor is higher than that of the boost and buck types and therefore it results in a greater size, weight, cost and losses in the inductor. Additionally, it has been pointed out in published papers [3]-[5] that the buck and boost cascade topologies with one dc-inductor, shared by the buck and boost parts, is desirable compared with the conventional buck-boost topology when a wide output voltage range with a high efficiency is required. The proposed topology (i.e., 3-phase buck PFC with 2 independent dc-dc converters ("Buck+Series-Boost")) is in the category. Three-level topologies [2] are also omitted because the upper and lower voltages can be imbalanced in this application since the output powers of the two dc-dc converters are not always the same.

III. OPERATION OF "BUCK+SERIES-BOOST" TOPOLOGY

The "Buck+Series-Boost" topology, as shown in Fig. 1, has a unique feature in its operation since the output current of the PFC rectifier and the input currents of the two dc-dc converters (Conv.-1 and -2) are common (i.e., they are all i_{DC}). This feature is the key and the hint to analyze the possible operation in order to satisfy all the requirements and to obtain a superior control scheme.

Since the "Buck+Series-Boost" is a buck and boost cascade system, requirement 1 (wide U_1 and U_2 control range) is satisfied. By controlling the PFC output voltage, U_{PFC}, to be zero and turning both switches S_1 and S_2 ON, requirement 2 (i.e., $U_1 = U_2 = 0$) is satisfied. When one switch (S_1 for example) remains in the ON-state and the other switch (S_2) remains in OFF-state, the PFC output voltage U_{PFC} equals the output voltage (U_2) of the converter (Conv.-2) with the OFF-state switch (S_2). Thus, the output voltage (U_2) is controlled by the PFC rectifier but only in the buck operating region. With this condition, the output voltage (U_1) of the converter (Conv.-1) with the ON-state switch (S_1) remains at zero. Hence, requirement 3 is satisfied. It must be noted that this condition is achieved without any PWM switching of the switches S_1 and S_2, and therefore requirement 6 is also satisfied. This is one of the key features of the proposed "Buck+Series-Boost" topology since such a load condition occurs often in the particular heating application.

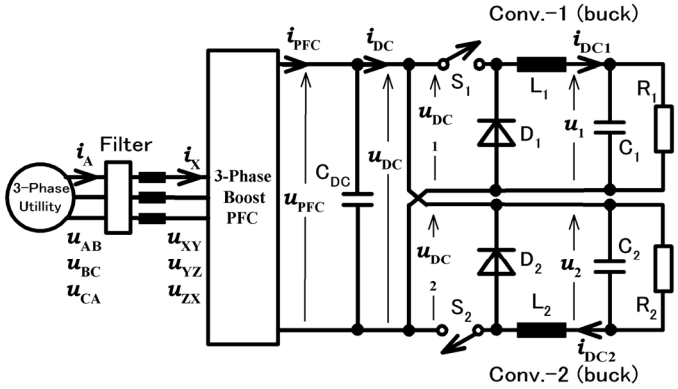


Figure 2. Alternative Topology.
(3-Phase Boost PFC + Parallel Buck DC-DC Converters)

In this topology, the PFC output current i_{DC} (or the input current of the boost dc-dc converters) is fed to the output load (R_1 or R_2) or bypassed depending on whether the switch (S_1 or S_2) is in the OFF-state or ON-state, respectively. Thus, the average of the output current (I_{R1} or I_{R2}) can be controlled to be equal to or less than the input current I_{DC} by using PWM operation of the dc-dc converter with an appropriate PWM index (i.e., Duty-Cycle) λ_{PWM}. That is,

$$I_{R1} = (1 - \lambda_{PWM\text{-}1})\, I_{DC},\ \ I_{R2} = (1 - \lambda_{PWM\text{-}2})\, I_{DC}, \qquad (1)$$

where $\lambda_{PWM\text{-}1}$ and $\lambda_{PWM\text{-}2}$ are the ON-Duty cycle of the two switches S_1 and S_2 respectively and

$$0 \le \lambda_{PWM\text{-}1} \le 1,\ \ 0 \le \lambda_{PWM\text{-}2} \le 1 \qquad (2)$$

The common input current I_{DC} is controlled by the PFC rectifier and the influence from the dc-dc converter operation on the current can be canceled by the PFC control. Thus, the two dc-dc converters can feed output currents (I_{R1} and I_{R2}) with a range from zero to the common input current I_{DC}. Since the output current of the buck PFC rectifier has no theoretical limitation in the amplitude, the output currents of the dc-dc converters have no theoretical limitation in the amplitude too. Hence, the dc-dc converters offer independent control of the output currents and thus allow the output voltages to have a wide range. Therefore, the new topology satisfies requirement 4.

In the above-mentioned condition, the PFC rectifier can control the output current I_{DC} to be equal or greater than one of the two dc-dc converter output currents. In this particular condition, the switch (S_1, for example) of the dc-dc converter (Conv.-1) with the greater output current (I_{R1}) can remain in OFF-state (i.e., $\lambda_{PWM\text{-}1} = 0$ and thus, $I_{R1} = I_{DC}$; from (1)) while the other switch (S_2) operates with PWM to control the output current (I_{R2}) in the range between zero and I_{DC}. This condition is identical to that of requirement 5.

The number of required passive components of the "Buck+Series-Boost" is less compared with "Boost+Parallel-Buck," as can be seen from Fig. 1 and 2.

IV. CONTROL AND PWM STRATEGY

The control and PWM strategy of the new 3-phase Buck PFC rectifier and two series-connected boost dc-dc converters cascade system is described in this section. Fig. 3 shows the control system.

The controlled values are the two output voltages u_1 and u_2 of the dc-dc converters and thus, the output voltages are detected and compared with references u_1* and u_2*, respectively, and control errors Δu_1 and Δu_2 are obtained. The errors are fed to a PI-Controller (only a P-type controller has been utilized in the simulation and experimental hardware) and the reference values i_{C1}* and i_{C2}* of the dc-capacitor currents are obtained. By adding the detected load current i_{R1} or i_{R2} and the reference i_{C1}* or i_{C2}*, we obtain the reference i_{DC1}* or i_{DC2}* of the dc-dc converter output currents which should flow through the diode D_1 or D_2, respectively. The references i_{DC1}* or i_{DC2}* are then multiplied by the detected output voltages u_1 or u_2, respectively, and the references p_{DC1}* or p_{DC2}* of the dc-dc converter output power are obtained. By summing the two reference powers, a reference $p_{DC\text{-}TOT}$* which represents the total output power (and is approximately equal to the output power of the PFC rectifier) is determined. As mentioned, the PFC rectifier needs to feed an output current i_{DC} that is equal to or greater than the largest output current (i_{R1} or i_{R2}) of the dc-dc converters (i.e., $i_{DC} \geq \text{MAX}[i_{DC1}, i_{DC2}]$). Additionally, a Unity-PWM-Index (UPI) condition (i.e., non-PWM operation) is achieved and requirements 4 and 5 are satisfied if the PFC output current is identical to the largest of the two output currents of the dc-dc converters. Thus, the reference u_{DC}*, which represents the sum of the two dc-dc converters' input voltages in order to achieve the UPI condition, is obtained by dividing the total power reference $p_{DC\text{-}TOT}$* by the largest dc-dc converter output current (i.e., $u_{DC}^* = p_{DC\text{-}TOT}^*/i_{DC}^* = p_{DC\text{-}TOT}^*/\text{MAX}[i_{DC1}^*, i_{DC2}^*]$). Since a dividing function now exists in the controller in order to obtain the reference u_{DC}*, the reference can exceed an acceptable value and the PFC operation could become unstable under severe transient and/or start-up conditions. To avoid this, a saturation function is applied to the original reference u_{DC}*, and the modified reference $u_{DC\text{-}LIM}$* is then obtained.

The reference i_{DC}* for the PFC output current (i.e., dc-dc converter input current) is obtained by dividing the total power reference $p_{DC\text{-}TOT}$* by the modified reference $u_{DC\text{-}LIM}$*. By comparing the reference i_{DC}* with the detected dc-current i_{DC}, an error Δi_{DC}* of the dc-current is obtained. The error is fed to a PI-Controller (only a P-type controller is utilized in the simulation and experimental hardware) and a reference u_{LD}* of the dc-inductor voltage is calculated. By subtracting this reference u_{LD}* from the modified reference $u_{DC\text{-}LIM}$* of the PFC output voltage, the reference u_S* is obtained. This reference is the reference for the local-average of the sum of the voltages across the boost converter switches, $u_S^* = u_{S1}^* + u_{S2}^*$. The u_S* is multiplied by the index α_1^* or α_2^* and references u_{S1}* and u_{S2}* are obtained, respectively.

For determining α_1* or α_2* each of the output power references p_{DC1}* and p_{DC2}* of the dc-dc converters is divided by the power reference $p_{DC\text{-}TOT}$*. The indexes represent the ratio between the voltages of the input and output (i.e., u_{S1}/u_1 or u_{S2}/u_2) or currents of the output and input (i.e., i_{R1}/i_{DC} or i_{R2}/i_{DC}), respectively, where the sum of the two indexes is unity. By comparing the references u_{S1}* or u_{S2}* of the boost stage switch voltages with the detected output voltage u_1 or u_2, the PWM index $\lambda_{PWM\text{-}1}$* or $\lambda_{PWM\text{-}2}$* for the dc-dc boost converter is determined. In a steady-state condition with no error in the output voltages and in the dc-current, the PWM index of the dc-dc converter with the largest output current reaches unity (i.e., achieving a UPI condition) and the switch remains continuously OFF and therefore the switching losses are eliminated in that dc-dc converter by means of the

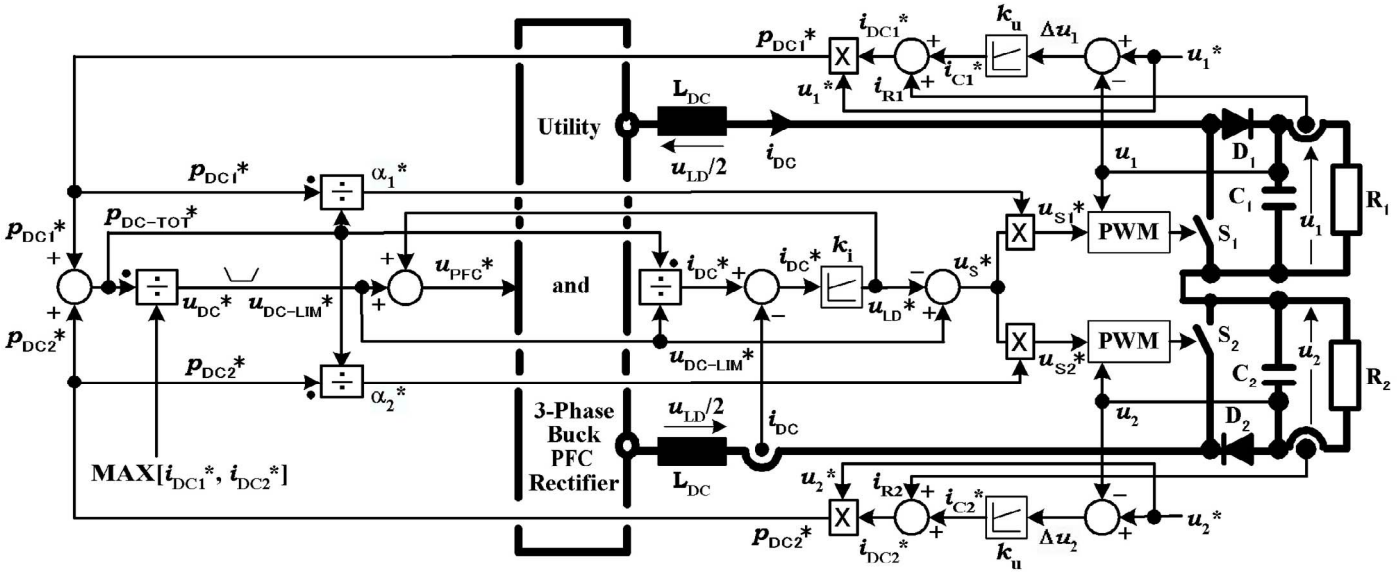


Figure 3. Control System for Proposed "Buck+Series-Boost" Topology.

proposed control strategy.

For controlling the i_{DC} in case the boost converter stage is operating in a modulation limit, the u_{LD}* must also be added to the modified reference $u_{DC\text{-}LIM}$* to obtain the reference u_{PFC}* of the PFC output voltage. This reference u_{PFC}* is fed to the PFC controller that determines the rectifier modulation patterns [3].

V. Simulation Study

The validity of the theory and practicability of the new converter system has been confirmed through a simulation study. TABLE I gives the system parameters and circuit conditions used in the PSIM simulation. The simulation is conducted for two different operating conditions. Figs. 4 and 5 show the operating waveforms where the output voltage reference of one converter is rapidly changed from 80 to 120V while that of the other converter remains at 80V.

A. Case-A: Step-Change of the Non-UPI Converter Reference

As seen in Fig. 4(a) and (b), the output voltage reference u_1* remains in at a constant value of 80V while the output voltage reference u_2* has a step-change from 80 to 120V at time t_A.

i) Steady-State Performance

Before and after the step-change of the reference u_1* (i.e., $t < t_A$) and $t >> t_A$), the converter system is operating in steady-state where the output voltages u_1 and u_2 agree with the references u_1* and u_2*, respectively, as seen in Fig. 4(a) and (b).

The switch voltages u_{S1} and u_{S2} in Fig. 4(a) and (b) show that the switch S_1 operates with high-frequency switching and that Conv.-1 remains in non-UPI operation (i.e., PWM operation) while switch S_2 remains in the OFF state and the Conv.-2 is in UPI operation.

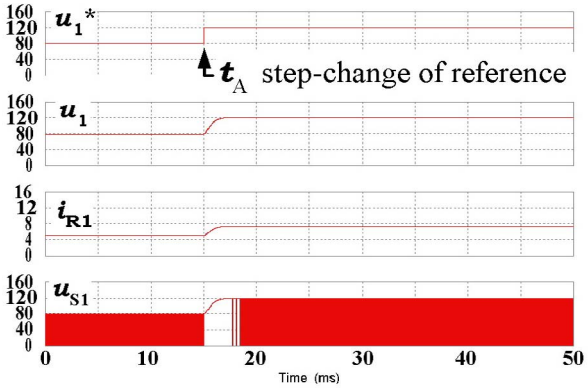
As seen in Fig. 4(c), the dc-voltage reference $u_{DC\text{-}LIM}$* and the PFC output voltage reference u_{PFC}* are almost the same since the voltage drop of the dc-inductor L_{DC} in steady-state is almost zero. The low-frequency components (or local-average) $u_{PFC\text{-}LF}$ of the PFC output voltage (obtained by applying a low-pass filter to the output voltage u_{PFC}) follows the reference u_{PFC}* very well as seen from their waveforms in Fig. 4(c).

Fig. 4(d) shows that the input currents of the buck rectifier offer 3-phase symmetrical sinusoidal waveforms with almost no distortion and they are in phase with the utility phase voltages.

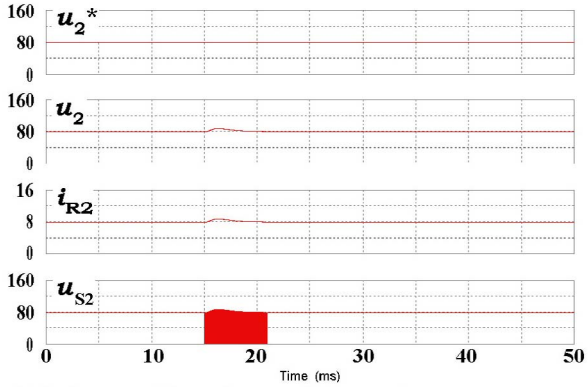
From the waveforms, it is shown that the proposed power converter system offers a good steady-state performance with

TABLE I
Simulations and Experimental System Parameters

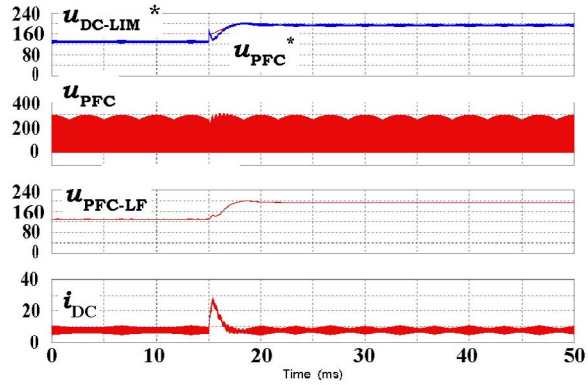
Utility Phase-Voltage U_{UTIL}	120 V_{RMS}
Filter Inductors L_F	200 µH
Filter Capacitors C_F	20 µF
DC Smoothing Inductor L_{DC} (total of upper and lower ones)	500 µH
DC Smoothing Capacitor C_1 and C_2	500 µF
Load Resistors R_1 and R_2	16 and 10 Ω
PWM/Switching Frequency f_{PWM}	20 kHz



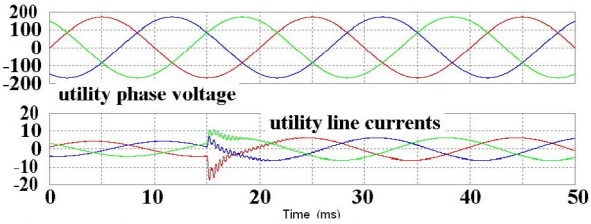
(a) Reference of Conv.-1 output Voltage u_1*, Output voltage of Conv.-1 u_1, Output current of Conv.-1 i_{R1} and Switch S_1 Voltage u_{S1}.



(b) Reference of Conv.-2 output Voltage u_2*, Output voltage of Conv.-2 u_1, Output current of Conv.-1 i_{R2} and Switch S_2 voltage u_{S2}.



(c) Reference of DC-Intermediate Voltage $u_{DC\text{-}LIM}$ *, Reference of PFC Output Voltage u_{Rec}*, PFC Output Voltage u_{RFC}*, Its Low-Freq. Components (i.e., local-average) $u_{REC\text{-}LF}$ and DC-Intermediate Current i_{DC}.



(d) Utility Phase Voltages And Currents.

Figure 4. Simulation Results: Case-A (Step-Change of Conv.-1 Ref. u_1*).

the UPI operating method as discussed in the previous section.

ii) Transient Response

Just after the step-change of the reference u_1* at time t_A, the output voltage u_1 of the Conv.-1 follows the step-change of the reference with a short delay of 4ms and without any overshoot while the output voltage u_2 of the Conv.-2 increases slightly but it returns to its stable value of 80V in a short time of approx. 4 ms, as seen in Fig. 4(a) and (b) respectively.

The waveforms of the switch voltages u_{S1} (Fig. 4(a)) and u_{S2} (Fig. 4(b)) show that the switch S_1 alternates between the UPI and non-UPI condition while switch S_2 remains in the non-UPI condition during the transient period.

Since the demand of dc-dc converter input voltage sum increases due to the reference step-change, both the references $u_{DC\text{-}LIM}$* of the dc intermediate voltage and u_{PFC}* of the PFC output voltage increase during in the transient time as seen in Fig. 4(c). The references $u_{DC\text{-}LIM}$* and u_{PFC}* are slightly different during the transient condition because the dc-current i_{DC} (shown in Fig. 4(c)) rapidly increases just after the reference step-change and the dc-inductor L_{DC} has a small voltage drop.

The utility currents (i_A, i_B and i_C, shown in Fig. 4(d)) rapidly increase in amplitude just after the reference step-change and they reach the new steady-state condition, i.e., 3-phase symmetrical sinusoidal waveforms with higher amplitude, within a half cycle of the fundamental frequency.

This simulation result shows that the proposed converter system offers a good transient response.

B. Case-B: Step-Change of the UPI Converter Reference

As seen in Fig. 5, the proposed system also has a good performance for Case-B under both steady-state and transient conditions.

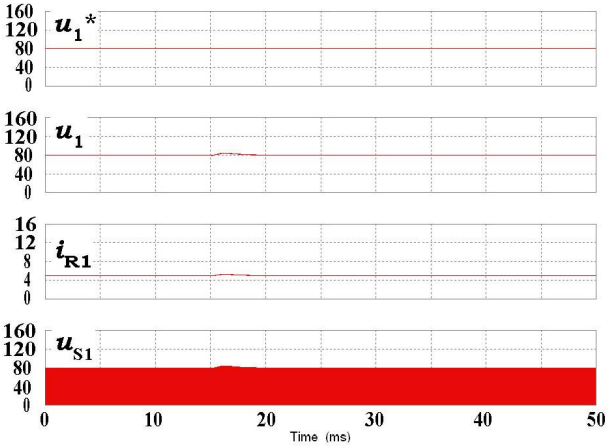
VI. Experimental Verification

A prototype converter based on the new topology and control strategy has been constructed with the system parameters given in TABLE I. A step-change of the output voltage references are arranged to be the same as those in the simulations. Figs. 6 and 7 show operating waveforms for the step-change of the output voltage reference u_1* and u_2* of the Conv.-1 and Conv.-2, respectively.

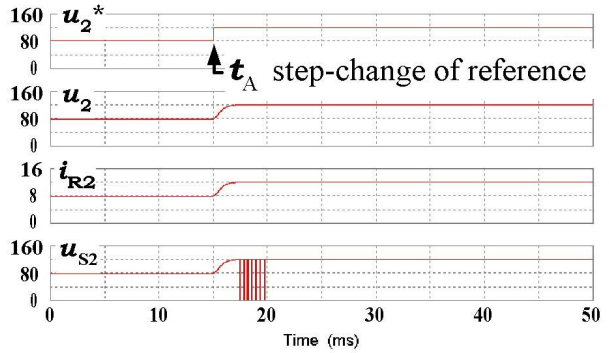
A. Case-A: Step-Change of Non-UPI Converter Reference

i) Steady-State Performance

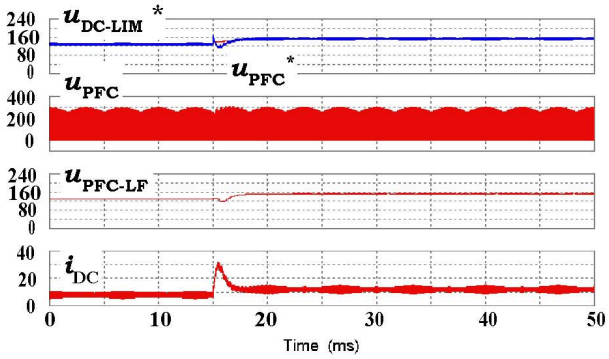
The experimental waveforms in Fig. 6 have virtually the same steady-state performance as given in the simulation results. The only difference between the waveforms occurs in the utility current. That is, the current waveforms from the experiment produce a larger current peak during the transient than predicted by simulation. This is caused by the dynamic change in the dc link current and an overshoot of the weakly damped input filter in the experimental hardware which do not appear in the simulation results due to the idea nature of the simulation.



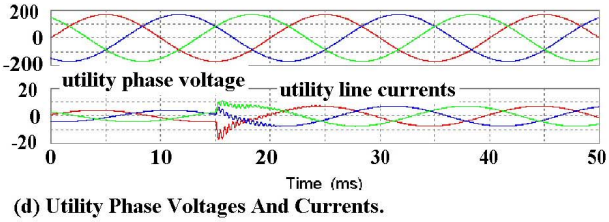
(a) Reference of Conv.-1 output Voltage u_1*, Output voltage of Conv.-1 u_1, Output current of Conv.-1 i_{R1} and Switch S_1 Voltage u_{S1}.



(b) Reference of Conv.-2 output Voltage u_2*, Output voltage of Conv.-2 u_1, Output current of Conv.-1 i_{R2} and Switch S_2 voltage u_{S2}.

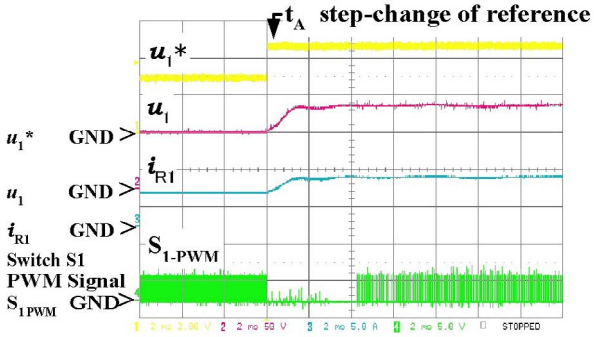


(c) Reference of DC-Intermediate Voltage $u_{DC\text{-}LIM}$ *, Reference of PFC Output Voltage u_{Rec}*, PFC Output Voltage u_{RFC}*, Its Low-Freq. Components (i.e., local-average) $u_{REC\text{-}LF}$ and DC-Intermediate Current i_{DC}.

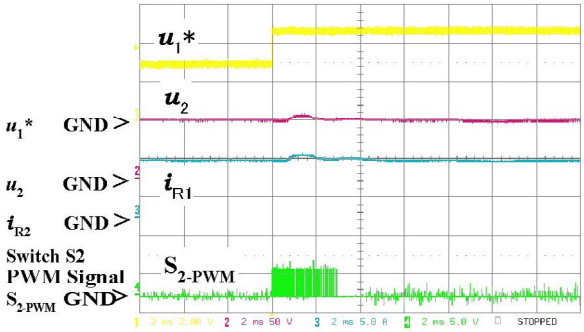


(d) Utility Phase Voltages And Currents.

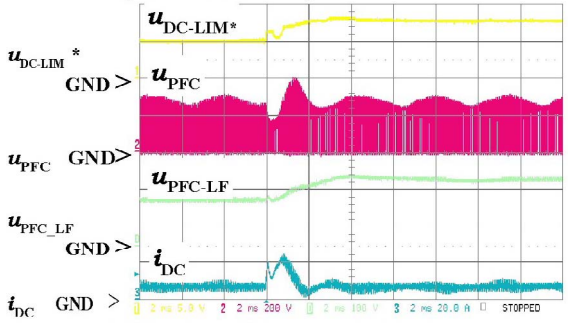
Figure 5. Simulation Results: Case-B (Step-Change of Conv.-2 Ref. u_2*).



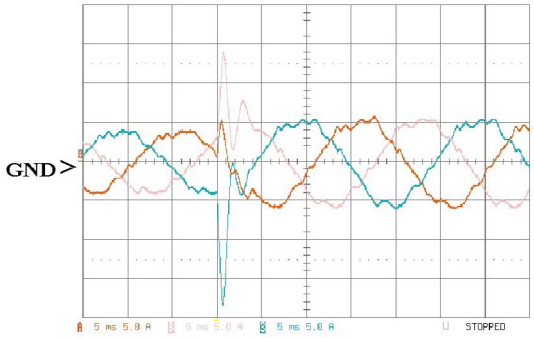
(a) Reference of Conv.-1 output Voltage u_1*,
Output Voltage of Conv.-1 u_1 (50V/div),
Output Current of Conv.-1 i_{R1} (5A/div) and
Switch S_1 ON/OFF Signal.
(Time-Scale: 2ms/div)



(b) Reference of Conv.-1 output Voltage u_1*,
Output voltage of Conv.-2 u_2 (50V/div),
Output current of Conv.-2 i_{R2} (5A/div) and
Switch S_2 ON/OFF Signal.
(Time-Scale: 2ms/div)

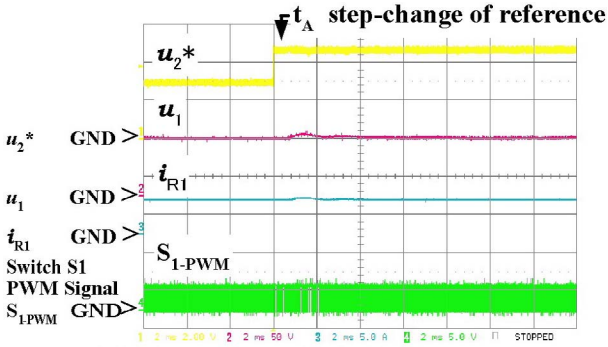


(c) DC voltage reference $u_{DC\text{-}LIM}$ *,
PFC output voltage u_{PFC} (200V/div),
Low-Frequency Components (or Local-Average) of
PFC output Voltage u_{PFC_LF} (100V/div) and
DC Current i_{DC} (20A/div).
(Time-Scale: 2ms/div)

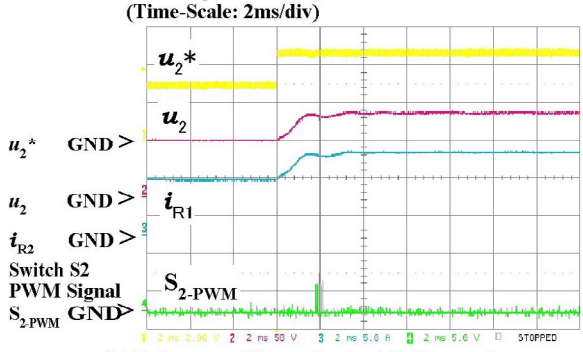


(d) Utility Line Currents (5A/div) . (Time-Scale: 2ms/div)

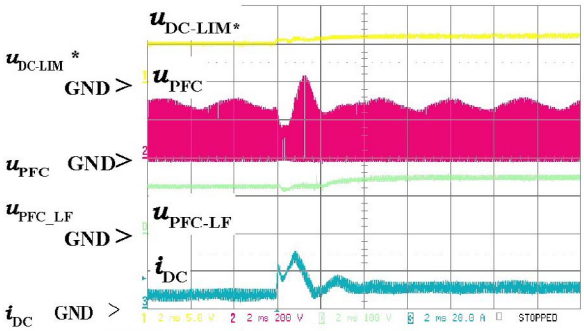
Figure 6. Experimental Res.: Case-A: Step-Change Conv.1 Ref. u_1*



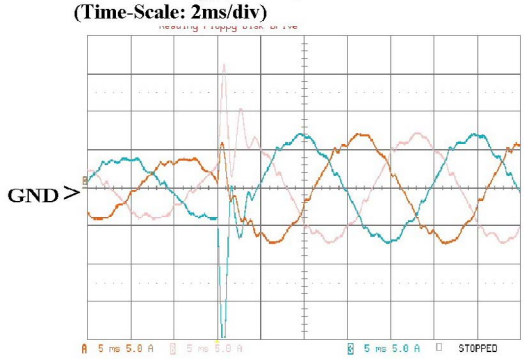
(a) Reference of Conv.-1 output Voltage u_1*,
Output Voltage of Conv.-1 u_1 (50V/div),
Output Current of Conv.-1 i_{R1} (5A/div) and
Switch S_1 ON/OFF Signal.
(Time-Scale: 2ms/div)



(b) Reference of Conv.-2 output Voltage u_2*,
Output voltage of Conv.-2 u_2 (50V/div),
Output current of Conv.-2 i_{R2} (5A/div) and
Switch S_2 ON/OFF Signal.
(Time-Scale: 2ms/div)



(c) DC voltage reference $u_{DC\text{-}LIM}$ *,
PFC output voltage u_{PFC} (200V/div),
Low-Frequency Components (or Local-Average) of
PFC output Voltage u_{PFC_LF} (100V/div) and
DC Current i_{DC} (20A/div).
(Time-Scale: 2ms/div)



(d) Utility Line Currents (5A/div). (Time-Scale: 2ms/div)

Figure 7. Experimental Res.:Case-B: Step-Change of Conv.2 Ref. u_2*

From the experiments, it is know that the proposed power converter system offers a sufficient steady-state performance with UPI operation as discussed in the previous section.

ii) Transient Response

The response of the two output voltages u_1 and u_2 of the dc-dc converters in the experiments is almost the same to those in the simulation. That is, the output voltage u_2 follows the step-change of the reference rapidly and it reaches the new reference value of 120V within a short time of 4 ms without any over shoot, while the output voltage u_2 increases slightly just after the step-change of the reference but it returns to the stable value of 80V in a short time of 4 ms.

The waveforms of the switch voltages u_{S1} and u_{S2} show that the switch S_1 of the Conv.-1 remains in the UPI condition while the switch S_2 of Conv.-2 remains in the non-UPI condition during in the transient period.

From the waveforms of u_{PFC} and i_{DC} shown in Fig.6(c) and utility current waveforms shown in Fig. 6(d), it is known that the experimental system has larger transients than in the simulations. This is also caused by the sensitivity of RLC network in 3-phase input (including the utility) to step-changes in the utility current. Therefore the utility currents contain an oscillation and thus, amplitude of the PMW voltage u_{PFC} and i_{DC} also have oscillations. Since these results are produced from the first experiments of the new topology, the phenomenon, which are typical for a Buck PFC due to the LC input filter, will be analyzed and the transient performance of the utility current will be improved.

B. Case-B: Step-Change of UPI Converter Reference

The waveforms shown in Fig. 7 are almost the same as those for Case-A shown in Fig. 6, except for the magnitude of the utility current oscillation. The oscillation in this Case-B is slightly larger than that of the Case-A since the difference between the load powers before and after the transient is greater. From the experimental results, the prototype offers a reasonable transient response even though the current oscillation requires further damping.

VII. CONCLUSIONS

A new 3-phase buck-boost unity power factor rectifier consisting of 3-phase bridge-type buck PFC rectifier and two boost dc-dc converters connected directly in series is proposed for an industrial application where two independently controlled heater loads must be supplied. The proposed topology is briefly compared with other candidate topologies and it is shown that only the proposed topology satisfies all the operational requirements. The unique operating modes for the two independent loads and the developed control strategy are described in detail. The validity of the theory is confirmed through simulation studies and experimental results. The simulation and experimental results are well matched except for a larger oscillation in the input voltages and currents of the PFC in the experiment hardware. The 3-phase buck PFC plus two series connected boost converters allows the two independent output voltages to be controlled and results in a reduction in switching losses due to the implementation of a unity-PWM-index for one converter.

In the course of further research a control oriented model of the system will be derived. There special attention will be on the mutual coupling of the two series connected boost stages and a decoupling control. Furthermore, the EMC input filter transfer function will be included into the converter control model and an active damping scheme will be implemented.

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