Novel Three-Phase AC–AC Sparse Matrix Converters

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***Abstract*—A novel three-phase ac-ac sparse matrix converter having no energy storage elements and employing only 15 IGBTs, as opposed to 18 IGBTs of a functionally equivalent conventional ac-ac matrix converter, is proposed. It is shown that the realization effort could be further reduced to only nine IGBTs in an ultra sparse matrix converter (USMC) in the case where only unidirectional power flow is required and the fundamental phase displacement at the input and at the output is limited to $\pm\pi/6$. The dependency of the voltage and current transfer ratios of the sparse matrix converters on the operating parameters is analyzed and a space vector modulation scheme is described in combination with a zero current commutation method. Finally, the sparse matrix concept is verified by simulation and experimentally using a 6.8-kW/400-V very sparse matrix converter, which is implemented with 12 IGBT switches, and USMC prototypes.**

***Index Terms*—Ac-ac converter, matrix converter, reduced switch count converter, sparse matrix.**

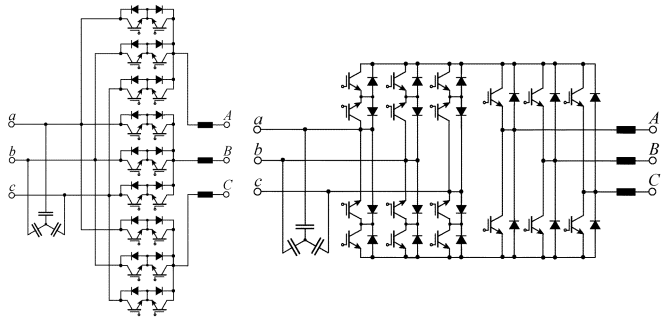

Fig. 1. (a) Conventional matrix converter with common emitter (CE) power transistor connection; a common collector (CC) connection reduces the number of isolated gate power supplies from 9 to 6 (cf. Table I) [7], [8]. (b) Indirect matrix converter as proposed in [9] and analyzed in [10].

I. Introduction

THREE-PHASE matrix converters are capable of providing simultaneous amplitude and frequency transformation of a three-phase voltage system and only require small switching frequency ac filter components compared to conventional two-stage ac/dc/ac conversion from the back-to-back connection of voltage dc-link PWM converter (BBC) systems [1]. Furthermore, matrix converters are inherently bidirectional and therefore can regenerate energy back into the mains from the load side. The mains side current is sinusoidal and the mains displacement factor can be adjusted, by proper modulation, irrespective of the type of load. Consequently, matrix converters show a high power density and a potentially high reliability since electrolytic capacitors are not required. Accordingly, there is considerable interest in the application of matrix converters for the realization of highly compact three-phase ac drives [2], [3] for industrial and military marine and avionics systems.

A conventional matrix converter (CMC) utilizes nine bidirectional, bipolar (four-quadrant) switches that, when based on available power semiconductor technology, are constructed using 18 unipolar turn-off power semiconductors (IGBTs) and 18 diodes, as shown in Fig. 1(a). The combination of two IGBTs and two anti-parallel diodes per four-quadrant switch allows for a selective turn-on of the switch in each current direction, which is a requirement to implement a safe multistep commutation strategy. This strategy avoids the short circuiting of an input line-to-line voltage or an abrupt interruption of an output phase current [1], [4].

Research on the matrix converter has mainly focused on modulation schemes and the digital generation of the PWM switching patterns [1], [5], [6]. The derivation of alternative topologies that exhibit identical functionality but utilize a reduced number of unipolar turnoff power semiconductors has not received much attention.

In this paper, novel matrix-equivalent three-phase ac-dc-ac converter topologies are developed based on the structure of an indirect matrix converter (IMC), shown in Fig. 1(b), which has been proposed in [9]. The converter topologies, presented in Section II, exhibit a reduced number of power transistors compared to the CMC or IMC and are therefore designated as the *sparse matrix converter* (SMC) and/or *ultra sparse matrix converter* (USMC). In Section III, a safe multistep commutation concept for the SMC is considered and a zero-current commutation method, featuring low complexity, is described. In Section IV, a space-vector modulation scheme is proposed, which inherently provides zero current commutation and ohmic fundamental (unity power factor) mains behavior. Furthermore, in Section V the operating range of the SMC and USMC is analyzed and the dependency of the current and voltage transfer ratio on the phase displacement of fundamental voltage and current at the input and at the output side is clarified. Section VI presents experimental results from a 6.8 kW *very sparse matrix converter* (VSMC) and a USMC.

II. Derivation of the SMC Topology

In this section, the derivation of the SMC circuit topology and the equivalence of the SMC to the CMC, concerning con-

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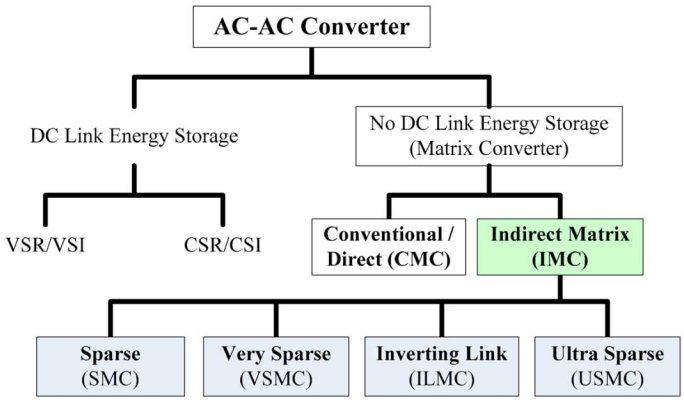

Fig. 2. Classification of ac-ac converter topologies.

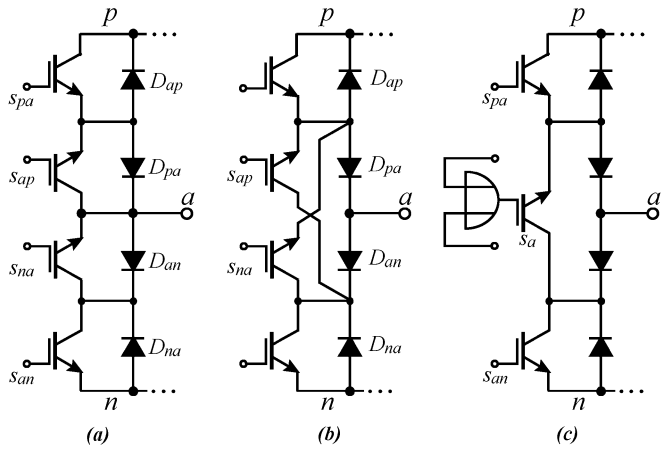

Fig. 3. Modification of the (a) IMC input-stage bridge leg structure of Fig. 1(b) into the (c) SMC bridge leg structure of Fig. 4(a).

TABLE I
REALIZATION EFFORT OF DIFFERENT MATRIX CONVERTER TOPOLOGIES

Converter Type	Transistors	Diodes	Isolated Driver Potentials
CMC	18	18	6 (CC), 9 (CE)
IMC	18	18	8
SMC	15	18	7
VSMC	12	30	10
USMC	9	18	7

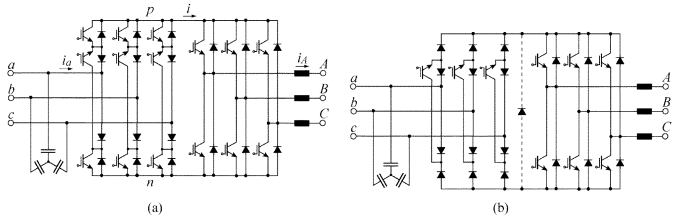

Fig. 4. Proposed matrix converter topologies: (a) SMC and (b) USMC.

trollability and/or modulation range, are treated. The topology of the CMC is shown in Fig. 1(a) where, with reference to a three-phase ac motor drive application, the converter input voltages and the output currents are assumed to be impressed. Modulation schemes for the CMC, as given in the literature, can be classified into direct frequency-conversion schemes [11], [12] and indirect frequency-conversion schemes [4], [13]. For the indirect frequency-conversion scheme, the CMC is fictitiously divided into a voltage-fed rectifier input stage and an inverter output stage with impressed output currents, which are directly connected on the dc side. The physical implementation of this basic idea results in the converter topology depicted in Fig. 1(b), [9], which is functionally equivalent to a CMC and is denoted as the indirect matrix converter (IMC) in Fig. 2.

For the IMC, a conventional (two-quadrant switch) voltage-source-type inverter is fed by a four-quadrant switch, current-source-type rectifier, which is able to operate with a positive *and* negative dc current for a *unipolar* dc-link voltage as required by the inverter stage. The input capacitor of the inverter is effectively realized by the ac-side (voltage impressing) filter capacitors of the rectifier stage and the output inductor of the rectifier is realized by the current-impressing inductance of the load. The IMC employs 18 unipolar turn-off power semiconductors and 18 diodes (cf. Table I) and therefore has basically the same realization effort as the CMC. However, the inverter stage could be implemented with a conventional six-pack power module and, therefore, this would slightly reduce the realization effort compared to a fully discrete CMC.

The dc-link voltage of the IMC must have a fixed polarity, but the IMC four-quadrant switch current-source-type rectifier is capable of operating with both positive and negative dc-link voltage polarities. Therefore, ways of reducing the rectifier stage circuit complexity are now considered and the reduction in the number of unipolar turn-off power semiconductors is verified step-by-step in Fig. 3 for a single bridge leg.

When $s_{pa}, s_{ap} = 1$ (where a switching function of $s_i = 1$ denotes an on-state of the corresponding power transistor S_i, while s_i =0 denotes an off-state) for the bridge leg topology, in Fig. 3(a), this means that the input a is connected bidirectionally to p. For the case of a positive dc-link voltage $(u_{pn} > 0)$, the transistor S_{an} is blocking voltage, while for a voltage of $u_{pn} < 0$ the blocking is taken over by S_{na} during the on-interval of S_{ap}. By restricting the operation to $u_{pn} > 0$, the blocking action of S_{na} is not required. Therefore, S_{na} in case of $s_{an}, s_{na} = 1$ only has to provide a path for a current flowing via the negative rail and D_{na} back to terminal a. This can be achieved without directly connecting the Emitter of S_{na} to a, i.e., the emitter of S_{na} also could be tied to the anode of diode D_{pa}, which then would guide the current back to a. An analogous consideration for switch S_{ap} leads to the possibility of connecting the collector of S_{ap} to the cathode of diode D_{an}. As a result, S_{na} and S_{ap} could be connected in parallel and/or can be combined into a single transistor S_a [cf. Fig. 3(b)], which is turned on for the connection of a to p *and* for the connection of a to n. The resulting bridge leg topology [cf. Fig. 3(c), [14], [15]] for $u_{pn} > 0$ still provides independent controllability in both current directions as required for the implementation of a safe commutation strategy [1]. Consequently, for $u_{pn} > 0$ the functionality of the IMC and/or CMC can be realized by the converter topology depicted in Fig. 4(a). This topology employs only 15 IGBTs, compared to 18 IGBTs of the IMC, and therefore the converter topology is designated as *Sparse Matrix Converter* (SMC).

The functional equivalence of the CMC/IMC and SMC is proven in [16], where the CMC and SMC line-to-line output voltages and input phase currents resulting for the different switching state combinations are compiled. The controllability and the operating range of the SMC are not restricted despite the reduced number of unipolar turn-off power semiconductors and as a result the SMC represents a highly interesting alternative to the CMC for industrial applications.

If the functionality of a unidirectional buck-type PWM rectifier system, as described in [17] and [18], is desired, then the realization effort of the SMC can be reduced by omitting the power transistors S_{pi} and S_{in} in each bridge leg (i) as they allow for the reverse flow of the dc-link current. This removal of the switches restricts the circuit operation to a unidirectional power flow $(u_{pn} > 0, i > 0)$ and the controllability of the phase displacement of input voltage and input current fundamental is limited to $\pm\pi/6$, while the phase displacement of load current and load voltage fundamental is not allowed to exceed $\pm\pi/6$. Due to the lower number of power transistors (nine IGBTs), this circuit topology is designated the USMC.

III. Commutation Scheme

A. Multistep Commutation

For a given switching state of the rectifier input stage, the commutation of the inverter output stage has to be performed in an identical manner to the commutation of a conventional voltage dc-link converter, where a dead time between the turn-off and turn-on of the power transistors of a bridge leg has to be implemented in order to avoid a short circuit of the dc-link voltage. To change the switching state of the SMC rectifier input stage for a given inverter switching state, one has to ensure that there is no bidirectional connection between any two input lines, i.e., no short-circuiting of an input line-to-line voltage occurs. Additionally a current path must be continuously provided. Therefore multistep commutation schemes, using voltage independent and current independent commutation as is known for the CMC [1], can be employed (cf. Fig. 5). Both commutation strategies have been analyzed extensively in the literature (cf. e.g., [19]–[21]), and therefore a detailed description is omitted for the sake of brevity.

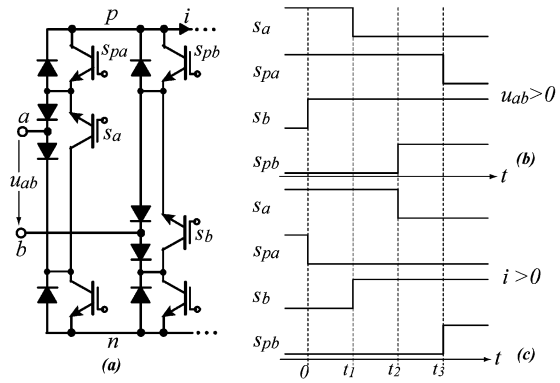

Fig. 5. Multistep commutation of the SMC rectifier input stage. (a) Basic structure of the commutating bridge legs. Switch sequence to change the connection of the positive dc-link voltage bus p from input a to input b. (b) Current-independent commutation assuming $u_{ab} > 0$. (c) Voltage-independent commutation assuming $i > 0$.

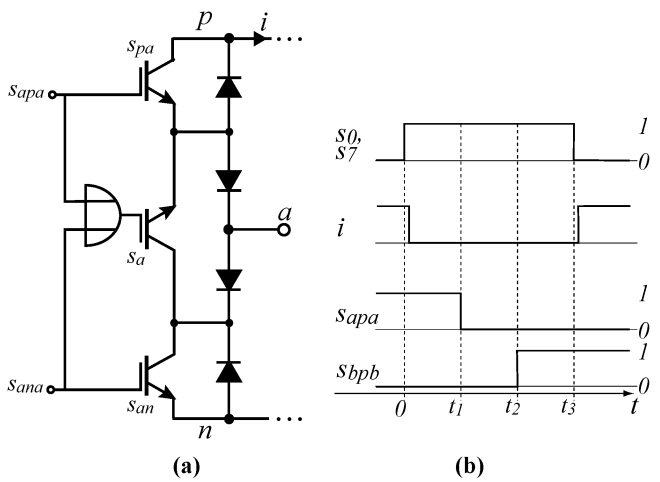

Fig. 6. Zero current commutation of indirect matrix converter topologies shown for the SMC. (a) Control of the power transistors in a bridge leg of the SMC. (b) Switching state sequence ($s_0, s_7 = 1$ indicates free-wheeling operation of the inverter stage) and dc-link current i to change the connection of the positive dc-link voltage bus p from input a to input b.

B. Zero dc-Link Current Commutation

The obvious drawback of the multistep commutation methods is the complexity. However, indirect matrix converters provide a degree of control freedom that is not available for the CMC and can be used to alleviate the complex commutation problem. As proposed in [22], the inverter stage could be switched into a free-wheeling state and then the rectifier stage could commutate with zero dc-link current (cf. Fig. 6). This has the added benefit of a reduction in the switching losses of the input stage. One only has to ensure that no overlapping of turn-on intervals of power transistors in a bridge half occurs, which would result in a short circuit of an input line-to-line voltage. It is interesting to note that by employing the zero dc-link current commutation strategy the topology of the IMC could be reduced to the circuit structure shown in Fig. 7(a), which is designated as the *very sparse matrix converter* (VSMC) [23], [24] since it has only 12 IGBTs.

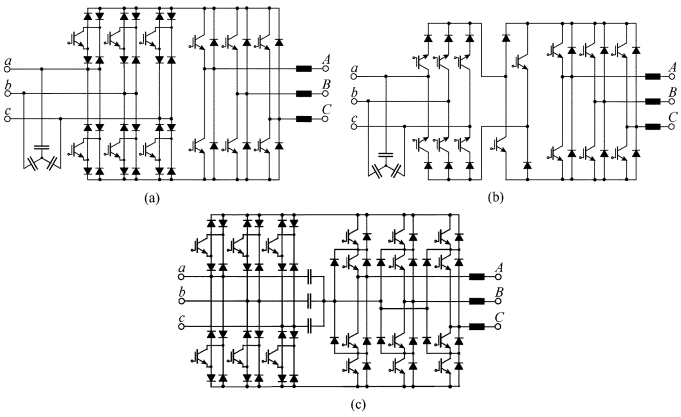

Fig. 7. Topology of the (a) VSMC, (b) ILMC, and the (c) SMC3.

Zero dc-link current commutation also allows for the circuit topology shown in Fig. 7(b) to be utilized for three-phase

ac-ac power conversion. The bidirectional current carrying capability of the input stage is achieved by combining a conventional current dc-link rectifier and a voltage and/or current inverting switching section, which is formed by two power transistors and two diodes [25]. Accordingly, this converter is designated as the *inverting link matrix converter* (ILMC). Compared to the SMC, the ILMC has a similar number of power transistors, however the inversion of the inverter output stage input current has to be performed at the switching frequency when the phase displacement of load current and load voltage fundamental is greater than $\pm\pi/6$. This results in higher switching losses and increased control complexity, therefore the ILMC is not further considered in this paper. In addition, the input stage of any SMC can be connected to a three-level voltage dc-link inverter output stage (SMC3), as shown in Fig. 7(c) where in this case the input stage is from a VSMC [Fig. 7(a)]. The mid point of the three-level inverter is connected to the star point formed by the input ac filter capacitors. A reduced switch count version of a three-level indirect matrix converter has been recently proposed by Klumpner [26]. A three-level output voltage can also be obtained from the conventional IMC by using a three-level output voltage modulation method [Fig. 12(c)].

For the USMC, since the dc-link current has to always be positive $(i > 0)$, therefore the commutation can be performed irrespective of the switching state of the output stage when a free-wheeling diode is provided in the dc-link, as shown in Fig. 4(b). The explicit freewheeling diode is not necessary as the output stage can provide the required free-wheeling current path in case of an input stage interruption. However, commutating the input stage at a nonzero dc-link current causes additional switching losses. Therefore, a coordination of the switching state changes of the input and output stage is advantageous for the USMC. The use of the free-wheeling diode for zero current commutation does potentially increase the circuit reliability because a path for the dc-link current is provided in case an input stage power transistor is not turned on due to, say, a gate drive failure. As is obvious from Fig. 6(a), the switching function of the power transistors of the USMC can be derived from the switching functions of the power transistors of a bridge leg of the SMC by using an OR gate.

IV. Space-Vector Modulation

The modulation concept derived in this section facilitates zero dc-link current commutation and is applicable to the SMC, VSMC and USMC. In order to make a maximum voltage available for the formation of the output voltage, a phase input is clamped to the positive or negative dc-link bus in $\pi/3$-wide intervals when the corresponding phase voltage has the highest absolute value (cf. Table II). Therefore, the required operating condition $u_{pn} > 0$ of the SMC, VSMC, and USMC is inherently satisfied.

With reference to the symmetry of the circuit topology and an assumed symmetry of the three-phase input voltage system with an angular frequency ω_1 and an amplitude of $\hat{U}_1$ (Fig. 8)

$$\begin{aligned} u_a &= \hat{U}_1 \cos(\omega_1 t) \\ u_b &= \hat{U}_1 \cos(\omega_1 t - 2\pi/3) \\ u_c &= \hat{U}_1 \cos(\omega_1 t + 2\pi/3) \end{aligned} \tag{1}$$

TABLE II
DC-Link Bus Potentials and Voltage Over One Input Voltage Period; Shading Indicates Clamping of a Phase Input to the p or n dc Bus

$\varphi_1=\omega_1 t$	u_p	u_n	u
$0 \ldots \pi/6$	u_a	u_b, u_c	u_{ab}, u_{ac}
$\pi/6 \ldots \pi/2$	u_a, u_b	u_c	u_{ac}, u_{bc}
$\pi/2 \ldots 5\pi/6$	u_b	u_c, u_a	u_{bc}, u_{ba}
$5\pi/6 \ldots 7\pi/6$	u_b, u_c	u_a	u_{ba}, u_{ca}
$7\pi/6 \ldots 3\pi/2$	u_c	u_a, u_b	u_{ca}, u_{cb}
$3\pi/2 \ldots 11\pi/6$	u_c, u_a	u_b	u_{cb}, u_{ab}
$11\pi/6 \ldots 2\pi$	u_a	u_b, u_c	u_{ab}, u_{ac}

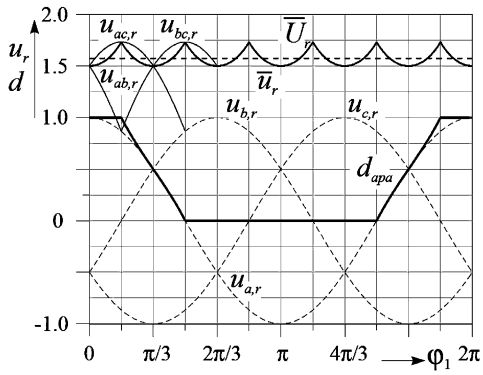

Fig. 8. Time behavior of the input phase voltages u_a, u_b, u_c and of the local average $\bar{u}$ of the dc-link voltage u; $\bar{U}$ denotes the global average value of u; voltages are normalized (index r) to the phase voltage amplitude $\hat{U}_1$. Furthermore shown: duty cycle d_{apa} of power transistor S_{apa}, where for the clamping of phase a to p, $d_{apa} = 1$ is valid.

we will limit our considerations in the following to $\varphi_1 = \omega_1 t = 0 \ldots \pi/6$, where phase a remains clamped to the positive dc bus p. Furthermore, we assume that the dc-link current i has a constant average value $\bar{i}$ for each rectifier switching state. The formation of i and $\bar{i}$ within a pulse period $t_\mu = 0 \ldots T_P$ (t_μ denotes a local time running within a pulse period) will be treated in detail, once the converter modulation scheme has been defined.

The dc-link voltage u is defined by segments of the input line-to-line voltages u_{ab} and u_{ac} according to the rectifier switching state. Therefore, the voltage employed by the inverter for output voltage formation has two different levels within each pulse half period (cf. Fig. 9). For coordinated switching of the rectifier and inverter stage the switching of the rectifier always occurs during the free-wheeling interval of the inverter and zero dc-link current commutation is naturally achieved.

A free-wheeling of the rectifier stage could be realized by turning on the power transistors of a bridge leg simultaneously (e.g., $s_{apa}, s_{ana} = 1$). This is equivalent to an inverter free-wheeling state concerning the formation of the input currents, $i_a, i_b, i_c = 0$, and the formation of the output voltages, $u_{AB}, u_{BC}, u_{CA} = 0$. A low complexity modulation scheme is achieved by; firstly, making each change of the rectifier switching state being linked to an inverter free-wheeling mode, and secondly, only the inverter stage is operated with free-wheeling intervals in order to adjust the output voltage zero vector. For the input stage, this is mathematically given as

$$d_{ab} + d_{ac} = 1 \tag{2}$$

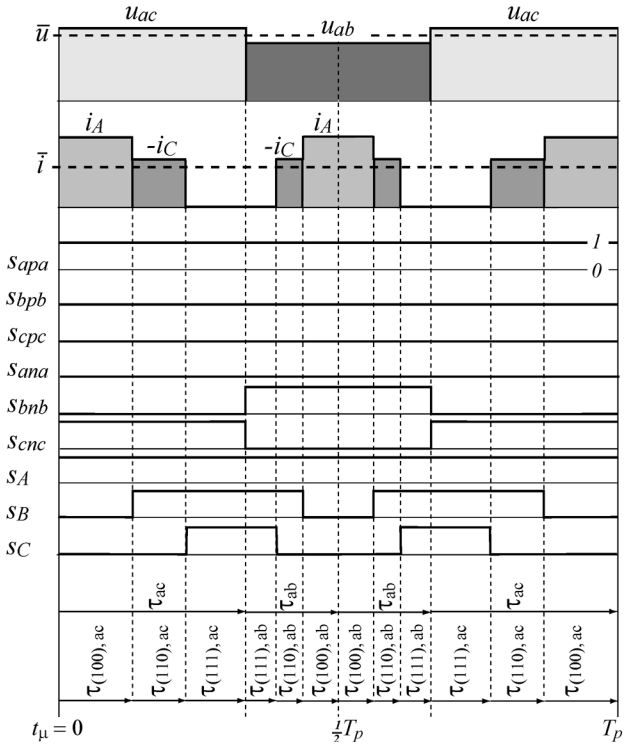

Fig. 9. Formation of the dc-link voltage u and dc-link current i within a pulse period and example switching functions of the rectifier and inverter stage for $\varphi_1 \in (0 \ldots \pi/6)$ and $\varphi_2 \in (0 \ldots \pi/6)$. Input stage switching occurs at zero dc-link current. The dc-link current has a constant average value $\bar{i}$ within τ_{ac} and τ_{ab}. s_A, s_B, and s_C are the output stage switching functions. The switching frequency ripple of u_{ac}, u_{ab}, i_A and i_C is neglected.

where d_{ab} and d_{ac} are the relative on-time of the switching states characterized by $u = u_{ab}$ and $u = u_{ac}$.

In the interval $\varphi_1 = 0 \ldots \pi/6$, where input a is clamped to the positive dc-link bus, the average input current of phases a, b, and c are

$$\bar{i}_a = (d_{ab} + d_{ac})\bar{i}, \quad \bar{i}_b = -d_{ab}\bar{i}, \quad \bar{i}_c = -d_{ac}\bar{i}. \tag{3}$$

In order to achieve an ohmic fundamental input behavior of the rectifier, $\cos\Phi_1 = 1$, we have to guarantee a proportional relationship between the local average value (related to a pulse period) of an input phase current and the corresponding input phase voltage. This results in

$$d_{ac} = -\frac{\bar{i}_c}{\bar{i}_a} = -\frac{u_c}{u_a}; \quad d_{ab} = -\frac{\bar{i}_b}{\bar{i}_a} = -\frac{u_b}{u_a} \tag{4}$$

where $u_a + u_b + u_c = 0$ has been considered.

At the inverter output, a voltage space vector $\underline{u}_2$ with an absolute value of $|\underline{u}_2|$ and a phase of $\varphi_2 = \omega_2 t$ is formed, in the average, over half a pulse period $1/2T_P$ (reference values are denoted by a superscript *). To analyze the voltage formation, we will limit our considerations to $\varphi_2 = \omega_2 t = 0 \ldots \pi/6$. The voltage formations for the other output period intervals can be derived from symmetry considerations.

For $\varphi_2 = 0 \ldots \pi/6$, the formation of the output voltage is achieved by using the active voltage space vectors $\underline{u}_{2,(100)}$ and $\underline{u}_{2,(110)}$ and by the free-wheeling state (111) or (000), where $\underline{u}_{2,(111)} = \underline{u}_{2,(000)} = 0$ is valid. (The inverter output voltage space vectors are denominated by the corresponding combinations $(s_A s_B s_C)$ of the bridge leg switching functions.)

In the time intervals $\tau_{ac} = d_{ac}T_P/2$ and $\tau_{ab} = d_{ab}T_P/2$, we have for the dc-link voltage $u = u_{ac}$ and/or $u = u_{ab}$, and accordingly the absolute value of the inverter output voltage space vector will have a different value. In order to fully utilize the voltages u_{ac} and u_{ab} for the formation of u_2, the output voltage space vectors are required to have the same relative values as τ_{ac} and τ_{ab} (cf. Fig. 10), and this is achieved by using identical values of the duty cycle for the active switching states (100) and (110) in τ_{ac} and τ_{ab}.

$$\delta_{(100),ac} = \frac{\tau_{(100),ac}}{\tau_{ac}} = \delta_{(100),ab} = \frac{\tau_{(100),ab}}{\tau_{ab}} = \delta_{(100)} \tag{5}$$

$$\delta_{(110),ac} = \frac{\tau_{(110),ac}}{\tau_{ac}} = \delta_{(110),ab} = \frac{\tau_{(110),ab}}{\tau_{ab}} = \delta_{(110)}. \tag{6}$$

With $\underline{u}_{(100)} = (2/3)u$ and $\underline{u}_{(110)} = (2/3)ue^{j(\pi/3)}$ for the dc-link voltage u, we then have for the output voltage space vector $\underline{u}_2$ formed in the average over $1/2T_P$

$$\underline{u}_2^* = \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{(100),ac} + u_{ab}\tau_{(100),ab} + u_{ac}e^{j\frac{\pi}{3}}\tau_{(110),ac} + u_{ab}e^{j\frac{\pi}{3}}\tau_{(110),ab}) \tag{7}$$

and by considering (5) and (6)

$$\begin{aligned}\underline{u}_2^* &= \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{ac}\delta_{(100)} + u_{ab}\tau_{bc}\delta_{(100)} + u_{ac}\tau_{ac}\delta_{(110)}e^{j\frac{\pi}{3}} + u_{ab}\tau_{bc}\delta_{(110)}e^{j\frac{\pi}{3}}) \\ &= \frac{2}{3}\left(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P}\right)\delta_{(100)} + \frac{2}{3}\left(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P}\right)e^{j\frac{\pi}{3}}\delta_{(110)} \\ &= \frac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})\delta_{(100)} + \frac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})\,e^{j\frac{\pi}{3}}\delta_{(110)}.\end{aligned} \tag{8}$$

Since the local average value $\bar{u}$ of the dc-link voltage u is

$$\bar{u} = u_{ab}d_{ab} + u_{ac}d_{ac} \tag{9}$$

this results in

$$\underline{u}_2^* = \frac{2}{3}\bar{u}\delta_{(100)} + \frac{2}{3}\bar{u}e^{j\frac{\pi}{3}}\delta_{(110)}. \tag{10}$$

Therefore, to calculate the on-times of the active switching states we could directly refer to the local average value $\bar{u}$ of the dc-link voltage and could omit the detailed consideration of the line-to-line input voltages u_{ac} and u_{ab} in τ_{ac} and τ_{ab}. We then would have

$$\begin{aligned}\delta_{(100)} &= \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\cos(\varphi_2^* + \frac{\pi}{6}) \\ \delta_{(110)} &= \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\sin\varphi_2^*\end{aligned} \tag{11}$$

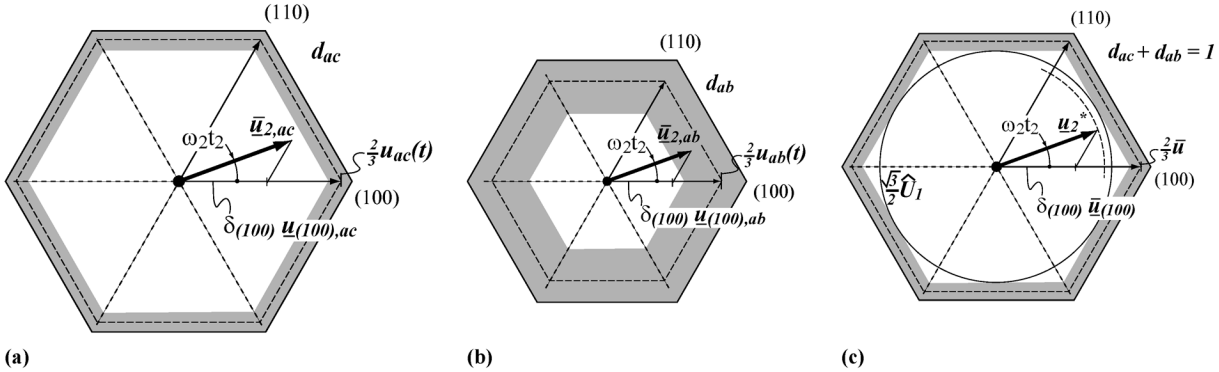

Fig. 10. Inverter output voltage space vectors $\underline{u}_{(100)}$ and $\underline{u}_{(110)}$ and average output voltage vector in (a) τ_{ac} and (b) τ_{ab} and (the range of variation of u_{ac} and u_{ab} is shown by the shaded area). (c) Formation of the inverter output voltage space vector reference value $\underline{u}_2^*$ based on the average value $\bar{u}$ of the dc-link voltage u over half a pulse period. Minimum value of $\bar{u}$ defines the maximum available inverter output phase voltage amplitude of $\sqrt{3}/2\hat{U}_1$.

and, therefore for the *absolute* turn-on times $\tau_{(100),ac}$ $\tau_{(100),ab}$ and $\tau_{(110),ac}$ $\tau_{(110),ab}$ of the output voltage space vectors $\underline{u}_{2,(100)}$ and $\underline{u}_{2,(110)}$ in τ_{ac} and τ_{ab}

$$\begin{aligned}
\tau_{(100),ac} &= -\frac{1}{\sqrt{3}} T_P \frac{\hat{U}_2^*}{\hat{U}_1^2} u_c \cos\left(\varphi_2^* + \frac{\pi}{6}\right) \\
\tau_{(100),ab} &= -\frac{1}{\sqrt{3}} T_P \frac{\hat{U}_2^*}{\hat{U}_1^2} u_b \cos(\varphi_2^* + \frac{\pi}{6}) \\
\tau_{(110),ac} &= -\frac{1}{\sqrt{3}} T_P \frac{\hat{U}_2^*}{\hat{U}_1^2} u_c \sin\varphi_2^* \\
\tau_{(110),ab} &= -\frac{1}{\sqrt{3}} T_P \frac{\hat{U}_2^*}{\hat{U}_1^2} u_b \sin\varphi_2^*.
\end{aligned} \tag{12}$$

As can be seen from (9) and Fig. 8, the local average value $\bar{u}$ of the dc-link voltage shows a variation with six times the input frequency

$$\bar{u} = \frac{3}{2}\hat{U}_1 \frac{1}{\cos(\omega_1 t)} \tag{13}$$

and a minimum of

$$\bar{u}_{\min} = 3/2\hat{U}_1 \tag{14}$$

(cf. Fig. 10). This allows the formation of an output phase voltage system

$$\begin{aligned}
u_A^* &= \hat{U}_2^* \cos(\omega_2 t + \varphi_0) \\
u_B^* &= \hat{U}_2^* \cos\left(\omega_2 t - \frac{2\pi}{3} + \varphi_0\right) \\
u_C^* &= \hat{U}_2^* \cos\left(\omega_2 t + \frac{2\pi}{3} + \varphi_0\right)
\end{aligned} \tag{15}$$

($\varphi_0 = 0$ is selected here for the sake of simplicity, however this does not restrict the general validity of the analysis) that has a maximum fundamental amplitude $\hat{U}_2^*$ of $\sqrt{3}/2\hat{U}_1$. Therefore, we have the relationship for the voltage transfer ratio M of the matrix converter, also known from e.g., [4], as

$$M = \frac{\hat{U}_2^*}{\hat{U}_1} \leqslant \frac{\sqrt{3}}{2}. \tag{16}$$

For a given constant output voltage amplitude $\hat{U}_2^*$ and/or given absolute value $|\underline{u}_2^*| = \hat{U}_2^*$ of the output voltage space vector, the variation of $\bar{u}$ makes a variation of the inverter modulation index necessary

$$m_2 = \frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}} = \frac{4}{3}\frac{\hat{U}_2^*}{\hat{U}_1}\cos(\omega_1 t). \tag{17}$$

In order to ensure, that the free-wheeling state of the inverter remains for a minimum time $\tau_{\min}$ (in $\varphi_2^* = 0 \ldots \pi/6$, we have $\tau_{\min} = \min(\tau_{(111),ac} + \tau_{(111),ab})$, as is required for changing the rectifier switching state at zero dc-link current, the modulation index of the inverter and/or the output voltage reference amplitude has to be limited to

$$\hat{U}_2^* \leqslant \frac{\sqrt{3}}{2}\hat{U}_1\left(1 - 2\frac{\tau_{\min}}{T_P}\right). \tag{18}$$

Therefore, the achievable maximum system voltage transfer ratio will be slightly lower than the theoretical maximum $M_{\max} = \sqrt{3}/2$ as given in (16).

To minimize the inverter switching losses, in $\varphi_2^* = 0 \ldots \pi/6$, only the free-wheeling state (111) is incorporated into the switching state sequence. Accordingly, the output phase A remains clamped within the whole interval to the positive dc-link bus. The clamping intervals of all phases over an output voltage period are given in Table III. Each output phase remains clamped within a $\pi/3$-wide interval which is arranged symmetrically in time around the maxima and minima of the corresponding phase voltage. Accordingly, minimum switching losses will result for an ohmic load.

In case the system is supplying an inductive load, the phase currents and the corresponding phase voltages will show a phase displacement Φ_2

$$\begin{aligned}
i_A &= \hat{I}_2 \cos(\omega_2 t + \Phi_2) \\
i_B &= \hat{I}_2 \cos\left(\omega_2 t - \frac{2\pi}{3} + \Phi_2\right) \\
i_C &= \hat{I}_2 \cos\left(\omega_2 t + \frac{2\pi}{3} + \Phi_2\right).
\end{aligned} \tag{19}$$

The clamping intervals then should be shifted accordingly in order to maintain low switching losses. For example, phase A

TABLE III
INVERTER OUTPUT PHASES POTENTIALS OVER ONE OUTPUT VOLTAGE PERIOD. SHADING INDICATES CLAMPING OF AN OUTPUT PHASE TO THE P OR N DC BUS

$\varphi_2=\omega_2 t$	u_A	u_B	u_C
0 ... $\pi/6$	u_p	u_p, u_n	u_p, u_n
$\pi/6$ ... $\pi/2$	u_p, u_n	u_p, u_n	u_n
$\pi/2$ ... $5\pi/6$	u_p, u_n	u_p	u_p, u_n
$5\pi/6$ ... $7\pi/6$	u_n	u_p, u_n	u_p, u_n
$7\pi/6$ ... $3\pi/2$	u_p, u_n	u_p, u_n	u_p
$3\pi/2$ ... $11\pi/6$	u_p, u_n	u_n	u_p, u_n
$11\pi/6$ ... 0	u_p	u_n, u_p	u_p, u_n

then should be clamped in $\varphi_2^* = 0 \ldots \pi/3$ (clamping of A to p) and $\varphi_2^* = \pi \ldots 4\pi/3$ (clamping of A to n). A detailed analysis of minimum switching loss clamping of dc voltage link inverters is given in [27].

For the formation of the input current [cf. (3)] we still have to prove that the local average $\bar{i}$ of the dc-link current exhibits a constant value. With (5) and (6), we have

$$\begin{aligned}\bar{i}_{ac} &= \frac{1}{\tau_{ac}}\left(i_A\delta_{(100),ac}\tau_{ac} - i_C\delta_{(110),ac}\tau_{ac}\right)\\ &= i_A\delta_{(100)} - i_C\delta_{(110)} \qquad (20)\end{aligned}$$

and

$$\begin{aligned}\bar{i}_{ab} &= \frac{1}{\tau_{ab}}\left(i_A\delta_{(100),ab}\tau_{ab} - i_C\delta_{(110),ab}\tau_{ab}\right)\\ &= i_A\delta_{(100)} - i_C\delta_{(110)}. \qquad (21)\end{aligned}$$

Accordingly, in τ_{ac} and τ_{ab}, an equal average value

$$\begin{aligned}\bar{i} = \bar{i}_{ac} = \bar{i}_{ab} &= \frac{3}{4}m_2\hat{I}_2\cos\Phi_2\\ &= \hat{I}_2\frac{\hat{U}_2^*}{\hat{U}_1}\cos\Phi_2\cos(\omega_1 t) \qquad (22)\end{aligned}$$

of i is available for input current formation as assumed in (3). The variation of $\bar{i}$ is inverse to the variation of $\bar{u}$ and this results in a constant local average value of the dc-link power flow $\bar{p} = \bar{u}\bar{i}$, and/or of the power taken from the input and/or supplied to the load.

Analogous to the analysis for the formation of the inverter output voltage to the local average value $\bar{u}$ of the dc-link voltage, one can give a description of the rectifier input current formation based on the local average value $\bar{i}$ of the dc-link current. There, the variation of $\bar{i}$ results in a variation of the diameter of the hexagon, which is defined by the input current space vectors resulting for the different rectifier switching states. To control the rectifier according to (2), the tip of the input current space vector $\underline{\bar{i}}_1$ being formed in the average over a pulse period will move along the side μ of the hexagon (cf. Fig. 11). In the interval $\varphi_1 = 0 \ldots \pi/6$ being considered, this results in a variation of the modulation index of the rectifier

$$m_1 = \frac{|\underline{\bar{i}}_1|}{\bar{i}} = \frac{1}{\cos\omega_1 t}. \qquad (23)$$

This would not lead to a space vector $\underline{\bar{i}}_1$ of constant absolute value $|\underline{\bar{i}}_1|$ and constant angular frequency ω_1 and/or to sinusoidally shaped local average values of the input phase currents for a constant value of $\bar{i}$. However, due to the variation of $\bar{i}$ according to (22), the hexagon diameter changes such that the tip

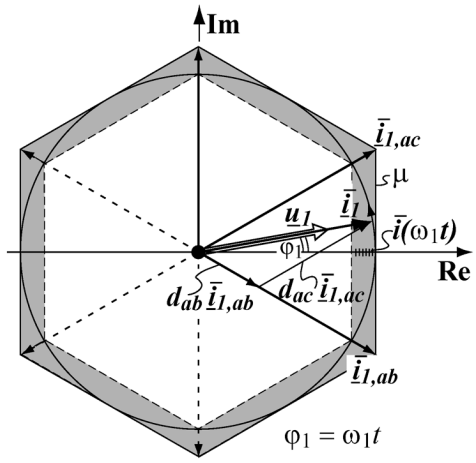

Fig. 11. Rectifier input current space vectors resulting, in the average, over a pulse half period and trajectory of the space vector $\underline{\bar{i}}_1$ within the input voltage fundamental. The diameter of the space vector hexagon is determined by the local dc-link current average value $\bar{i}$ varying over the fundamental period. The range of variation of the hexagon is shown by the shaded area.

of $\underline{\bar{i}}_1$ moves along a circular trajectory and/or sinusoidal local average values of the input phase currents are generated

$$\begin{aligned}\bar{i}_a &= \hat{I}_1\cos(\omega_1 t)\\ \bar{i}_b &= \hat{I}_1\cos\left(\omega_1 t - \frac{2\pi}{3}\right)\\ \bar{i}_c &= \hat{I}_1\cos\left(\omega_1 t + \frac{2\pi}{3}\right). \qquad (24)\end{aligned}$$

This can be verified immediately by combining (22) and (23) into

$$|\underline{\bar{i}}_1| = \bar{i}m_1 = \hat{I}_2\frac{\hat{U}_2^*}{\hat{U}_1}\cos\Phi_2\cos(\omega_1 t)\frac{1}{\cos\omega_1 t} = \hat{I}_1. \qquad (25)$$

As is clear from Fig. 9, the inverter switching frequency is two times the rectifier switching frequency

$$f_{P,1} = 2f_{P,2} \qquad (26)$$

as a full switching cycle of the inverter is contained in each rectifier pulse half interval. A different ratio of the pulse frequency could be selected as long as it ensures that the commutation of the rectifier stage is at zero dc-link current.

As explained, the dc-link voltage u is derived from segments of the input line-to-line voltages u_{ab} and u_{ac} for $\varphi_1 \in [-\pi/6 \ldots \pi/6)$ and can be visualized using Fig. 12(a). In this case, the highest and second highest line-to-line voltages are used and this allows the greatest positive dc-link voltage to be generated. In certain applications (e.g., motor drives operating at low speed) where a low output voltage is required, the input stage can be modulated such that a lower average dc-link voltage is generated as shown in Fig. 12(b). In this case, the dc-link voltage u is derived from the second highest and lowest positive line-to-line voltages, or u_{ab} and u_{bc} for $\varphi_1 \in [0 \ldots \pi/6)$ [28]. Three-level output voltages [Fig. 12(c)] can also be generated using a combination of the conventional [Fig. 12(a)] and the low output voltage modulation [Fig. 12(b)] methods. Alternatively, a three-level output voltage can be

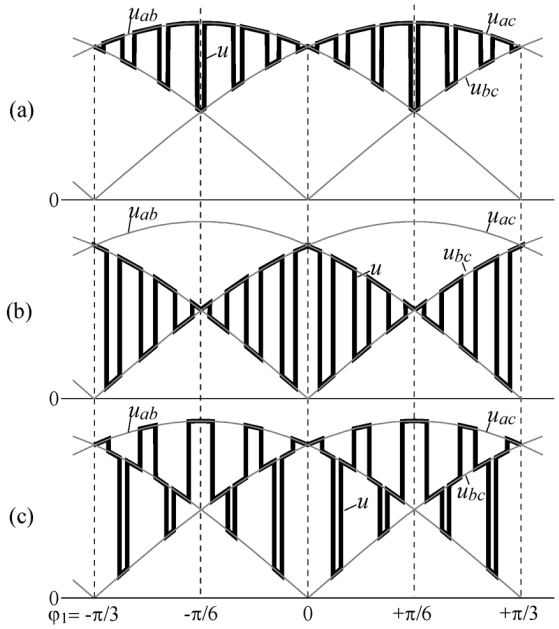

Fig. 12. Generation of the dc-link voltage u using: (a) the highest line-to-line voltages, (b) low-output voltage modulation, and (c) three-level output voltage modulation.

obtained by using additional switches such as that proposed in [26].

V. Operating Range of SMC, VSMC, and USMC

In this section, we will briefly show which space vectors are available for output voltage and input current formation for the SMC, VSMC, and USMC and the restrictions on the operating range that have to be accepted due to the simplification of the circuit structure.

A. Admissible Converter Switching States: SMC and VSMC

For the space-vector description of input voltage and input current, we have the instantaneous active power of

$$p = \frac{3}{2}\Re\{\underline{u}_1^*\underline{i}_1(n)\} = ui \tag{27}$$

supplied to the dc-link ($\underline{u}_1^*$ now denotes the complex conjugate of $\underline{u}_1$). The dc-link current i as impressed by the inverter defines the absolute value of the input current space vectors $\underline{i}_1(n)$ resulting for the different rectifier switching states n. The voltage $u(n)$ occurring at the rectifier output then can be determined with reference to (27) by projection of the input current space vectors along the input voltage space vector $\underline{u}_1$ (cf. Fig. 13(a) and [22]). The condition $u(n) > 0$ is met only by using switching states for which the corresponding current space vector shows a component in the direction of $\underline{u}_1$ and/or is located in the half-plane defined by the direction of $\underline{u}_1$. Therefore, three switching states are not available as they would result in a negative dc-link voltage.

If the sign of i now changes, as could occur by inverting the switching state of the output stage [e.g., by changing form (100) to (011)], the switching states and/or current space vectors $\underline{i}_1(n)$ which result in a negative dc-link power, $p < 0$, are permitted. By changing the sign of i, the current space vectors are also inverted, and as such the switching states are identical to the permitted switching states for $i > 0$. In summary, all current space

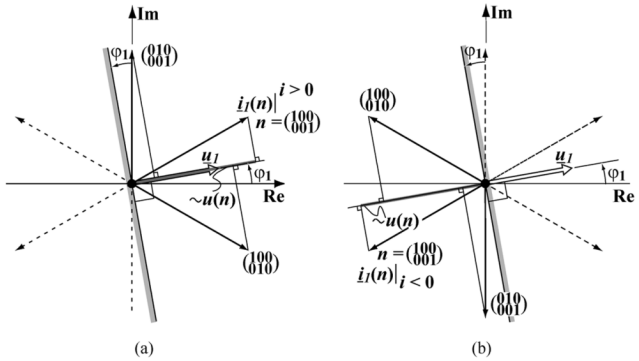

Fig. 13. Input current space vectors and/or rectifier switching states permitted for a given angular position φ_1 of the input voltage space vector $\underline{u}_1$. Current space vectors not available are shown by broken lines. The rectifier switching states n are denoted by a combination of transistors switching functions in matrix form, where each row characterizes the switching state of a bridge leg. (a) Dc-link current $i > 0$ and (b) dc-link current $i < 0$.

vectors available for the CMC can be formed also by the SMC or VSMC despite only three out of six active rectifier switching states being employed.

There are only three space vectors available for the formation of the input current, and therefore the phase displacement of the input current fundamental $\underline{i}_1$ and of the input voltage $\underline{u}_1$ is limited to

$$\Phi_1 \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right). \tag{28}$$

To form an input current with a larger phase displacement angle, with this basic modulation method the current space vectors would not be continuously available over the fundamental period. However, this restriction is of rather low importance, as in most cases ohmic mains behavior is required and (28) would also allow compensation of the capacitive reactive power of the input filter capacitors at rated load. With an extended modulation strategy, the full range of input phase displacement can be realized. The basic principle of this extended strategy is to invert the corresponding output switching states whenever a nonadmissible input stage switching state is desired.

B. Admissible Converter Switching States: USMC

For the USMC, there is the additional restriction that the dc-link current has to be positive ($i > 0$). As will be shown this additional condition also restricts the admissible load power factor. For the inverter stage, in analogy to (27),

$$p = \frac{3}{2}\Re\{\underline{u}_2^*(m)\underline{i}_2\} = ui \tag{29}$$

where $\underline{u}_2^*(m)$ denotes the complex conjugate of the output voltage space vector being present for a switching state m. In order to ensure $i(m) > 0$, only output voltage space vectors and/or switching states m are permitted that are located in the half-plane defined by the output current space vector $\underline{i}_2$ (cf. Fig. 14). Therefore, we have for the output stage the requirement that

$$\Phi_2 \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right) \tag{30}$$

(cf. Fig. 15), which is analogous to the input stage. To supply significant inductive loads, this limitation could be satisfied by using compensating capacitors.

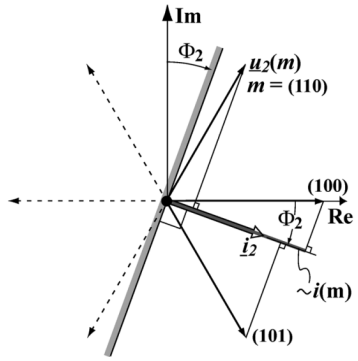

Fig. 14. Output voltage space vectors and/or inverter switching states admissible for the USMC for a given angular position $\varphi_2^* + \Phi_2$ of the output current space vector $\underline{i}_2$. Voltage space vectors not available are shown by broken lines. The inverter switching states m are denoted by the combination of the bridge leg switching functions.

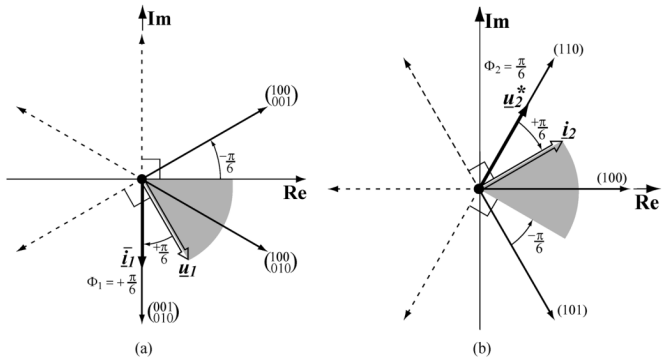

Fig. 15. (a) Input current space vectors and (b) output voltage space vectors available for the USMC for $u_a > 0, u_b, u_c < 0$ (corresponding angular interval of $\underline{u}_1$ shown by shaded area) and $i_a > 0, i_b, i_c < 0$ (corresponding angular interval of $\underline{i}_2$ shown by shaded area). Only current space vectors showing a phase displacement $\Phi_2 < \pi/6$ to the input voltage can be formed; furthermore, the voltage space vectors $\underline{u}_2^*$ to be formed at the output have to remain within $\pm\pi/6$ phase displacement to the output current $\underline{i}_2$ in order not to generate a negative dc-link current.

Since the USMC has a unidirectional power flow, the load must not be allowed to feed energy back into the dc-link since there are no energy storage capacitors and excessive dc-link voltages would be generated. Therefore, the addition of a clamp circuit to the USMC is important. The clamp can be as simple as a series connection of a diode and capacitor across the dc-link [29], [30] and/or as a braking resistor with a series connected controllable switch, which provides braking capability in case of a mains failure, unlike for the conventional MC.

C. Voltage and Current Transfer Ratio

From (17), (22), and (23), we obtain the amplitude of the input current fundamental as

$$\hat{I}_1 = m\bar{i} = \frac{3}{4} m_1 m_2 \hat{I}_2 \cos\Phi_2 \tag{31}$$

and accordingly for the current amplitude transfer ratio of the matrix converter

$$\frac{\hat{I}_1}{\hat{I}_2} = \frac{3}{4} m_1 m_2 \cos\Phi_2. \tag{32}$$

Considering the input and output power balance

$$\frac{3}{2}\hat{U}_1\hat{I}_1 = \bar{u}\bar{i} = \frac{3}{2}\hat{U}_2^*\hat{I}_2\cos\Phi_2, \tag{33}$$

where losses are neglected and $\cos\Phi_1 = 1$ is assumed, it therefore follows that the voltage amplitude transfer ratio is

$$\frac{\hat{U}_2^*}{\hat{U}_1} = \frac{\hat{I}_1}{\hat{I}_2}\frac{1}{\cos\Phi_2} = \frac{3}{4} m_1 m_2. \tag{34}$$

The voltage and current transfer of the system are therefore characterized by a transfer ratio of

$$M = \frac{3}{4} m_1 m_2 \tag{35}$$

where $M \in (0, \sqrt{3}/2)$; introducing (35) into (32) and (34) results in

$$\begin{aligned} \hat{U}_2^* &= M\hat{U}_1 \\ \hat{I}_1 &= M\hat{I}_2\cos\Phi_2. \end{aligned} \tag{36}$$

In the case of a phase difference Φ_1 between the input current and voltage, as set by proper control of the input stage, we would have

$$\begin{aligned} \hat{U}_2^* &= M\hat{U}_1\cos\Phi_1 \\ \hat{I}_1 &= M\hat{I}_2\cos\Phi_2. \end{aligned} \tag{37}$$

It is important to point out that the maximum voltage transfer ratio $(\hat{U}_2^*/\hat{U}_1)_{\max} = \sqrt{3}/2$ is only available for $\cos\Phi_1 = 1$.

Another interesting property of the matrix converter is that the formation of an output voltage is not necessarily connected to the formation of an input current fundamental, such that $\hat{I}_1/\hat{I}_2 = 0$ could be valid. This can be explained by the fact that, with this basic modulating method, only active power is transferred via the dc-link, accordingly, for an output current fundamental displacement factor of $\cos\Phi_2 = 0$ no current, on average, flows in the dc link. On the other hand, $\hat{U}_2^*/\hat{U}_1 = 0$ is possible for $\hat{I}_1/\hat{I}_2 \neq 0$ for the case where the input stage is controlled to give $\cos\Phi_1 = 0$. The segments of the line-to-line input voltages occurring at the rectifier output do not form a local average value $\bar{u}$ of the dc-link voltage and therefore no voltage is available for formation of an output voltage fundamental, i.e., $\hat{U}_2^* = 0$.

Furthermore, the input and output side are basically decoupled concerning the formation of fundamental reactive power, however, the generation of reactive power at the input side is possible for the basic modulation method only when active power is transferred to the output and is limited by the required voltage transfer ratio (38). By using more complex modulation methods it is possible to facilitate reactive power transfer independently of the active power flow [31]. Based on (35) and (37), the maximum admissible phase displacement is

$$\cos\Phi_{1,\max} = \frac{2}{\sqrt{3}}M \quad \text{where } M \leqslant \sqrt{3}/2 \tag{38}$$

or

$$\Phi_1 \leqslant \arccos\left(\frac{2}{\sqrt{3}}M\right). \tag{39}$$

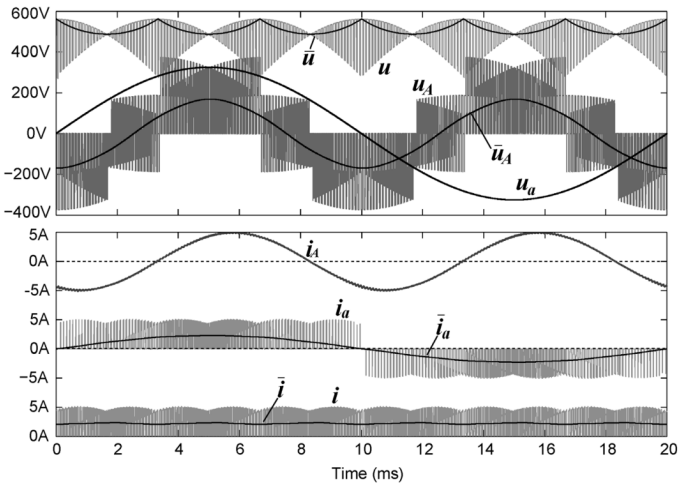

Fig. 16. Simulation waveforms of a 3-phase, 400-V, 50-Hz input SMC supplying 1 kW to the output. The waveforms plotted are: dc-link instantaneous and average voltages u and $\bar{u}$, phase A output voltage instantaneous and averaged u_A and $\bar{u}_A$, input phase voltage u_a, output phase A current i_A, instantaneous and averaged input phase a current i_a and $\bar{i}_a$, and the instantaneous and averaged dc-link current i and $\bar{i}$.

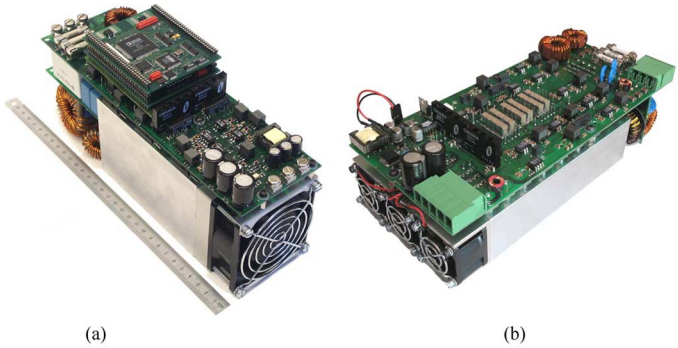

Fig. 17. Photographs of the 6.8-kW prototypes (a) VSMC with dimensions of 24.4 cm × 8 cm × 11.8 cm and power density of 3 kW/liter and (b) USMC, without DSP control board, and dimensions of 26 cm × 12 cm × 6 cm.

Accordingly, with reference to

$$Q_1^2 = \left(\frac{3}{2}\hat{U}_1\hat{I}_1\right)^2 - P^2 \tag{40}$$

where P denotes the active power, the maximum fundamental reactive power Q_1 that can be generated at the input is given by

$$Q_{1,\max} = \frac{3\sqrt{3}}{4}\hat{U}_1\hat{I}_2\sqrt{1-\frac{4}{3}M^2}\cdot\cos\Phi_2. \tag{41}$$

VI. Simulation and Practical Realization

An ideal simulation of SMC [Fig. 4(a)] has been performed using SIMPLORER™ assuming there is no EMI filter, i.e., an ideal mains supply, and an input stage switching frequency of 10 kHz. A 3-phase, 400-V, 50-Hz voltage is applied to the input of the SMC. The inverter stage is controlled to produce a sinusoidal, 100-Hz output voltage, which is applied to a resistive and inductive (RL) load of 30 Ω and 25 mH, respectively. This produces a sinusoidal rms current of 3.5 A in the load (Fig. 16) and the output power is 1 kW. It can be seen that the dc-link voltage is switching between line-to-line voltages [cf. Fig. 12(a)] and that the output phase voltage has an average fundamental component of 100 Hz, the same as the reference frequency. The current pulses flowing in the dc-link are switched by the input stage to the appropriate input phases. Finally, the ideal mains shapes the phase current pulses to form the sinusoidal line currents. In the experimental system, the EMI filter provides the current shaping.

To verify experimentally the operation of the sparse matrix converter concept a 6.8-kW VSMC, shown in Fig. 7(b), has been constructed. For all of the sparse matrix derivatives, the modulation is the same and therefore the waveforms generated have all the same form. It will be shown that the waveforms generated experimentally by the VSMC are the same as those from the simulation of the SMC. The VSMC has been selected for experimental verification as it has 12 controlled switches, which is the same number as the back-to-back converter (BBC), and allows a comparison of the two systems to be undertaken [32]. The prototype VSMC is designed to operate from a 50/60-Hz, 400-V line-to-line mains supply, with an inverter stage switching frequency of 40 kHz and a rectifier stage switching frequency of 20 kHz. The switching times and switch vectors are calculated in a 160-MHz Analog Devices DSP and then transferred to a PLD that generates each of the switch gate signals.

To produce a compact design, semiconductor modules are used that combine as many individual devices as possible into one package. For the inverter stage, three IXYS phase leg modules (IXYS FII 50-12E [33]), which contain two IGBTs and two fast diodes, have been used. This IXYS module has a voltage rating of 1200 V and a current rating of 32 A at a case temperature of 90 °C. For the rectifier stage, six IXYS four-quadrant switch modules [34], manufactured with four diodes and the same IGBT as in the inverter stage modules, are used.

The VSMC has been thermally designed so that the maximum junction of any one semiconductor module is 150 °C. The power dissipation of each switch module is calculated using analytical equations [32] and is used as the input to a 3-D thermal simulation. The length of the heatsink is adjusted to ensure that the maximum junction temperature is not exceeded and to reduce the heatsink volume. The results from the thermal analysis indicate that the highest spot temperature on the VSMC heatsink is 122 °C for an ambient of 45 °C.

The physical arrangement of the VSMC, which includes all power devices, gate drives, passive components, EMI filter, fan, control and power supply, can be seen from the photograph in Fig. 17. The overall volume of the VSMC is 2.3 L and is significantly better compared to a BBC that has a volume of 4.6 L for the exactly the same power rating and thermal limitations of the VSMC [32].

Experimental measurements of the VSMC system have been made (Fig. 18) on the input/output currents and voltages, and the dc-link voltage and switch voltages for the basic modulation method [Fig. 12(a)]. The same operating conditions from the SMC simulation are also applied to the VSMC. The input voltage is 3-phase, 400-V, 50-Hz. The DSP controls the inverter stage to produce a sinusoidal, 100-Hz output voltage $(M = 0.8)$ that is applied to a RL load of 30 Ω and 25 mH, respectively. A sinusoidal rms current of 3.5 A flows in the load [Fig. 18(b)], and the output power level is 1 kW. Fig. 18(a) shows the near-sinusoidal

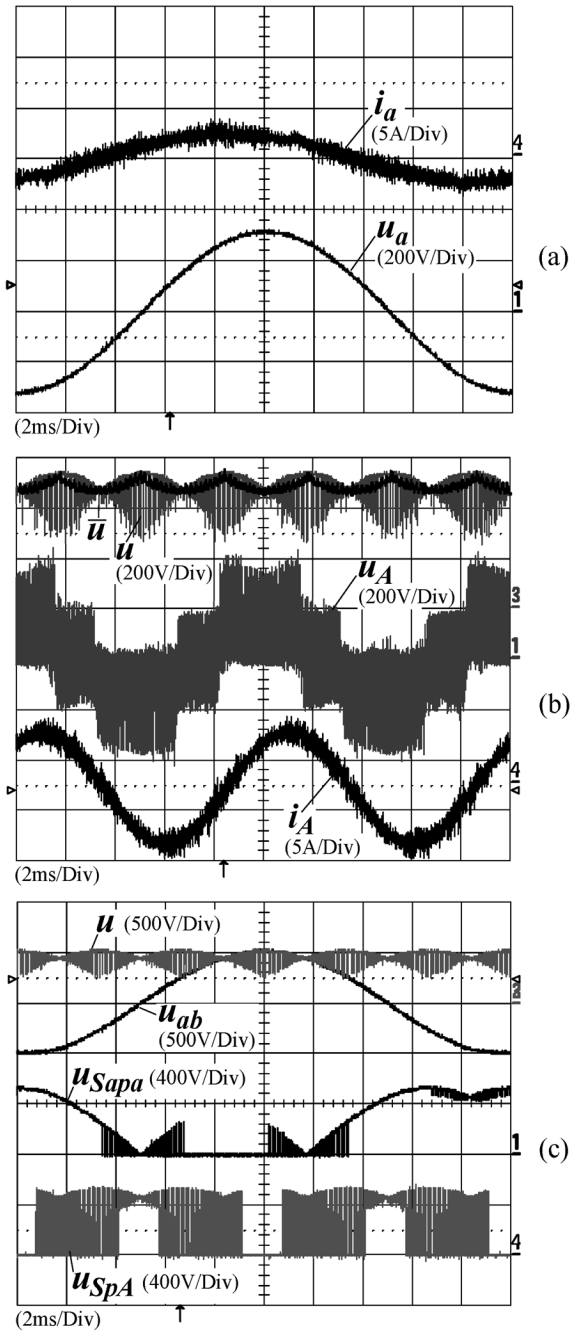

Fig. 18. Experimental results from a VSMC: (a) input phase current and voltage for phase a, (b) output phase voltage and current, and the dc-link voltage and local average value, and (c) dc-link voltage, input line-to-line voltage, and rectifier/inverter-stage switch voltage between p bus and phase a/A.

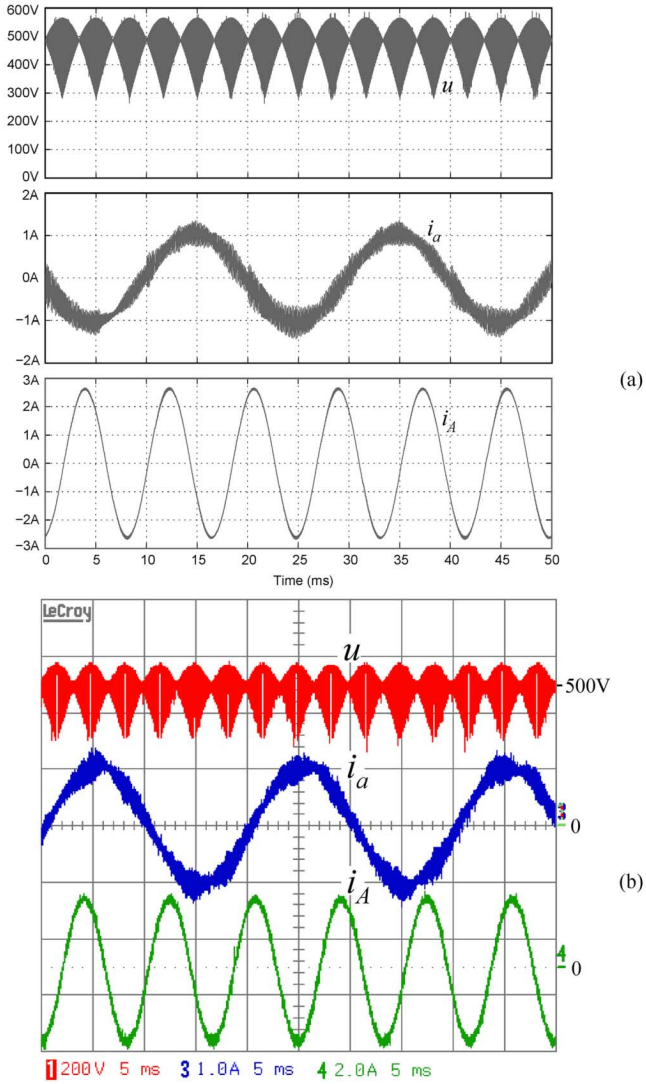

Fig. 19. (a) Simulation and (b) experimental waveforms from the USMC supplying a 1-kVA R-L load. Shown are the dc-link voltage u, 50-Hz input phase A current i_a, and the 120-Hz output phase A current i_A.

input current and the supply-phase voltage waveforms. At this low output power level compared to the rated power, the current is leading the voltage due to the reactive power of the ac input filter (10 μF per phase [32]). As the real component of the output load current is increased then input power factor becomes closer to unity. Fig. 18(b) shows the unfiltered output voltage, the current flowing in the RL load and the instantaneous dc-link voltage, u, which is formed from switching between the line-to-line voltages. The average value of this dc-link voltage, $\bar{u}$, is represented by the dark line plotted on top of the dc-link voltage. It can be seen that the output current is sinusoidal and has a fundamental frequency twice that of the supply. Therefore, the VSMC is successfully operating as an ac-to-ac matrix converter.

The voltage stress across the rectifier and inverter stage switches, the input phase-a to phase-b voltage and the dc-link voltage are presented in Fig. 18(c). It can be seen that the dc-link is switched to u_{ab} for a duration of 60° and that the switch *Sapa* clamps the input voltage to the p dc bus for 60° (as seen when $u_{S_{apa}} = 0$). The top inverter stage switch for the *A* phase is clamped to p dc bus for two 60° intervals and is turned off for a further two 60° intervals, while the remainder of the time active switching occurs.

To experimentally verify the operation of the USMC [Fig. 4(b)] a 6.8-kW prototype has been constructed [Fig. 17(b)]. The same output stage IGBT modules from the VSMC are used in the USMC. Each phase of the input stage is constructed from a single four-quadrant switch module, as used in the VSMC but where only two of the four diodes are used, and two discrete diodes are added. Fig. 19 shows SIMPLORER™ simulation and experimental waveforms of the USMC when operated from a 3-phase, 400 V_{ll}, 50-Hz input and supplying a 1-kVA RL load

with a 120-Hz output voltage. The output and input stages have a switching frequency of 50 and 25 kHz, respectively. As can be seen, the dc-link voltage has the same characteristic shape as the SMC and VSMC. The input and output currents are sinusoidal and therefore an unidirectional ac-to-ac converter based on the USMC topology is possible.

VII. Conclusion

As proposed in this paper, the functionality of a conventional three-phase ac-ac matrix converter could be achieved by employing only 15 IGBTs based on the SMC concept. A zero dc-link current commutation scheme provides lower control complexity and potentially higher reliability compared to the multistep commutation strategies. Zero dc-link current commutation also allows the input stage of an IMC to be realized by four-quadrant switches. This results in the VSMC topology, which comprises of only 12 IGBTs. An isolated four-quadrant switch is commercially available and therefore the SMC and the VSMC are of great interest to industry as an alternative to the CMC concept. The disadvantage with all matrix converters is the output voltage range is less than the input voltage. For electrical drive applications this requires that a nonstandard machine is used. In certain applications, such as aircraft actuators and elevator drives, specialist machines are required and therefore sparse matrix converters are applicable.

If only unidirectional power flow with an output phase displacement angle limited to $\pm\pi/6$ is required then the USMC is an attractive alternative for three-phase ac-ac energy conversion. The USMC only requires nine IGBTs for the system realization. A VSMC and a USMC prototype have been constructed and they experimentally verify that the concept of reduced switch number matrix converters is feasible. All the sparse matrix derivatives show great promise in industrial applications that require specialized direct ac-to-ac conversion.

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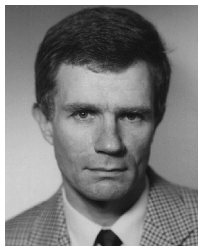

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