Control-Oriented Modeling and Robust Control of a Three-Phase Buck+Boost PWM Rectifier (VRX-4)

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***Abstract* – The modeling and control of a three-phase, three-switch buck-type rectifier system with integrated boost output stage (VRX-4) is analyzed in this paper. A cascaded multi-loop control structure is presented that has the following features: constant output voltage for a wide input voltage range and step-wise changes of load; sinusoidal input currents in phase with the mains voltages that also remain sinusoidal in case of asymmetric mains conditions; and active damping of the input filter resonance. For the control design an equivalent DC-DC small-signal model of the converter is derived and verified by simulations and measurements. Based on this and the identification of the critical operating point the controllers for the inner DC current and outer voltage control loops are selected. The stability of the closed loop system is discussed and the robust operation of the system is verified by measurements on a 5kW prototype.**

I. INTRODUCTION

In [1] a three-phase PWM rectifier formed by integration of a three-phase, three-switch buck-type front end and a DC-DC boost-type output stage has been proposed. This topology e.g. gives the possibility of controlling the output voltage to 400V for a wide input voltage range of $208V_{rms}…480V_{rms}$ with employing only 4 power transistors (cf. **Fig. 1**), therefore it is denominated as Voltage Range Extended 4-Switch Rectifier (**VRX-4**). For the control-oriented modeling, control design and implementation of the system one has to consider the following points:

- Firstly, for operation in a wide input voltage range the dynamics of the system to be controlled changes. Therefore, controllers have to be identified that enable stable operation with good reference tracking and disturbance rejection behavior for all operating points.
- Secondly, the input filter shown in Fig. 1 which has been developed in [2] for compliance to the EMC standard EN55022 takes a major influence on the control stability by significantly increasing the system order. In [3] a sufficient condition for a separate design of the control and the input filter was given, whose fulfillment, however, leads to oversized filters and/or poor control bandwidth [4]. Thus, for achieving a good control performance the dynamics of the filter has to be directly considered in the control design.
- Furthermore, an active damping of the input filter resonance, as developed in this paper, takes substantial influence on the stability of the inner control loop and therefore should not be neglected in the controller design.
- And finally, the losses of the power semiconductors (switching and conduction losses) also influence the dynamics as they provide additional passive damping to the system. This fact is often neglected in conventional converter modeling [5],[6].

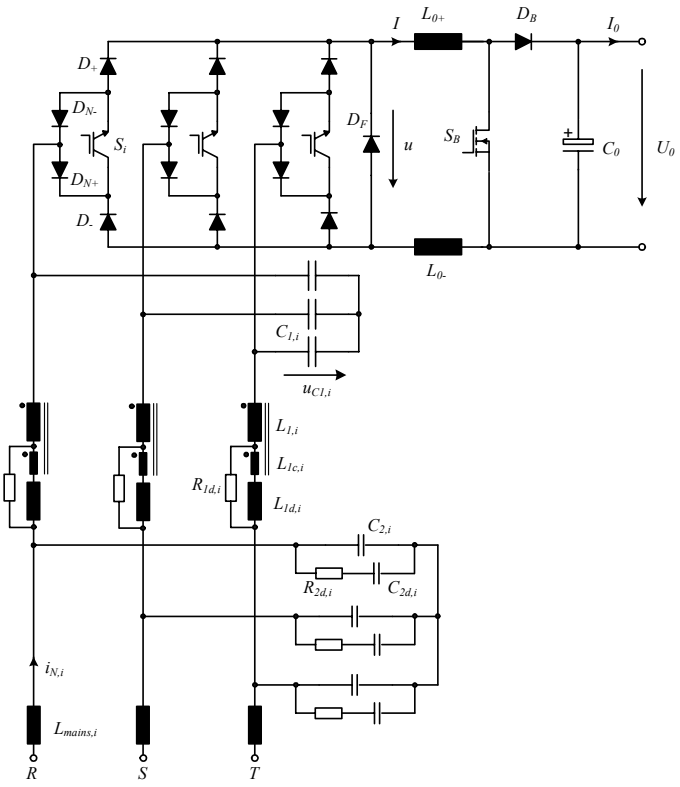

Fig. 1: Topology of the Voltage Range Extended 4-Switch Rectifier (VRX-4) including input filter [2], three-phase buck-type rectifier input part and boost-type output part.

In this paper, a control implementation for the VRX-4 rectifier is proposed. After a short description of the basic operating behavior of the rectifier in **section II** the control-oriented modeling of the topology is presented and verified in **section III** and the dynamically critical operating point of the system is identified in **section IV**. In **section V** the proposed control structure that features robustness against disturbances from the mains and/or load side and ensures sinusoidal mains currents under unbalanced mains conditions is discussed. Especially, four important issues for the control are then matter of discussion, namely: a *feedforward of the load* facilitating an optimum disturbance rejection and/or minimum output voltage drop for load variations; a *DC current shaping* in order to enable sinusoidal mains currents also for asymmetric mains condition; a *common current controller* allowing a smooth transition between the operation modes, i.e. the pure buck mode for high input voltages and the buck+boost mode for low input voltages; and an effective and easy-to-realize *active damping scheme* and its influence on the input filter stability; and. In **section VI** the controllers are designed and the control performance is shown by measurements on a 5kW prototype in **section VII**.

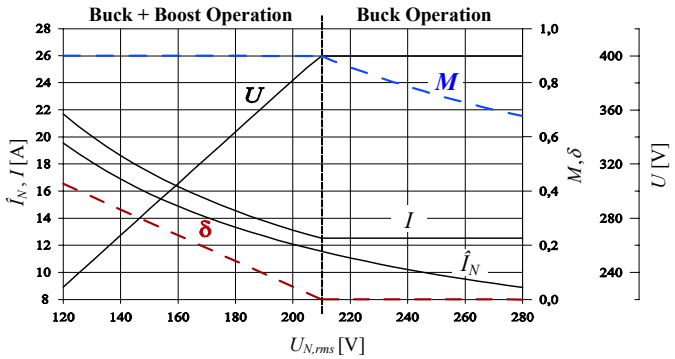

Fig. 2: Operating areas of the buck+boost rectifier: in the buck operating mode the modulation index M of the buck-type rectifier input stage is reduced with increasing input voltage and the relative on-time δ of the boost switch is equal to zero, while in the buck+boost operating mode the modulation index M is set to M_{max} = 0.9 and the boost switch is activated according to (4).

II. Basic Operating Behavior

The operating behavior of the system is already described in [1] in detail, therefore it will be treated very briefly. Basically, there are two operation modes. First, the buck operating mode, where only the switching functions of the three transistors S_i of the buck-type rectifier input stage have to be controlled and the boost switch is turned off. And, secondly, the buck+boost mode, where due to low mains voltages and/or high reference output voltage the boost stage and/or boost switch is controlled and the buck stage is operated in open-loop. The maximum DC link voltage u_{max} at the output of the buck-type rectifier input stage is given by

$$u_{max} = \frac{3}{2} \cdot M_{max} \cdot \sqrt{\frac{2}{3}\left(u_{C1,R}^2(t) + u_{C1,S}^2(t) + u_{C1,T}^2(t)\right)}\,, \qquad (1)$$

which corresponds for the case of symmetric mains to

$$U_{max} = \frac{3}{2} \cdot M_{max} \cdot \hat{U}_{C1}\,. \qquad (2)$$

The modulation index

$$M = \frac{\hat{I}_N}{I} = 0 \ldots M_{max} \qquad (3)$$

is limited to M_{max} = 0.9 in order to reserve some modulation margin $m_{damp} = 0 \ldots 0.1$ for active damping which will be discussed later in section V. For an output voltage reference value U_0* being higher than u_{max} the on-time of the boost converter has to be set according to

$$\delta = 1 - \frac{u_{max}}{U_0^*}\,. \qquad (4)$$

Fig. 2 shows the dependency of the operating variables on the input voltage for symmetric mains conditions. However, for asymmetric mains, such as loss of one phase, the control structure presented in section V has to be applied in order to maintain sinusoidal input current shapes and the modulation index of the buck converter m and the duty cycle of the boost converter δ are then both changing during the mains period.

For the forthcoming modeling and control design the following operating parameters were considered:

$U_{N,l-l} = 208V_{rms} \ldots 480V_{rms}$	$L_0 = L_{0+} + L_{0-} = 2mH$
$U_0 = 400V$	$C_0 = 750\mu F$
$P_0 = 5kW$	$C_{l,i} = 6.8\mu F$
$f_S = 28kHz$	$L_{l,i} = 240\mu H$

III. Control-Orientated Converter Modeling

An equivalent DC-to-DC model of the three-phase AC-to-DC rectifier has already been developed in [7] for the rectifier input stage, the complete equivalent model is given in **Fig. 3**(a). The main idea of the modeling is that for a DC side control the three-phase AC-to-DC buck-type rectifier stage shows similar behavior as a DC-to-DC buck converter with a suitable DC input voltage and appropriate values of the passive filter components (cf. Fig.3(a)) [8]. The complete equivalent input filter is shown in Fig.3(a), however, as Fig. 9 in [2] shows, the cut-off frequency of the mains-sided filter stage lies about one decade above the converter-sided filter stage, wherefore for the control-orientated modeling finally only the converter-sided filter stage has to be considered.

For developing a small signal model of the converter showing exactly the same dynamic behavior it is not sufficient only to consider the voltage and current transfer ratios. The switching and conduction losses of the rectifier provide considerable damping that can be modeled by equivalent series and parallel resistors, as depicted in Fig. 3(b).

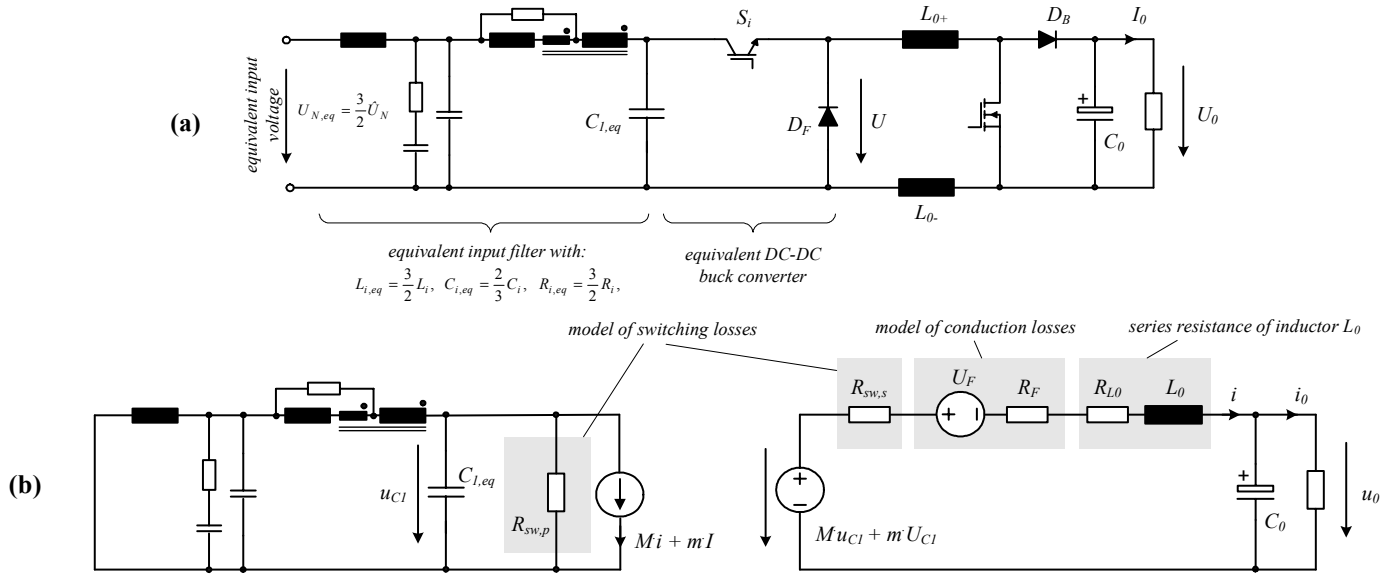

Fig. 3: DC-DC model of the VRX-4 rectifier system with equivalent input parameters **(a)** and linearized small signal model of the converter for $U_{N,l-l}$ = 230V$_{rms}$ (M = 0.82) containing damping elements such as the series resistor of the DC inductor and equivalent resistors modelling switching and conduction losses **(b)**.

Since the controller design will be carried out for the buck operation mode which is the critical case as will be shown later, the boost switch is not considered here.

In order to ascertain the equivalent resistor values first the switching losses of the converter at the operating point of interest have to be determined as it was done for the system at hand in [9]. The turn-on, turn-off, reverse and forward recovery losses are dependent on the switched voltage and the switched current according to the function given by (1) in [9]. However, for deriving a linear model the function has to be simplified to a linear dependency on the equivalent capacitor voltage U_{C1} (cf. Fig. 3(a)) and the DC current I

$$P_{sw} \approx k \cdot U_{C1} \cdot I \,. \tag{5}$$

The losses occurring in the equivalent resistors $R_{sw,p}$ and $R_{sw,s}$ (cf. Fig. 3(b) are given by

$$P_{sw} \approx \frac{U_{C1}^2}{R_{sw,p}} + I^2 \cdot R_{sw,s} \,. \tag{6}$$

By taking the derivative of (5) and (6)

$$\frac{\partial}{\partial U_{C1}}\left(P_{sw}\right) = k \cdot I = \frac{2 \cdot U_{C1}}{R_{sw,p}}, \tag{7}$$

$$\frac{\partial}{\partial I}\left(P_{sw}\right) = k \cdot U_{C1} = 2 \cdot I \cdot R_{sw,s} \tag{8}$$

the values of the resistors can therefore be ascertained

$$R_{sw,p} = \frac{2 \cdot U_{C1}}{k \cdot I}, \tag{9}$$

$$R_{sw,s} = \frac{k \cdot U_{C1}}{2 \cdot I} \,. \tag{10}$$

E.g. for $U_{N,l\text{-}l} = 230\mathrm{V_{rms}}$ and the operating parameters given in section II (I = 12.5A) and the losses calculation in [9] (k = 0.013) the equivalent damping resistors $R_{sw,p}$ = 5.9kΩ and $R_{sw,s}$ = 260mΩ are derived. The separation into a parallel and a series resistor represents a separation into a purely voltage dependent and a purely current dependent part of the switching losses. It should be noted that an equivalent model with a series resistor at the input side and a parallel resistor on the DC side would also be possible. This would, however, lead to resistor values that are then dependent on the actual modulation index.

The conduction losses of the IGBTs (U_{CE0}, r_{CE}), module diodes ($U_{F,DM}$, r_{DM}), the freewheeling diode ($U_{F,DF}$, r_{DF}) and the boost diode ($U_{F,DB}$, r_{DB}) can be modeled by a total forward voltage drop U_F, which is not influencing the dynamics of the system but is altering the operating point

$$U_F = M \cdot \left(2U_{CE,0} + 4U_{F,DM} + U_{F,DB}\right) + (1-M) \cdot \left(U_{F,DF} + U_{F,DB}\right), \tag{11}$$

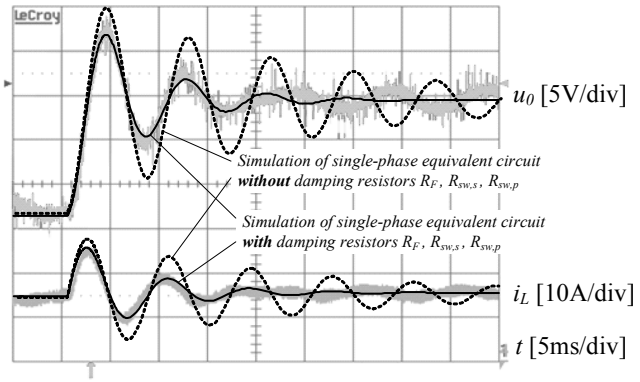

Fig. 4: Response of the output voltage for a stepwise change of the modulation index (M = 0.82 → 0.84) in open-loop operation for the three-phase system and the single-phase equivalent DC-DC circuit with and without consideration of the switching and conduction losses in the model.

and a total forward resistance R_F

$$R_F = M \cdot \left(2r_{CE} + 4r_{DM} + r_{DB}\right) + (1-M) \cdot \left(r_{DF} + r_{DB}\right). \tag{12}$$

Together with the series resistance R_{L0} of the DC inductor $L_0 = L_{0+}+L_{0-}$ the damping provided by the equivalent resistors R_F, $R_{sw,p}$ and $R_{sw,s}$ precisely corresponds with the damping appearing in the real system, which is verified in **Fig. 4** for a small signal step response of the output voltage for open loop operation of the system[1]. In contrary, without consideration of switching and conduction losses in the model the damping is considerably lower.

However, the waveforms in Fig. 4 are mainly dominated by the output filter dynamics of the output filter (the oscillation frequency in Fig. 4 corresponds with the output filter resonance frequency) wherefore the equivalent model of the input parameters can not be verified directly by this test.

Hence, additionally a step of the input voltage for impressed output current was simulated. As can be seen in **Fig. 5** the time behavior of the local averaged value of the DC link voltage u at the freewheeling diode D_F perfectly coincides with the time response of the equivalent linearized single phase model for a small-signal step of the input voltage. Both the overshoot amplitude and the resonance frequency are matching accurately, what from it can be concluded that the modeling of the rectifier is successful.

IV. Critical Operating Point

The system is operating in two operation modes, namely: the pure buck mode, where the control variable is the duty cycle of the buck-type input part of the converter; and the buck+boost mode, where the duty cycle of the buck part is set to a constant value and the on-time of the boost transistor is the control variable (cf. section II).

As will be explained in section V one common controller for both operating modes is utilized, therefore the critical operating condition for the plant that is seen by the controller has to be identified. The controllers will then be designed for this worst case condition.

For both operation modes the plant that is seen by the inner current loop controller mainly shows integral behavior with a conjugated complex pole-pair and a conjugated complex zero-pair. These zeros/poles that are originating from the first section of the input filter basically define the stability of the inner loop, while the output filter, due to the significantly lower resonance frequency and the slow output voltage controller, has no influence. Therefore, the identification of the critical operating point can be restricted to an analysis of the dominant zero-pole combination.

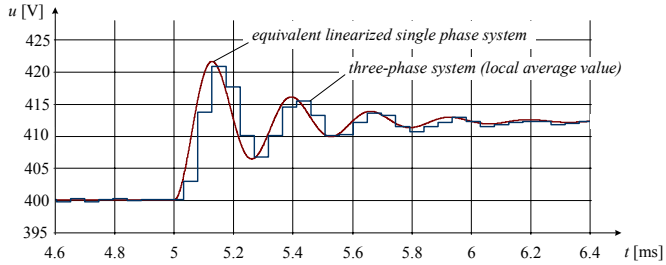

Fig. 5: Simulated response of the DC link voltage u at the freewheeling diode D_F for a stepwise change of the amplitude of the input voltage ($\Delta\hat{U}$ = 10V) and for constantly impressed output current I =12.5A in open-loop operation for the three-phase system and the single-phase equivalent DC-DC circuit.

[1] The 100Hz component that can be observed in the hardware measurement is originating from small asymmetries in the hardware setup but is not caused by a resonance in the system.

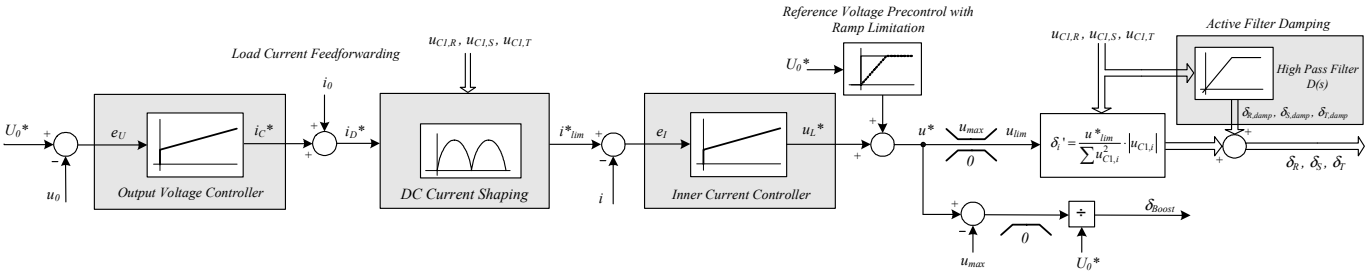

Fig. 7: Complete control structure enabling sinusoidal input currents under unbalanced mains conditions including a feedforward of the load current and active damping of the input filter.

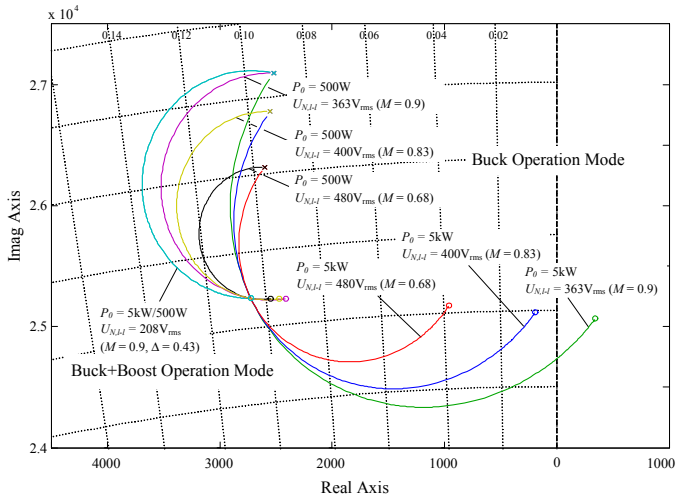

Fig. 6: Zoom of the root locus diagram showing the dominant poles of the inner control loop for different operating points. The input line-to-line voltage is varied within the specified voltage range and the output power varied between rated load and 10% of the rated load.

In **Fig. 6** the root locus diagram is shown for several operating conditions. It can be seen that for higher output power the system is less stable than for low output power[2]. The position of the poles of the open loop system are not changed while the zeros move towards the right half plane. Also with decreasing input voltage (higher modulation index M) the stability margin decreases. The worst case condition in the buck operating mode is therefore full power P_0 = 5kW and minimum voltage $U_{l\text{-}l} = 363\text{V}_{\text{rms}}$ at the border of the buck+boost mode. If the input voltage is further lowered the control variable then becomes the duty cycle of the boost transistor and therefore the plant is changed. From Fig. 6 it can be seen that the system is always stable in this operating mode and that the dynamics are not influenced by the output power.

This fact can be explained if we derive the open loop transfer functions of the two operation modes.

In the first step, only a single stage input filter without passive damping is considered and the output voltage is assumed to be constant. Then, the open-loop transfer function for the buck operation is equal to

$$G_{Buck}(s) = \frac{i}{m} = \frac{U_N}{L_0} \cdot \frac{(1 + s^2 L_I C_I) - \frac{M^2}{C_1} \cdot \frac{I_0}{U_0} s}{s(1 + M^2 \cdot \frac{L_I}{L_0} + s^2 L_I C_I)} . \qquad (13)$$

[2] Here, a minimum load of 10% was chosen in order to maintain continuous mode operation

It can be seen that in (13) a zero in the right half plane occurs due to the negative s-coefficient in the numerator. If the passive damping of the filter is added, the zero will move towards the left and potentially enter the left half plane for decreasing loads (I_0 in (13)) and increasing input voltages (decreasing M in (13)), as already described above for Fig. 5.

For the buck+boost operating mode it can be shown that the negative s-coefficient in the numerator disappears, therefore also the dependency of the position on the load and the input voltage:

$$G_{Boost}(s) = \frac{i}{\delta} = \frac{U_0}{L_0} \cdot \frac{1 + s^2 L_I C_I}{s(1 + M^2 \cdot \frac{L_I}{L_0} + s^2 L_I C_I)} . \qquad (14)$$

Hence, the converter always has higher stability in the buck+boost operation mode compared to the pure buck operation mode.

Based on these considerations, for the forthcoming controller design the before-mentioned operating point (P_0 = 5kW, M = 0.9) is considered.

V. Control Structure

In **Fig. 7** the basic control structure of the buck-type rectifier is depicted. A slow outer control loop regulates the output voltage to a constant reference voltage U_0* and sets the reference value for the fast inner DC current loop. A feedforward of the load current (cf. section V.A) decreases the variation of the output voltage in case of sudden load changes. A current shaping circuit which will be discussed in section V.B provides sinusoidal input currents also in case of asymmetric mains phase conditions such as phase loss or short-circuit between two phases. The output of the inner current controller u_L* has a precontrol of the rate-limited reference output voltage $U_{0,lim}$* in order to improve the large-signal behaviour of the controller in case of a start-up. The output of the current controller is the required inductor voltage so that the DC current follows the reference current and is used for the calculation of the relative on-times of the transistors of the buck input part as well as the boost output part (cf. section V.C). An active damping scheme (cf. section V.D) is additionally employed in order to damp the resonance of the input filter.

A. Load Current Feedforward

A load current feedforward scheme is added to the output of the output voltage controller, which can be viewed as the reference capacitor current i_C*. This gives a direct reference step for the underlying DC current control loop and enables an immediate change of the relative on-times of the power transistors for sudden steps of the load current. Hence, the reference value for the underlying current control loop is changed instantly without causing significant involvement of the (very slow) outer voltage loop. The effect of this disturbance feedforward method is proved experimentally in section VII. However, it is necessary to include the dynamics of the feedforward in the design of the output voltage controller as it is done in section VI.

B. DC Current Shaping

For a constant output voltage reference value, a slow output voltage controller and no variation of the load the current reference value i_D^* (cf. Fig. 7) will be a constant value according to the power demand of the load. However, for asymmetric mains conditions the power that can be drawn from the mains is varying over the mains periods if sinusoidal input currents shall be maintained. Hence, accordingly the current reference then has to be changed [10],[11].

The average power demand of the output voltage controller is calculated by

$$P^* = U_0^* \cdot i_D^* . \tag{15}$$

For achieving sinusoidal mains currents in phase with the input voltages the three phases of the converter must show resistive behavior, i.e. the rectifier inputs look from the mains side as three resistors with resistance and/or conductance values

$$G^* = \frac{1}{R^*} = \frac{\bar{i}_{rec}}{u_{C1}} . \tag{16}$$

being constant over one mains period. The conductance values can be calculated by summation of the average power drawn from the three phases

$$\begin{aligned} P^* &= \left(\frac{\hat{U}_{C1,R}}{\sqrt{2}}\right)^2 \cdot G^* + \left(\frac{\hat{U}_{C1,S}}{\sqrt{2}}\right)^2 \cdot G^* + \left(\frac{\hat{U}_{C1,T}}{\sqrt{2}}\right)^2 \cdot G^* = \\ &= \frac{\hat{U}_{C1,R}^2 + \hat{U}_{C1,S}^2 + \hat{U}_{C1,T}^2}{2} \cdot G^*, \end{aligned} \tag{17}$$

where the peak values of the phase voltages have to be detected by a peak detection circuit. The instantaneous power at the input of the rectifier has to equal the instantaneous power at the output side of the rectifier

$$p = \left(u_{C1,R}^2 + u_{C1,S}^2 + u_{C1,T}^2\right) \cdot G^* = u_{0,lim} \cdot i^* , \tag{18}$$

where $u_{0,lim}$ is the reference output voltage, that is limited to the maximum instantaneous DC link voltage u_{max} (1)

$$\begin{aligned} u_{0,lim} &= U_0^* \qquad for \qquad U_0^* \le u_{\max} \\ u_{0,lim} &= u_{\max} \qquad for \qquad U_0^* > u_{\max} \end{aligned} \tag{19}$$

Using (18) the reference current can be calculated:

$$i^* = \frac{u_{C1,R}^2 + u_{C1,S}^2 + u_{C1,T}^2}{u_{0,lim}} \cdot G^* . \tag{20}$$

As stated before, for the case of asymmetric mains conditions the DC link current is then shaped by the inner controller according to the power demand with double mains frequency. The peak values can then potentially exceed the maximum allowable current values I_{max}. Therefore, the current reference value i^* has to be limited to I_{max}, or – if the sinusoidal shape of the mains currents has to be maintained also in this case – i^* has to be re-scaled according to

$$\begin{aligned} i_{scal}^* &= i^* \qquad for \qquad i_{peak}^* \le I_{\max} \\ i_{scal}^* &= i^* \cdot \frac{I_{\max}}{i_{peak}^*} \qquad for \qquad i_{peak}^* > I_{\max} \end{aligned} , \tag{21}$$

where i^*_{peak} is the peak value of i^* during a half mains period.

C. Common Current Controller for Smooth Transition between Operation Modes

In order to prevent oscillations at the boundary between the pure buck operation mode and the buck+boost operation mode a common controller is employed (cf. Fig. 7). The output of the current controller is then utilized for the calculation of the relative on-times of the buck-type input part as well as for the boost output stage.

If different controller types and/or gains would be employed the boundary between the operation modes would have to be detected accurately and without any time delay in order to switch exactly between the two control modes and to enable a smooth transition. Since measurements in reality contain noise and/or delay times the robustness of the control is significantly improved with a common controller.

For the case that the reference voltage u^* is lower than the maximum output voltage of the buck input part u_{max} the duty cycle of the boost transistor is set to zero and the relative on-times of the three buck transistors are derived by

$$\delta_i' = \frac{u^*}{\sum u_{C1,i}^2} \cdot \left|u_{C1,i}\right| . \tag{22}$$

If u^* exceeds u_{max} the on-times of the buck transistors are set to

$$\delta_i' = \frac{u_{max}}{\sum u_{C1,i}^2} \cdot \left|u_{C1,i}\right| \tag{23}$$

and additionally the boost converter has to be turned on

$$\delta_{Boost} = \frac{u^* - u_{\max}}{U_0^*} . \tag{24}$$

The smooth transition between these two operation modes will be verified experimentally in section VII.

D. Active Damping of the Input Filter

An active damping method that has been analyzed for the equivalent DC-to-DC buck converter and for a one-stage input filter without passive damping in [7] is applied and designed here for the three-phase system with the two-stage EMI input filter shown in Fig.1. Due to the

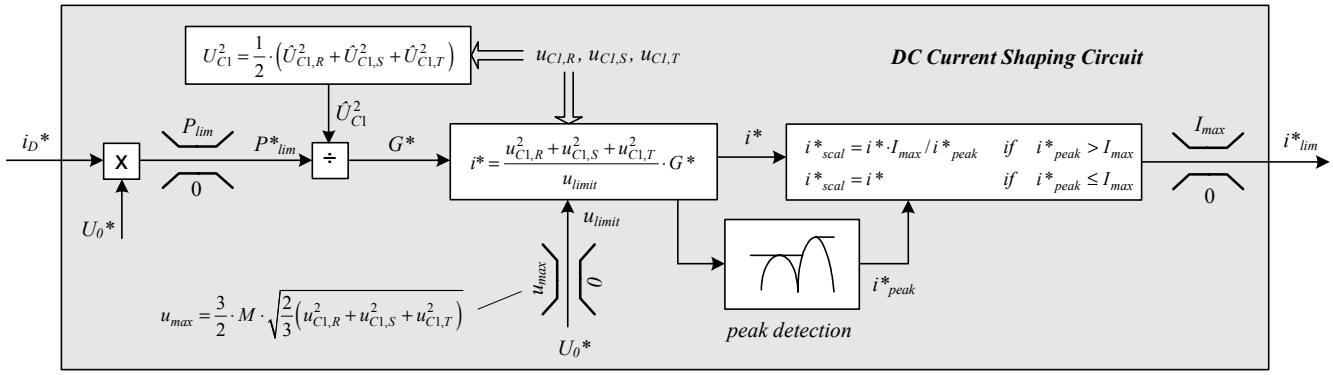

Fig. 8: Complete control structure enabling sinusoidal input currents under unbalanced mains conditions including hysteresis type output voltage controller, a feed-forward of the load current and active damping of the input filter.

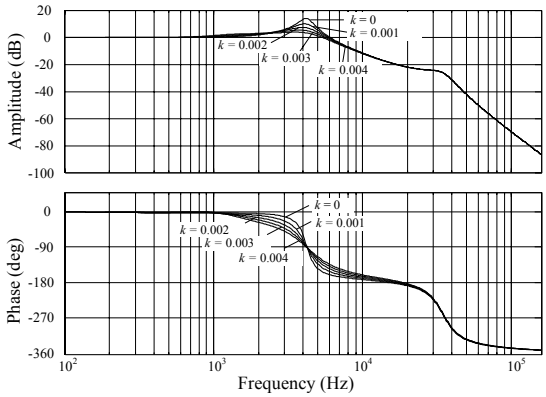

Fig. 9: Bode diagram of the transfer function $G(s) = u_{C1} / u_N$ for different damping factors k (with $L_{mains} = 50\mu H$).

input filter characteristic the filter can possibly be excited by harmonics contained in the feeding mains voltages mainly at the resonance frequency of the first filter stage (L_1-C_1) at $f_{res,1} = 3.4kHz$ (for $L_{mains} = 50\mu H$). For providing active damping, the resonant part of the filter capacitor voltages are fed back to the control system and band-pass filtered around $f_C \sim f_{res,1}$. As the control block diagram in Fig. 7 of [7] shows, this method works like a damping resistor that is only valid for frequencies above f_G. The gain of this feedback has to be selected very carefully, since the amount of damping has substantial impact on the stability of the system. Compared to other active damping methods this technique does not require any additional measurements such as mains voltages or filter inductor voltages [12] that are usually not available and is not only restricted to oscillations originating from the rectifier itself [13].

In the design step the considerations are limited to one phase due to the equivalent DC-to-DC model resulting in a change of the duty cycle by

$$m = m' + m_{damp} . \tag{25}$$

However, for a three phase system resonances normally cause ringing in the amplitude and phase of the capacitor voltage space vector, hence the relative on-times of the switches of all phases have to be adapted to

$$\delta_i = \delta_i' + \delta_{i,damp} \qquad i = R,S,T . \tag{26}$$

Due to phase symmetry it is sufficient to calculate only two damping coefficients

$$\begin{aligned} \delta_{R,damp} &= D(s) \cdot u_{C1,R}, \\ \delta_{S,damp} &= D(s) \cdot u_{C1,S} \end{aligned} \tag{27}$$

and derive the third one by

$$\delta_{T,damp} = -(\delta_{R,damp} + \delta_{S,damp}) . \tag{28}$$

For the design of the active damping filtering function

$$D(s) = \frac{m_{damp}}{u_{C1}} = k \cdot F(s) \tag{29}$$

the filter type $F(s)$ and the active damping factor k have to be selected. An important requirement for the filter is the sufficient suppression of the fundamental component of the filter capacitor voltage $u_{C1,50Hz}$ in order not to introduce an additional 50Hz component to the duty cycle. Here, a digital Bessel high-pass filter of third order with a cut-off frequency of 1kHz and an attenuation of -78dB at 50Hz was selected. It can be shown that due to the characteristic shape of the Bessel filter it less manipulates the phase of the open loop inner control path compared to other filter structures such as Chebyshev, Cauer or Butterworth filters. Since the digital high-pass filter is only working until the switching frequency it performs the required band-pass filtering function.

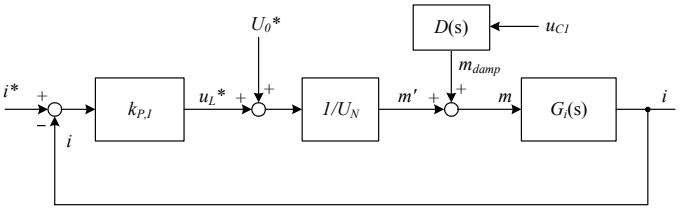

Fig. 10: Block diagram of the inner current control loop.

The damping effect can be observed in the transfer functions that are plotted in **Fig. 9** for different k-factors. Obviously, the resonant peak at the resonance frequency is lowered with increasing damping factors. However, the damping should not be chosen too high. One reason is the loss of phase margin and/or decrease of bandwidth of the inner current control loop. Secondly, the amplitudes of the damping coefficients (13),(14) should not exceed considerably the reserved modulation space of $|\delta_{i,damp}| \leq 0.1$ for practical cases of mains voltage disturbances. With this, the damping factor of $k = 0.002$ is selected as a good compromise.

The effect of the active damping scheme will be proved by experimental measurements in section VII.

VI. Controller Design

Based on the small-signal model derived in section II the appropriate controllers for the inner current loop and the outer voltage loop have to be selected for the critical operating point.

A. Inner DC Current Control Loop

Once that a model of the system is found and verified (cf. section III) and the critical operating condition is identified (cf. section IV), the control structure is decided and the active damping function $D(s)$ is determined (cf. section V) the ultimate task is the controller design, where all of the before-mentioned issues have to be considered. A control oriented block diagram for the inner control loop is depicted in **Fig. 10**.

The bode diagram in **Fig. 11** shows, that a purely proportional controller

$$K_I(s) = k_{P,I} \tag{30}$$

is sufficient due to the integral behaviour of the plant below the input filter resonance frequency[3].

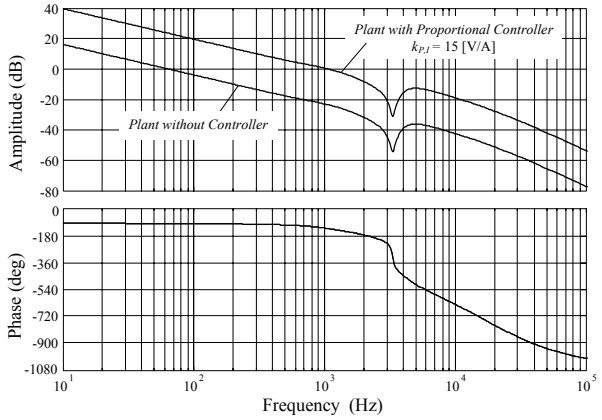

Fig. 11: Open loop bode diagram of the inner DC current control loop without controller and with the selected controller ($k_{P,I} = 15$ [V/A]).

[3] Due to the low dynamics of the outer output voltage control loop the output voltage can be regarded as constant for the inner loop.

The selection of the appropriate controller gain is naturally a trade-off between dynamics and stability. For the case at hand, a gain of

$$k_{P,I} = 15 \ [\mathrm{V/A}] \tag{31}$$

was selected.

B. Outer Output Voltage Control Loop

For the design of the output voltage controller the whole dynamics of the plant including the load current feedforwarding (cf. section V) and the closed inner control loop (cf. section VI.A) have to be considered.

Generally, the bandwidth and therefore the gain of the output voltage loop has to be much lower than twice the mains frequency in order to suppress the 100Hz component of the output voltage for a mains phase failure and keep the reference power P^* and the reference conductance G^* constant over one mains period. For achieving a bandwidth of f_{BW} = 1Hz and a sufficient phase margin for ensuring an overshoot-free step response (φ_M > 70°) a purely integral controller with

$$k_{I,U} = 0.43[\mathrm{A \cdot rad/(Vs)}] \tag{32}$$

is selected. The bode diagram of the plants with and without the voltage controller is shown in **Fig. 12.**

For the loss of one phase, which represents the worst case, the capacitor voltage ripple (peak-to-peak value) according to

$$e_{U,p-p} = \Delta u_{p-p,100Hz} = 2 \cdot \frac{P_0}{U_0} \frac{1}{2\omega C_0} = 53V \ . \tag{33}$$

would cause with this controller (32) a reference power ripple (peak-to-peak value) of

$$\Delta P^*_{p-p} = e_{U,p-p} \frac{k_{I,U}}{2\pi \cdot 100Hz} \cdot U_0^* = 14.5W \ , \tag{34}$$

which is less than 0.3% of the rated output power.

VII. Experimental Verification

The proposed control structure has been implemented on a DSP board and tested on a 5kW hardware prototype of the system. In the following, the features of the robust control scheme that were discussed in section V will be verified by measurement results.

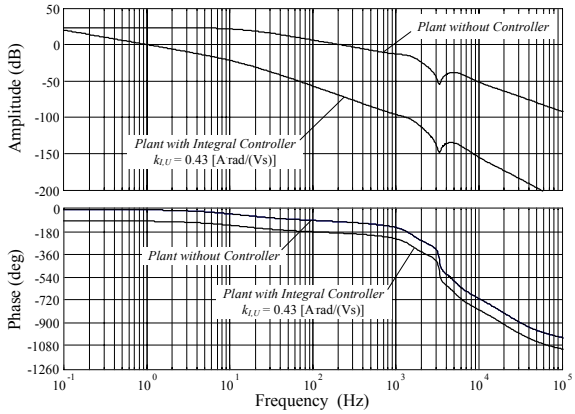

Fig. 12: Open loop bode diagram of the outer output voltage control without controller and with the selected controller ($k_{I,U}$ = 0.43 A rad/(Vs)).

First, in order to show the robustness of the control to load variations a load step from half load to full load was performed. The waveforms in **Fig. 13** prove that the DC link current and therefore also the mains currents immediately change their amplitude due to the load current feedforward (cf. section V.A), while the output voltage remains on a constant level.

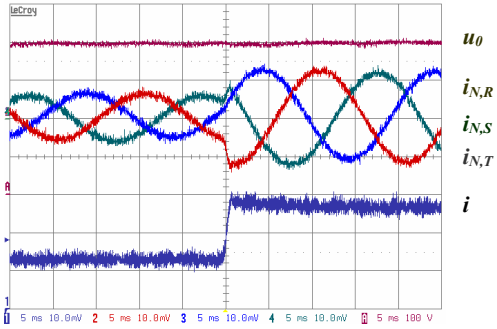

Fig. 13: Voltage and current waveforms for a sudden load step (2.76kW → 5.52kW) (voltage scale: 100V/div, current scale: 5A/div, time scale: 5ms/div).

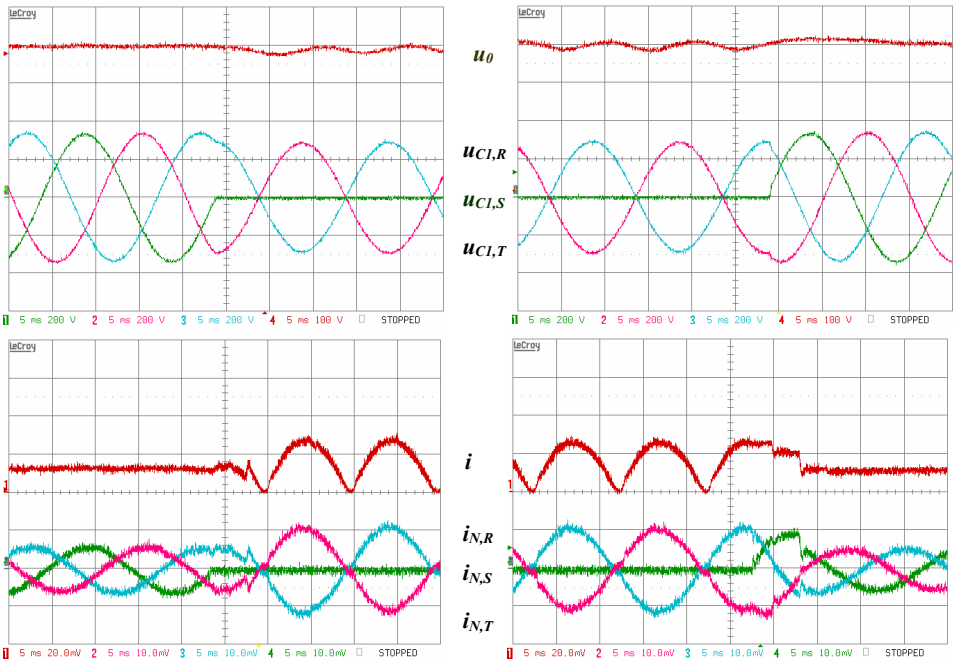

Fig. 14: Experimental results for a phase loss and a reconnection of phase *S*. Time behaviour of output voltage u_0, input filter capacitor voltages $u_{C1,i}$, DC link current i, and mains phase currents $i_{N,i}$. Voltage scales: u_0: 100V/div, $u_{C1,i}$: 200V/div, current scales: i, $i_{N,i}$: 10A/div, time scale: 5ms/div.

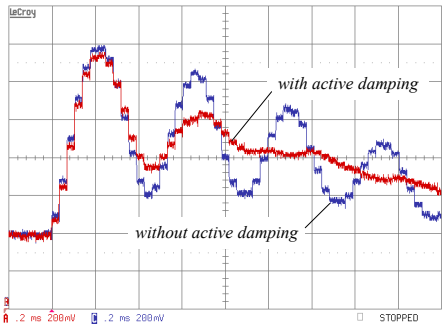

Fig. 15: Filter capacitor voltage waveforms $u_{C1,R}$ (local averaged values) for a sudden step of the mains voltage amplitude $\hat{U}_N$ of 70V (voltage scale: 20V/div, time scale: 200µs/div).

For a loss of one mains phase the measurement results are shown in **Fig. 14**. It can be seen that the two remaining phases maintain with sinusoidal input currents in phase with the input voltages, while the DC link current then also has sinusoidal shape due to the DC current shaping circuit (cf. section V.B) and the output voltage shows a 100Hz ripple. For the phase loss as well as the re-connection of the phase the new peak values of the filter capacitor voltages are detected after a quarter mains period and therefore the power reference and the current reference for the underlying control loop are adapted without affecting the output voltage significantly.

In **Fig. 15** the effect of the active damping technique (presented in section V.C) is shown. The reaction of the input filter capacitor voltage $u_{C1,R}$ was observed for a sudden step of the mains voltage amplitude appearing at the moment of the maximum value of $u_{C1,R}$. Apparently, the active damping scheme exhibits a great improvement in the time behavior of the capacitor voltage. While the amplitude of the overshoot can not be reduced notably with this measure, the input filter capacitor voltage shows a well-damped time behavior compared to the operation without active damping scheme.

Last, the smooth transition between buck mode and buck+boost mode due to the common current controller (cf. section V.D) is illustrated in **Fig. 16**. Due to a sudden change of the voltage reference u_0^* from a value below the maximum buck rectifier output voltage u_{max} to a value $u_0^* > u_{max}$ the converter has to perform a transition from pure buck mode ($m = 0.65$, $\delta = 0$) to buck+boost mode ($m = 0.9$, $\delta = 0.1$). According to the proposed control scheme at the boundary between theses two operation modes the modulation index m of the buck rectifier input stage is simply limited to its maximum value ($m = 0.9$) and the output of the current controller is used then for controlling the duty cycle of the boost converter. Since the controller was designed for the critical operating point of the system (cf. section IV) stable operation is ensured in both control modes and the transition between the modes is performed in the predicted smooth way.

VIII. CONCLUSIONS

The control of the VRX-4 (Voltage Range Extended 4-Switch Rectifier) was investigated in this paper. With the proposed robust control scheme the output voltage can be kept constant ($U_0 = 400$V) and sinusoidal input currents are guaranteed for a wide input voltage range ($U_{N,l\text{-}l} = 208$V…480V), for extensive load variations as well as heavily unbalanced mains conditions such as loss of one phase or short-circuit between two phases.

In the course of the control design a detailed modelling of the system was undertaken, where it was found that the damping effect of switching and conduction losses of the converter has to be considered in the model. Since the system has to operate in two dynamically different control modes due to the wide input voltage range, the worst

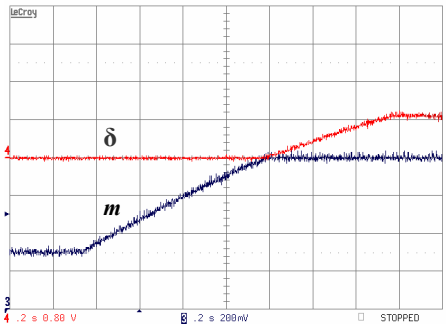

Fig. 16: Time behavior of the modulation index m of the buck-type rectifier input stage and the duty cycle δ of the boost output stage for a step-wise change of the voltage reference u_0^* from pure buck operation ($m = 0.65$, $\delta = 0$) to buck+boost operation ($m = 0.9$, $\delta = 0.1$). Duty cycle scales (m, δ): 0.1/div, time scale: 200ms/div).

case operating condition was identified and a common controller for both operation modes was utilized in order to achieve a smooth transition between the two modes. Furthermore, an active damping scheme for additional damping of the input filter resonance was designed.

All theoretical considerations could be verified by experimental results on a hardware prototype of the system. With the proposed control scheme the topology is of high interest where a wide input voltage and/or wide output voltage range is required, e.g. for telecom power supplies or future applications in the More Electric Aircraft area.

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