Prediction Techniques Compensating Delay Times Caused by Digital Control of a Three-Phase Buck-Type PWM Rectifier System

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***Abstract* – The digital control of a three-phase, three switch buck-type rectifier system is analyzed in this paper. Three main sources of delay times in the control loop can be identified for the implementation on a digital signal processor, namely: the delay time due to the sampling of the control quantities; the one due to the calculation time of the DSP; and the one due to the sample-and-hold function of the PWM modulator. Their influence on the stability of the inner current control loop is discussed and two prediction methods for compensation, namely a linear prediction and the Smith prediction, are comparatively evaluated. The control performance and the effect of the delay times and the prediction methods are finally shown by simulation results and through and measurements on a 5kW prototype.**

I. INTRODUCTION

Three phase buck-type PWM rectifiers (cf **Fig. 1**, frequently also denominated as current source rectifiers) feature constant output voltage, sinusoidal input currents, unity power factor, direct start-up and overcurrent protection in case of an output short circuit. Therefore, this topology is of high interest for the realization of front-end converters for telecommunications power supply modules, for applications in future More Electric Aircrafts or as power supplies for process technology. By integration of the buck-type rectifier with a boost-type output stage [1] a wide input and/or output voltage range can be achieved and sinusoidal input currents in phase with the input voltages can also be maintained in case of heavily unbalanced mains and/or in case of a mains phase loss.

The control of this system has already been treated in literature [1]-[4], however, the influence of a digital realization has not been considered until now. The implementation of the control on a digital signal processor (DSP) is the state of the art nowadays since it facilitates the integration of more functionality, the implementation of more complex control schemes and high flexibility for changes of the program. On the other hand, digital signal processing always results in delay times, mainly due to three reasons:

- the sampling of the continuous current and voltage quantities [5]
- the calculation time of the DSP and
- the PWM outputs [6],[7].

Each of these delay times introduces a phase shift in the control loop

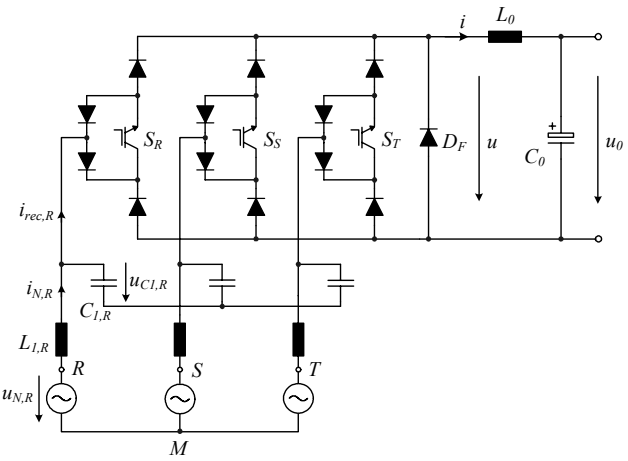

Fig. 1: Topology of the three phase buck-type PWM rectifier

which reduces in total the achievable control bandwidth or diminishes the closed-loop system stability. Therefore, prediction methods have been investigated in order to compensate the delay times, among them the most popular one, the Smith prediction [8], which was successfully implemented e.g. in [9]. However, to the knowledge of the authors until now the implementation effort of this prediction method has not been investigated for the control of more complex system such as buck rectifier systems and compared with simple alternatives.

In this paper, the delay times due to the DSP control are identified and their effect on the stability is analyzed for a three-switch buck-type PWM rectifier. In **section II** a basic control structure of the rectifier is presented and explained briefly. The delay times that are occurring due to the digital computation are analyzed in **section III**. In **section IV** two prediction methods for compensating the delay times are presented and their performance is shown by simulation results in the time-domain. **Section V** summarizes the comparative evaluation of the two prediction methods and in **section VI** measurement results on a 5kW hardware prototype show the effect of the delay times and the prediction techniques.

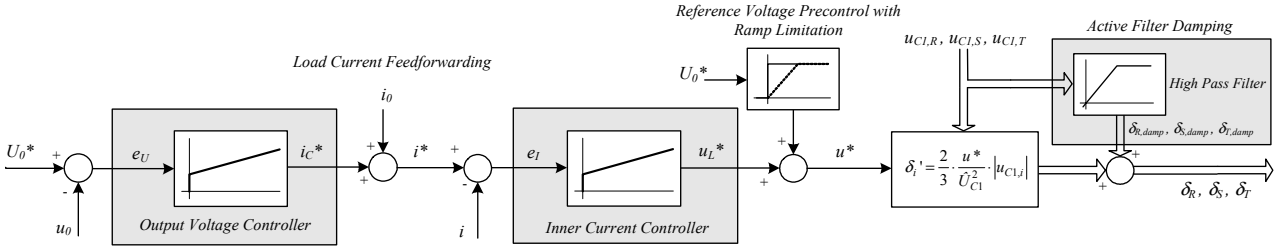

Fig. 2: Cascaded two-loop control structure for the buck-type PWM rectifier including load current feedforward, reference voltage precontrol and an active damping of the input filter resonance.

II. CONTROL STRUCTURE

In **Fig. 2** a basic control structure of the buck-type rectifier is depicted. An outer control loop regulates the output voltage to a constant reference value U_0* and sets the reference value i* for the inner DC current loop. A feedforward of the load current decreases the variation of the output voltage in case of load changes. The output of the inner current controller u_L* has a precontrol of the rate-limited reference output voltage $U_{0,lim}$* in order to improve the large-signal behaviour of the controller in case of a start-up. For achieving sinusoidal input currents the conduction times of the three buck transistors have to be

$$\delta_i' = \frac{2}{3} \cdot \frac{u^*}{\hat{U}_{C1}^2} \cdot \left| u_{C1,i} \right| \qquad (1)$$

independent of the utilized modulation method [1]. An active damping scheme, which is explained in detail in [4] is additionally employed in order to damp the resonance of the input filter.

Therefore, for this control scheme the output voltage u_0, the DC current i and at least two of the input filter capacitor voltages $u_{C1,i}$ ($u_{C1,R} + u_{C1,R} + u_{C1,R} = 0$) have to be measured. The output voltage loop usually is very slow, therefore the measurement of the output voltage is not time-critical, while for the fast inner loop eventual delays in the detection and calculation of the current and the voltages can decrease the control performance, as will be shown in the following.

III. ANALYSIS OF SYSTEM DELAYS

The following considerations are based on the analysis of the delay times for the inductor current i. However, for the derivation of the delay times of the filter capacitor voltages $u_{C1,i}$ that are also relevant for the dynamics of the inner current control loop (see active damping in section II) the same conclusions can be drawn, therefore this is not executed here for the sake of brevity.

The selection of the switching frequency is always a crucial part of the converter design. On one hand it significantly influences the efficiency and the power density of the system, on the other hand the delay times introduced by the digital control are directly decreased for lower switching frequencies.

In [10] it was found that for the buck-type rectifier topology (cf. Fig. 1) a switching frequency in the range of f_P = 20Hz...30kHz leads to a good compromise between efficiency (switching losses) and power density (volume). For the system at hand a switching frequency of $f_P = 1/T_P$ = 28kHz was selected.

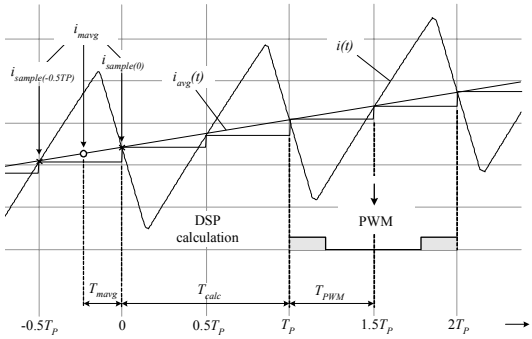

Fig. 3: Delays occurring due to current acquisition (two-times oversampling and moving averaging of the inductor current i), DSP calculation and PWM generation. The current is sampled two times within one pulse period (in the middle and in the beginning and/or end of each period) and the moving average function introduces a delay of $0.25T_P$. Due to the calculations of the control commands and on-times a delay of one full pulse period occurs. Additionally, the sample-and-hold function of the PWM causes a half pulse period delay, therefore resulting in $1.75T_P$ total delay.

The measurement of the DC current is performed by a magnetoresistive Sensitec CMS 2025 DC current sensor [11]. The DSP [12] has a 20MSPS, 14-bit analog-to-digital converter and therefore the conversion delay can be neglected. As shown in **Fig. 3**, the samples are taken every half pulse period exactly at the middle and at the end/beginning of each pulse interval (in Fig. 3 this is explicitly shown for $t = -0.5T_P$ and $t = 0$). If a symmetric triangular carrier is used for the PWM generation the samples at these time instants are ideally not containing any switching frequency components, therefore should be identical to the local average values of the current $i_{avg}(t)$ (cf. Fig. 3 at $t = -0.5T_P$ and $t = 0$).

However, in order to improve the robustness of the measurement result against inaccuracies in the current acquisition an additional moving average function of second order is employed. The transfer function of this filter is given by

$$G_{mavg} = \frac{1}{2}\left(1 + e^{-sT_P/2}\right), \qquad (2)$$

the effect of this filter is depicted in **Fig. 4**. It can be seen that the switching frequency and its higher harmonics are perfectly suppressed while the magnitude of lower frequencies (<5kHz) is not essentially affected by this operation.

For lower frequencies, the moving averaging function can be approximated with good accuracy as a delay of a quarter pulse period

$$G_{mavg} \approx e^{-sT_P/4}, \qquad (3)$$

which is proven in Fig. 3, where the moving average value i_{mavg} occurs at $-0.25T_P$. Fig. 4 also shows the good accordance of the magnitudes of (2) and (3) until 10kHz and of the phases until the switching frequency f_S = 28kHz.

For the calculation of the actual input voltage sector and/or relation of the input phase voltages which determines the switching states employed for forming the input current, the control commands and the calculation of the relative on-times of the PWM outputs one pulse period is reserved (cf. Fig. 3), therefore generating an additional delay of

$$G_{calc} \approx e^{-sT_P}. \qquad (4)$$

In the subsequent pulse period the PWM pulse pattern according to the relative on-times δ_i that have been calculated before is applied to the system. In [7] it is shown that a modulator with instantaneous sampling, as e.g. for analog control, has zero phase lag. Compared to this, the system at hand performs a sample-hold function, thus keeping the values of δ_R, δ_S, and δ_T constant for one whole pulse period.

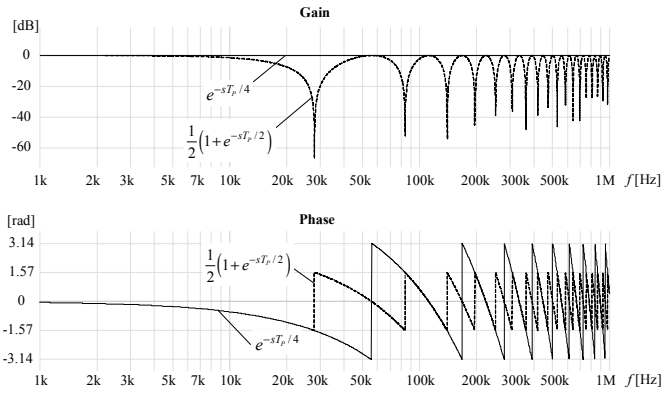

Fig. 4: Bode diagram of the transfer function of a moving averaging operation of second order (2) in comparison with the approximated transfer function of a delay of $0.25T_P$ (3).

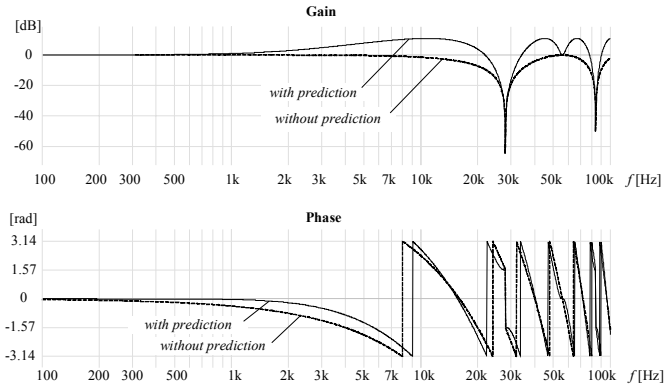

Fig. 5: Influence of the linear prediction (7) on the magnitude and phase of the delay transfer function (6).

As can be proven by simulations and/or analytical calculations this introduces an additional delay time of a half pulse period[1]:

$$G_{PWM} = e^{-T_P/2}. \tag{5}$$

The resolution of the PWM output of the DSP (12.5ns) and the delay time of the utilized gate driver (200ns) are small and could be neglected, therefore. Accordingly, the total transfer function of the digital processing of the DSP is

$$G_{del} = G_{mavg} \cdot G_{calc} \cdot G_{PWM} = \frac{1}{2}\left(1 + e^{-sT_P/2}\right) \cdot e^{-s \cdot 1.5T_P} \approx e^{-s \cdot 1.75T_P}. \tag{6}$$

IV. Prediction Methods

A. Linear Prediction

The sampling, digital processing and pulse-width modulation introduce a large phase shift, e.g. $\varphi = \pi/2$ at $f = 4$kHz (cf. **Fig. 5**). For a purely integral plant and a proportional controller this would already represent the maximum bandwidth at the border to instability. For a conservative controller design the maximum loop bandwidth would be limited to $f = 1$kHz.

A possible way to compensate the delay time effect is a linear prediction of the forthcoming current values. This method works without knowledge about the system to be controlled and simply predicts the forthcoming value by a linear function based on the past values.

As a first step the total average delay time has to be calculated. From (6) and as can be seen in **Fig. 6** an average delay time of $1.75T_P$ occurs between the point $t = -T_{mavg} = -0.25T_P$ if the value i_{mavg} would occur without ripple (which provides the basis for the calculation of the relative on-times for the PWM) and the point when the PWM pattern becomes effective for the rectifier $T_{calc} + T_{PWM} = 1.5T_P$.

The discrete transfer function that has to be calculated in the DSP can be derived as

$$G_{pred}(z) = \frac{i_{pred}}{i_{mavg}} = 2.75 - 1.75z^{-1}, \tag{7}$$

therefore expressed in difference equation format

$$i_{pred,k} = 2.75 \cdot i_{mavg,k} - 1.75 \cdot i_{mavg,k-1}, \tag{8}$$

[1] This statement is valid if the PWM is updated only once per pulse period. For a double update mode the delay time introduced by the PWM operation is reduced to a quarter pulse period [5].

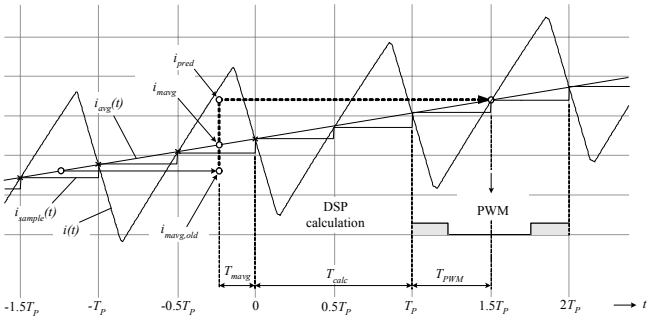

Fig. 6: Linear prediction of the forthcoming current value in order to compensate the delays due to the digital signal processing.

which has a derivative behaviour. The effect of the prediction in combination with the total transfer function of the digital processing as described above (cf. (6)) can be viewed in Fig. 5. The phase is increased by nearly $\Delta\varphi = \pi/4$ between 1kHz and 10kHz resulting in higher control bandwidth and/or stability of the inner control loop. The magnitude in this frequency band is increased by up to 6.5dB, therefore the current controller gain can be lowered accordingly in the design step compared to a system without prediction.

The effect of the prediction of the current can be seen in the step response of the inner current control loop, as depicted in **Fig. 7**. As described above, apparently the system stability is improved and/or the current overshoot is reduced while the inner control bandwidth is kept the same.

Since a sudden step of the load condition is directly changing the current reference value, the prediction is also improving the load disturbance behaviour. In the same way this method can be utilized for the prediction of the input filter capacitor voltages $u_{Cl,i}$. With this, also the disturbance rejection of the inner loop can be improved for disturbances from the mains side.

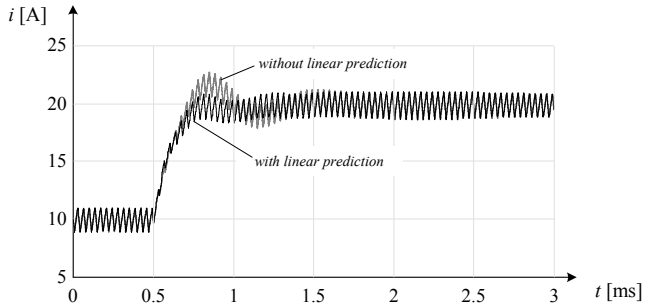

Fig. 7: Effect of the linear prediction of the DC current.

B. Smith Prediction

A more advanced prediction method including a model of the plant has been first presented in [8]. This so called Smith prediction is described briefly and applied to the system at hand.

Generally, as depicted in **Fig. 8**(a), the feedback of a control variable y including a total delay time T_x is changed according to

$$y' = y \cdot e^{-sT_x} + (1 - e^{-sT_x}) \cdot u \cdot G'_y(s), \tag{9}$$

where $y e^{-sTx}$ is the control variable containing the delay T_x, u is the controller output and $G'_y(s)$ is the model of the plant. As can be seen in Fig. 8(b), in the ideal case $G'_y(s) = G_y(s)$ the delay is moved outside of the plant that is seen by the controller, therefore the controller can be designed for considerably higher bandwidth and stability, respectively.

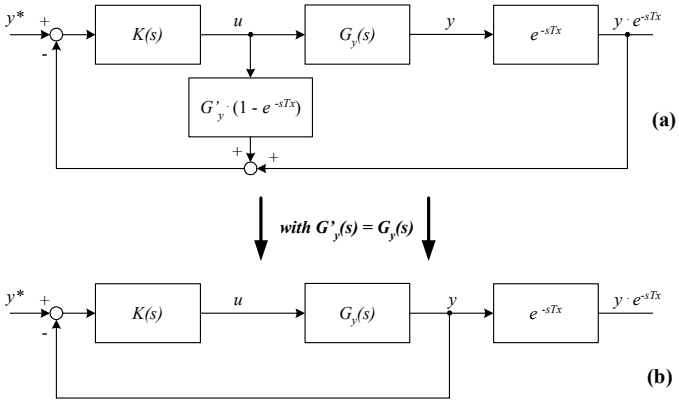

Fig. 8: Principle of the Smith prediction: general structure of the prediction method **(a)**; equivalent circuit showing that the delay is removed from the control loop **(b)**.

For the system at hand a prediction of both the DC current in the control feedback path and a prediction of the capacitor voltages in the active damping path has to be considered. In **Fig. 9**(a) the block diagram of the inner control loop including the Smith prediction feedback terms are depicted. Analogously to Fig. 8(b) the delay-free loops are shown in Fig. 9(b).

However, despite this technique seems to be promising two main problems are associated with the practical implementation:

- First, the transfer functions of the plants G'_i and G'_{uC1} have to be derived in every calculation step in the DSP, which results in a high computational effort. For example, for the system at hand the actual current value i_k of the pulse period k according to a simplified discretizised model $G'_i(z)$ is given in difference equation form by[2]

$$i_k = 3.56(m_k - 0.35m_{k-1} - 0.33m_{k-2} + 1.02m_{k-3}) + \\ +2.15i_{k-1} - 2.02i_{k-2} + 0.86i_{k-3} \quad . \quad (10)$$

  Additionally, the current value with $T_x = 1.75T_P$ has to be calculated

$$i_{k-1.75} = 3.56(m_{k-1.75} - 0.35m_{k-2.75} - 0.33m_{k-3.75} + 1.02m_{k-4.75}) + \\ +2.15i_{k-2.75} - 2.02i_{k-3.75} + 0.86i_{k-4.75} \quad . \quad (11)$$

  Since these values are not available for the proposed sampling method (cf. Fig. 3), e.g. sampling instants at $t = 0.25T_P$ and $t = 0.75T_P$ would have to be selected resulting in a total delay of $T_x = 2T_P$. With this, the equation

$$i_{k-2} = 3.56(m_{k-2} - 0.35m_{k-3} - 0.33m_{k-4} + 1.02m_{k-5}) + \\ +2.15i_{k-3} - 2.02i_{k-4} + 0.86i_{k-5} \quad (12)$$

  could be calculated. However, the current ripple suppression would then be reduced.

- The parameters in (10) - (12) given for a specific operating point are strongly dependent on the operating variables such as input and output voltage and output power. Additionally, the inductor values are dependent on the actual inductor current and the capacitors values are usually only given within a tolerance range. Since the effect of the prediction is strongly dependent on the accuracy of the model small inaccuracies in the model as always occurring due to the reasons described above have large influence on the control performance.

[2] An exact modelling of the plant would result in considerably higher computation effort which is dispensable due to model uncertainties and different operating point variations.

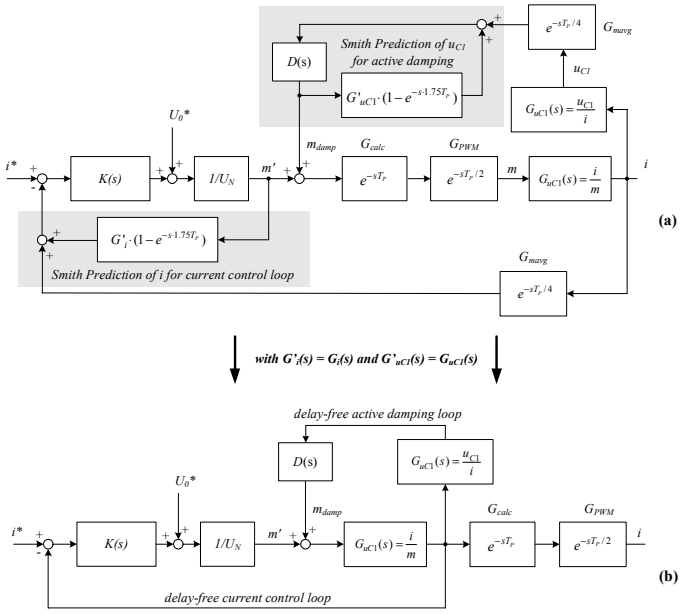

Fig. 9: Block diagram of the inner current loop including the Smith prediction feedback for the DC current and the input capacitor voltage **(a)**; equivalent circuit for a perfect model of the plant utilized in the feedback functions **(b)**.

In **Fig. 10** the effect of the Smith prediction on the inner current loop step response is illustrated. For the ideal case of a perfect modelling of the plant $G'_i = G_i$ and $G'_{uC1} = G_{uC1}$ the step response is only delayed by 1.75 pulse periods compared to a system containing no delays. Compared to the step response of the controlled system without prediction the reference tracking performance is obviously improved. However, due the simplification of the model the performance is significantly decreased, i.e. the step response is much slower.

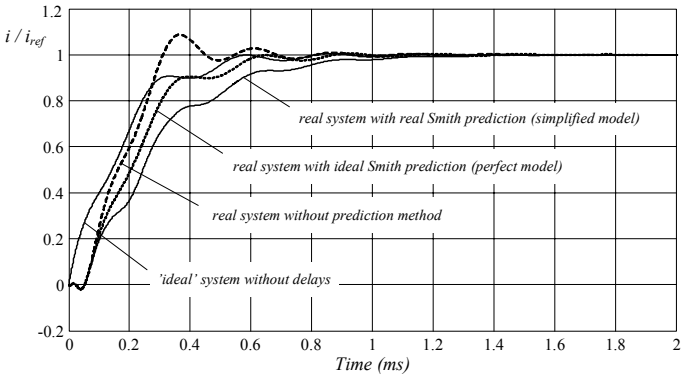

Fig. 10: Influence of the Smith prediction for perfect and simplified modelling of the plant, shown for the step responses of the inner current control loop for with $k_{P,I}$ = 15 [V/A].

V. Comparison of Prediction Methods

Summing up, it can be stated that the effort for the implementation of the Smith prediction, which is much higher when compared to the linear prediction, cannot be justified by better performance. The Smith prediction was originally developed for simple plants of low order systems, however, the buck rectifier systems with the input and

output filter does not fulfil this requirement. It is also seen that uncertainties in the model decrease the performance of the prediction significantly. Therefore, for compensating the delay times in the control of the buck rectifier the implementation of a linear prediction of the DC current and the input capacitor voltages without knowledge about the system to be controlled is sufficient and reasonable in terms of performance and implementation effort.

VI. Experimental Verification

The proposed control structure has been implemented on the DSP board and tested on a 5kW hardware prototype of the system (cf. **Fig. 11**). The two times oversampling, averaging, DSP control and PWM generation was implemented as described in section III. The linear prediction method that was proposed in section IV is obviously increasing the stability of the system (cf. **Fig. 12**) due to the compensation of the phase shift introduced by the delay times occurring in the digital system. For achieving the same overshoot-free step response of the system without prediction method the gain of the inner current controller would have to be reduced whereby the bandwidth of the current control would decrease.

Therefore, it could be shown that the stability of a system including delay times is improved by the linear prediction of the control quantities while the system control bandwidth is maintained.

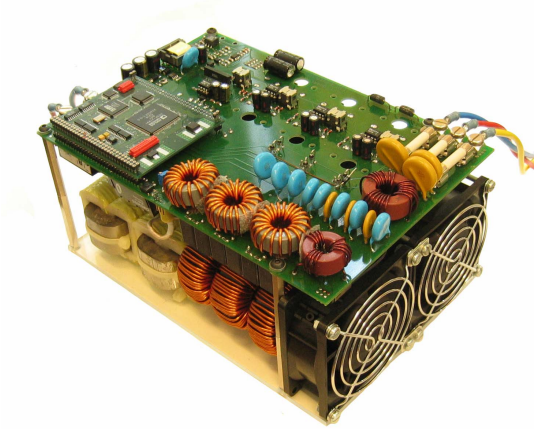

Fig. 11: 5kW prototype of the buck-type rectifier including DSP control board and EMC input filter. Overall dimensions: 240mm x 160mm x 120mm.

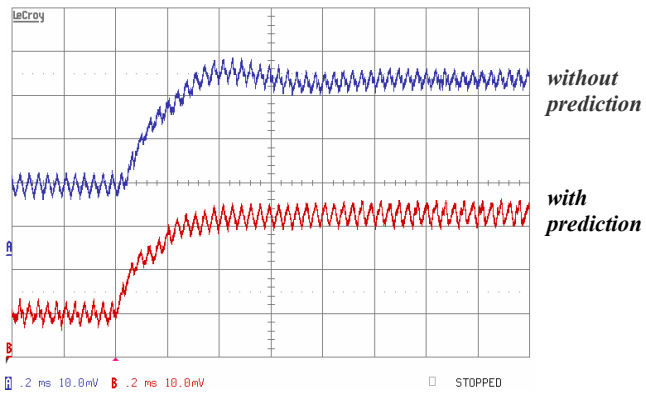

Fig. 12: Current waveforms of the closed loop system for a step in the current reference of 4.6A (performed by a load step) without prediction method (upper curve, channel A) and with linear prediction (lower curve, channel B) (current scale: 2A/div, time scale: 200µs/div).

VII. Conclusions

The digital control of a three-phase rectifier system was analyzed in this paper. First, the origins of relevant delay times in the control loop were found to be the sampling of the control quantities, the calculation time of the control program in the DSP, and the sample-and-hold function of the PWM modulator.

It was shown that these delay times introduce a large phase shift of nearly $\varphi = \pi/2$ already one decade below the switching frequency, what reduces the phase margin and the stability and therefore the achievable bandwidth of a controller. In order to reduce these phase shift two prediction methods, namely a linear prediction and the Smith prediction, are analyzed and compared.

The Smith prediction ideally completely compensates the delay times, but requires a precise model of the system to be controlled resulting in a high implementation effort. It could be shown that the performance of this prediction technique is highly sensitive on the accuracy of the modelling. In contrast, a linear prediction cannot compensate completely the introduced phase shift, but does not require any information about the model and is therefore characterized by a significantly lower implementation. Taking this into account it is concluded that for a system with high system order (due to the complex model) - as it is usually the case for converter systems with input and output filters - the effort of a Smith prediction is not worthwhile if compared to the one of a linear prediction method.

Measurements on a hardware prototype could verify that the linear prediction method clearly increases the stability of the system by counteracting the delay times introduced by the digital control.

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