Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier

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***Abstract*—A three-phase three-switch buck-type pulsewidth modulation rectifier is designed for telecom applications in this paper. The rectifier features a constant 400-V output voltage and 5-kW output power at the three-phase 400-V mains. The principle of operation and the calculation of the relative on-times of the power transistors are described. Based on analytical relationships the stresses of the active and passive components are determined and the accuracy of the given calculations is verified by digital simulations. Exemplarily, a 5-kW power converter is then designed based on the analytical expressions and on switching loss measurements from a hardware prototype constructed with insulated gate bipolar transistor/diode power modules. The loss distribution of the components, the total efficiency, and the junction temperatures of the semiconductors are then evaluated in dependency on the operating point. Finally, the trade-off between the selected switching frequency and the admissible power range for the realized design is shown and a total efficiency of 95.0% is measured on the hardware prototype, where an excellent agreement with the theoretically evaluated efficiency is shown.**

***Index Terms*—AC–DC conversion, insulated gate bipolar transistor (IGBT), pulsewidth modulation (PWM).**

I. Introduction

THE design of an electronic system in the industry is often based on the experience of the designer or even a trial-and-error method. Obviously, this does not lead to an optimum design, whereas analytical calculations of the component stresses [1] provide a clear and general guideline for the component selection and for the converter design. Furthermore, analytical calculations give insight in the dependency of the design on the operating parameters (input voltage, output power, switching frequency, etc.) and allow the design to be easily extended to other specifications.

As an application case a front-end converter for telecommunications power supply modules shall be dimensioned that should have the following features: constant output voltage of $U_0 = 400$ V for operation at the 400 V mains ($U_{N,l-l,\mathrm{rms}} = 400\ \mathrm{V} \pm 10\%$), output power of $P_0 = 5$ kW, sinusoidal mains currents, unity power factor, high power density and simplicity of the power circuit structure.

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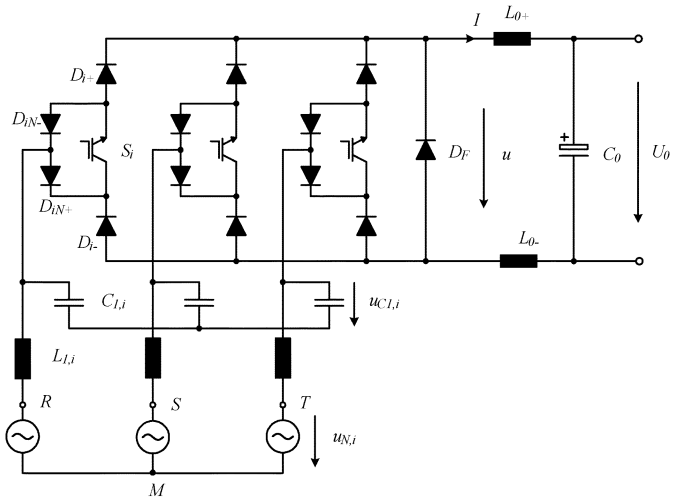

Fig. 1. Topology of the three-phase three-switch buck-type rectifier.

Basically, two structures are possible for performing this task: i) a boost-type input rectifier (e.g., Vienna rectifier, [2]), that typically features two 400-V output voltages with a three-level isolated dc–dc converter or two isolated dc–dc output stages and ii) a buck-type input rectifier (conventionally six-switch topologies as proposed in [3]–[6]) with only one two-level isolated dc–dc converter output stage. If the input stage of the latter is realized as a three-switch topology (cf. Fig. 1) it shows a considerably lower system complexity as compared to the boost-type structure. In particular, the number of utilized active and passive components is much lower. Furthermore, there is no middle-point that has to be stabilized, as this is the case for the boost-type structures especially for the case of asymmetrical load of the two parallel output stages. Further system advantages are the potential of a direct start-up and the overcurrent protection in case of an output short circuit. Therefore, this topology is of high interest for these applications and could also be attractive for future electric aircraft applications or as power supplies for process technology.

The three-switch buck rectifier topology was first proposed in [7]. In [8] and [9], aspects of the system modulation and control have been treated. The application of the topology used as an active filter is discussed in [10]. In [11] and [12], the function of the 12-pulse rectifier is emulated by interleaving of two three-switch buck rectifier stages which leads to a reduction of the input filtering requirements. The addition of a dc–dc output boost-stage has been proposed in [13] in order to maintain 400-V output voltage for a wide input voltage range and for the case of unbalanced mains as, e.g., the loss of one phase. A modulation scheme aiming for minimum switching losses and

minimum input current distortion has been proposed in [14], a parallel operation of two dc-side connected rectifiers has been discussed in [15], and a common mode (CM) and differential mode (DM) input filter has been designed in [16] and [17].

However, in none of these publications a complete system design has been performed discussing current and voltage stresses and selection criterias for the passive and active components of the rectifier.

Therefore, in this paper the design of the three-phase three-switch buck-type rectifier system is discussed in detail. After a description of the basic principle of operation of the rectifier in Section II the stresses of the semiconductor components and of the passive components are calculated analytically in Section III with dependency on the input current amplitude and the voltage transfer ratio of the converter. The validity of the theoretical considerations is proven in Section IV by digital simulations. In Section V, the dimensioning of the system is described and illustrated by a numerical example and the active and passive components are selected. The performance of the designed system is discussed in Section VI, the power loss distribution is shown and the total efficiency is derived. Section VII presents the maximum output power, according to thermal limitations of the power semiconductors that can be achieved for the selected design as a function of the switching frequency. Finally, in Section VIII the calculated efficiency of the designed converter is compared with measurements on a hardware prototype and the correctness of the design procedure is verified as well as the good performance of the three-phase three-switch buck rectifier is shown.

II. Principle of Operation

In the following, the basic principle of operation of the three-phase three-switch buck rectifier is explained based on some simplifying assumptions and the duty cycles of the power transistors are derived based on space vector calculations.

A. Assumptions

For the derivation of the relative on-times of the three buck transistors S_i (with $i = R, S, T$) the following assumptions are made for clarity and facilitation of calculations.

- The filter capacitor voltages $u_{C1,i}$ at the input of the rectifier are of purely sinusoidal shape and are in phase with the mains phase voltages $u_{C1,i} \sim u_{N,i}$ with

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\omega_N t) \\ u_{N,S} &= \hat{U}_N \cos(\omega_N t - 2\pi/3) \\ u_{N,T} &= \hat{U}_N \cos(\omega_N t + 2\pi/3) \end{aligned} \tag{1}$$

  where ω_N is the mains angular frequency. Therefore the voltage drops across the filter inductors, which have to be inserted for fulfilling the electromagnetic compatibility (EMC) regulations [19], are neglected.
- The mains currents are assumed to be equal to the fundamental component of the rectifier input currents $i_{N,i} \sim i_{\mathrm{rec},(1),i}$, therefore the reactive currents due to the filter capacitors are also neglected.
- The current I in the dc output inductors L_{0+}, L_{0-} is assumed to be constant, i.e., the high frequency ripple due to the switching operation is neglected.

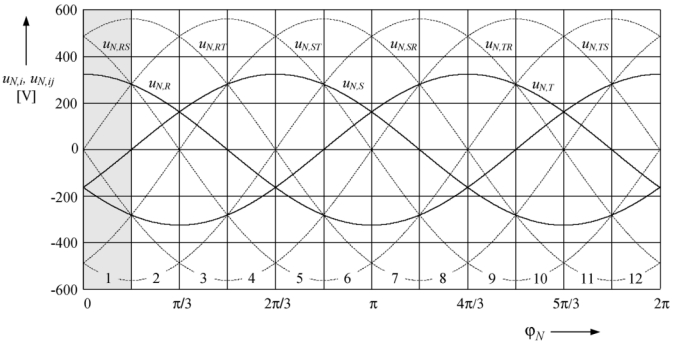

Fig. 2. Mains phase voltages $u_{N,i}$, line-to-line voltages $u_{N,ij}$ ($u_{N,ij} = u_{N,i} - u_{N,j}$ with $i = R, S, T$, and $j = R, S, T$, and $i \neq j$), and mains sectors 1–12 being defined by the different relations of the instantaneous values of the mains phase voltages for $U_{N,l-l,\mathrm{rms}} = 400$ V.

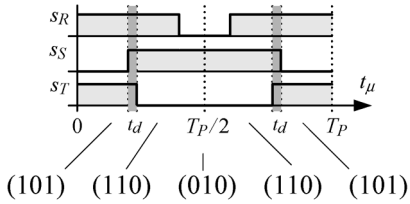

Fig. 3. Switching pattern shown for one pulse period according to an optimum modulation method regarding switching losses, ripple values, and mains current quality [14]. The depicted switching pattern is shown here exemplarily for an instant within the first mains sector ($0° < \varphi_N < 30°$). The state (111) between the two active states (101) and (110) has to be employed for a short time period t_d to preventing a freewheeling state, which would result in additional switching losses. However, for the calculation of the relative on-times this short overlapping time can be disregarded for sake of simplicity.

For the analysis of the conduction states, the derivation of the current space vector and the calculation of the relative turn-on times symmetric mains conditions are assumed.[1] The waveforms of the phase and line-to-line mains voltages are depicted in Fig. 2, where the mains period is divided into twelve 30°-wide sectors. The following calculations are based on the analysis of the first sector ($0° < \varphi_N < 30°$ with $\varphi_N = \omega_N \cdot t$), which is characterized by the mains phase relation $u_{N,R} > 0 > u_{N,S} > u_{N,T}$. However, for the remaining sectors the calculations can be accomplished in an similar manner.

B. Modulation, Conduction States and Current Space Vectors

A modulation method was developed in [14] that ensures minimum switching-losses, minimum ripple values of the input capacitor voltages and of the output inductor current as well as low distortion of the mains currents at the sector boundaries. According to this modulation, each pulse interval comprises two active states and a freewheeling state, arranged symmetrically about the middle of the pulse interval. For example, in the first mains sector $(0° < \varphi_N < 30°)$ the switching state sequence (101)-(110)-(010)-(110)-(101) is applied (cf. Fig. 3), where $j = (s_R s_S s_T)$ indicates a combination of the three switches S_i and $s_i = 1$ means that the according switch is turned on and $s_i = 0$ indicates an off-state of the according switch.

[1]For achieving ohmic mains behavior also in case of asymmetric mains conditions the explained modulation method can still be utilized, however, additionally the control structure presented in [20] has to be employed.

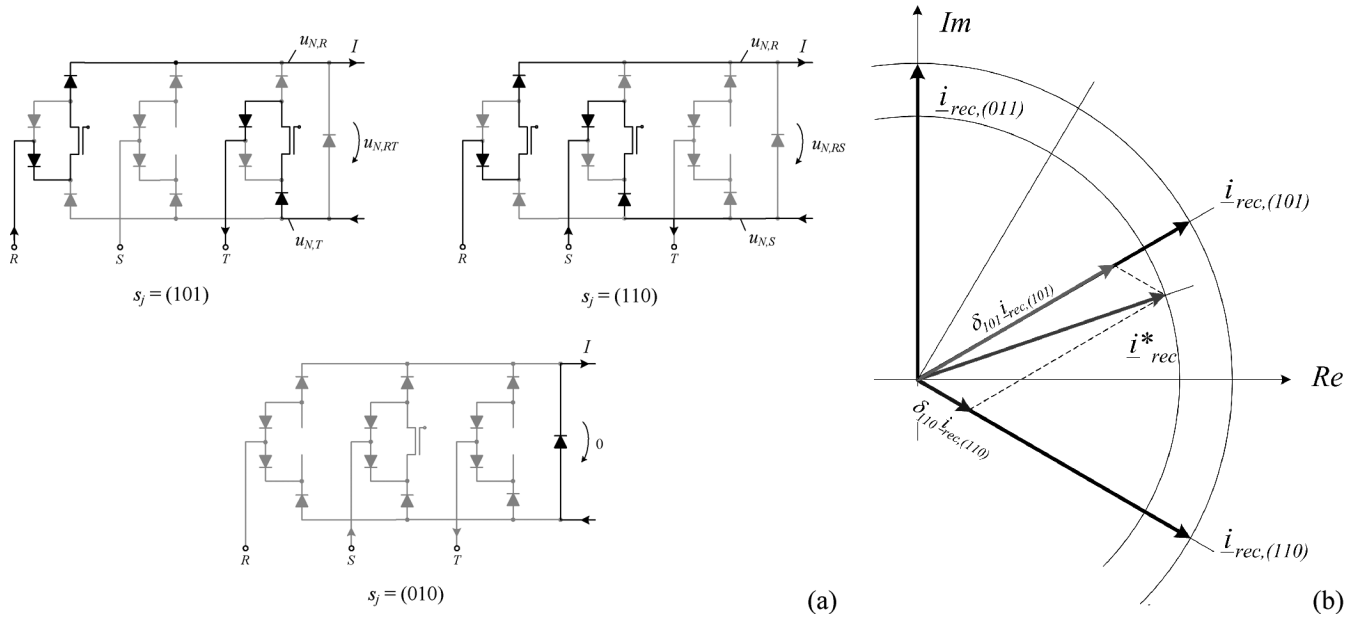

Fig. 4. Conduction states of the buck-type input stage for the switching states (cf. Fig. 3) occurring in the first mains sector ($0< \varphi_N < 30°$); available current space vectors within the first mains sector and composition of the resulting input current space vector by weighting and vectorial summing of the current space vectors.

The current flow in the bridge legs of the rectifier is shown in Fig. 4(a) for these switching states. According to the actual switch combination the dc link current I impressed by the inductors L_{0+}, L_{0-} is distributed to two of the input phases or the freewheeling diode D_F. With this, the input current space vectors can be calculated for each of the before-mentioned switching states. Generally, the space vector of three-phase quantities (e.g., for the rectifier input current) is defined as

$$\underline{i}_{\mathrm{rec}} = \frac{2}{3}(i_{\mathrm{rec},R} + e^{j2\pi/3}\cdot i_{\mathrm{rec},S} + e^{j4\pi/3}\cdot i_{\mathrm{rec},T}). \quad (2)$$

For the switching state j =(101) the rectifier input currents are $i_{\mathrm{rec},R} = I$, $i_{\mathrm{rec},S} = 0$ and $i_{\mathrm{rec},T} = -I$ [cf. Fig. 4(a)], therefore, the rectifier input current space vector for this switching state results in

$$\underline{i}_{\mathrm{rec},(101)} = I \cdot \frac{2}{\sqrt{3}} e^{j\pi/6}. \quad (3)$$

Analogously, the two remaining space vectors can be calculated

$$\underline{i}_{\mathrm{rec},(110)} = I \cdot \frac{2}{\sqrt{3}} e^{-j\pi/6} \quad (4)$$

$$\underline{i}_{\mathrm{rec},(010)} = 0. \quad (5)$$

With these three space vectors a resulting input current space vector $\underline{i}^*_{\mathrm{rec}}$ can be produced [cf. Fig. 4(b)] so that it is in phase with the mains voltage vector $\underline{u}_N$ and has the required amplitude according to the actual power demand. For the calculation of the required relative turn-on times of the power transistors the following conditions have to be fulfilled.

- The fundamental components of the three rectifier input currents denominated by the index (1), that are formed by the dc link current and the relative on-times have to be in phase with (i.e., proportional to) the three input voltages

$$\begin{aligned} i_{\mathrm{rec},R,(1)} &= I\cdot(\delta_{101}+\delta_{110}) && \sim u_{N,R} \\ i_{\mathrm{rec},S,(1)} &= -I\cdot\delta_{110} && \sim u_{N,S} \\ i_{\mathrm{rec},T,(1)} &= -I\cdot\delta_{101} && \sim u_{N,T} \end{aligned} \quad (6)$$

  where δ_{101} and δ_{110} are the relative on-times of the active states s_i =(101) and s_i =(110), respectively.
- During the two active switching states [in the case at hand (101) and (110)] the according line-to-line voltages $u_{C1,RT}$ and $u_{C1,RS}$ appear at the freewheeling diode (cf. Fig. 4). The relative on-times have to be adjusted in order to form the required dc link voltage according to the actual power demand

$$u^* = \delta_{101}\cdot u_{N,RT} + \delta_{110}\cdot u_{N,RS}. \quad (7)$$

- The sum of the relative on-times during one switching period has to be equal to one

$$\delta_{101} + \delta_{110} + \delta_{FW} = 1 \quad (8)$$

  where δ_{FW} is the relative on-time of the freewheeling state.

With these conditions and the definition of the modulation depth

$$M = \frac{2}{3}\cdot\frac{u^*}{\hat{U}_N} \quad (9)$$

the relative on-times for the first sector can be calculated

$$\delta_{101} = -M\cdot\frac{u_{N,T}}{\hat{U}_N} \quad (10)$$

$$\delta_{110} = -M\cdot\frac{u_{N,S}}{\hat{U}_N} \quad (11)$$

$$\delta_{FW} = 1 - M\cdot\frac{u_{N,R}}{\hat{U}_N}. \quad (12)$$

The on-times for the remaining sectors can be derived in an analogous manner. As can be shown easily, the effective conduction times α_i of the three switches—and independently of the utilized modulation method—have to be for all sectors

$$\alpha_i = M \cdot \frac{|u_{N,i}|}{\hat{U}_N}. \tag{13}$$

III. System Design

In this section, the stresses of the active and passive components are calculated analytically with dependency on the operating parameters of the converter. This is the essential part in the system design as it provides the basis for the selection of the appropriate components.

A. Voltage Stresses

The voltage stresses on the active and passive components can be determined easily. The maximum line-to-line input voltage is

$$U_{N,l-l,\max} = \sqrt{2} \cdot (400\ \text{V} + 10\%) = 622\ \text{V}. \tag{14}$$

However, for the selection of the blocking capability of the insulated gate bipolar transistors (IGBTs) and the power diodes additionally an ample margin (around 50%) has to be considered, since the LC input filter usually has low passive damping in order not to decrease the suppression of the high frequency harmonics that is required for compliance with EMC standards. A potential active damping of the input filter is not effective in case the rectifier is directly connected to the mains in off-state.

The output voltage is controlled to the constant value $U_0 = 400$ V, therefore the inductor L_0 and capacitor C_0 are selected for this value plus a control overshoot margin. Since the output voltage control is typically very slow and stable, an overshoot margin of 10% is usually sufficient.

B. Current Stresses

The calculation of the current stresses is more involved as compared to the voltage stresses, therefore some assumptions for keeping the analysis to the essentials are done in advance.

1) Assumptions: The analysis of the component stresses is based on the following assumptions:

- purely sinusoidal, symmetric mains phase voltages, cf. (1);
- negligible fundamental voltage drops at the filter inductors, therefore $u_{C1,i} \sim u_{N,i}$;
- constant load current I_0;
- a switching frequency f_S being much higher than the mains frequency f_N. For achieving a good accuracy of the analytical calculations, $f_S > 200 f_N$ is set [1].

For the calculation of the semiconductor current stresses the last condition translates to a neglecting of the ripple values of the passive components, i.e., negligible voltage ripple at the input filter capacitors and negligible ripple of the dc inductor current I.

2) Analysis Method: In order to dimension the active and passive components it is necessary to calculate the average and rms values of the device currents. For an exact calculation of the global average current values the contributions of each pulse interval have to be determined and summed over a whole mains period.

As shown in [1], the summation can be replaced by an integration of the local averaged values over the mains period

$$I_{i,\text{avg}} = \frac{1}{2\pi} \int_0^{2\pi} \left(\frac{1}{T_P} \int_0^{T_P} i_i(\varphi_N, t_\mu) dt_\mu \right) d\varphi_N \tag{15}$$

where

$$\varphi_N = \omega_N t \tag{16}$$

defines the actual position of a pulse interval within a mains period. Analogously, the square of the global rms value can be found by integration of the square local rms value

$$I^2_{\text{i,rms}} = \frac{1}{2\pi} \int_0^{2\pi} \left(\frac{1}{T_P} \int_0^{T_P} i_i^2(\varphi_N, t_\mu) dt_\mu \right) d\varphi_N. \tag{17}$$

With this, the component stresses can be evaluated analytically, and this allows an analysis of the influence of the system parameters (output power, input voltage, switching frequency, etc.) on the dimensioning of the rectifier. In order to check the accuracy of the analytical expressions in Section IV the results will be compared with numerical calculations through digital simulations of the converter circuit.

3) Power Semiconductor Current Stresses: As a first step, the local average values

$$i_{i,\text{avg}} = \frac{1}{T_P} \int_0^{T_P} i_i(\varphi_N, t_\mu) dt_\mu \tag{18}$$

of the power semiconductors are calculated. For indicating the difference between local (according to a pulse period) and global (according to a mains period) values the local average values are written in lowercase letters and the global values in uppercase ones. With the assumption of a constant inductor current I and with (13) the local average value of the current in the transistor S_R is derived

$$i_{SR,\text{avg}} = \frac{1}{T_P} \int_0^{\delta_R \cdot T_P} I\, dt_\mu = I \cdot \delta_R = I \cdot M \cdot |\cos\varphi_N|. \tag{19}$$

The time behavior is shown in Fig. 5 along with the time behavior of the local average values of the bridge leg diodes and the freewheeling diode. Through the integration of (19) over one mains period according to (15) the global average value of the transistor current $I_{SR,\text{avg}}$ is calculated as

$$I_{SR,\text{avg}} = \frac{1}{2\pi} \int_0^{2\pi} I \cdot M \cdot |\cos\varphi_N| d\varphi_N = \frac{2}{\pi} I \cdot M = \frac{2}{\pi} \hat{I}_N. \tag{20}$$

Due to the before-mentioned phase symmetry it is sufficient to consider only one phase, the integration of the local average values of the other phases will lead to the same result. In an analogous manner the local rms value of the transistor current

$$i^2_{SR,\text{rms}} = \frac{1}{T_P} \int_0^{\delta_R \cdot T_P} I^2 dt_\mu = I^2 \cdot \delta_R = I^2 \cdot M \cdot |\cos\varphi_N| \tag{21}$$

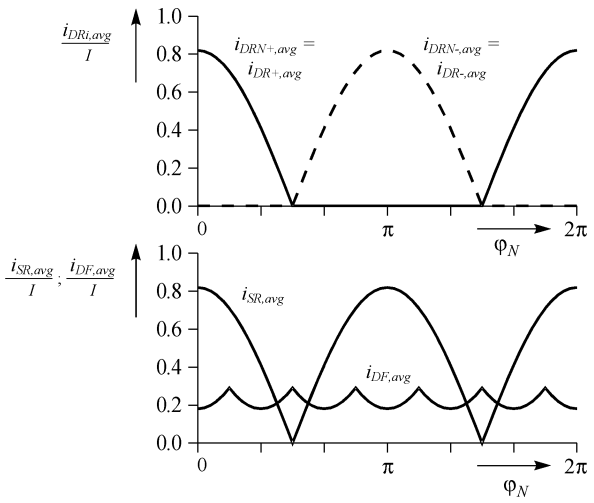

Fig. 5. Time behavior of the of the local average values of the currents of the power transistor S_R, the bridge leg diodes D_{RN+}, D_{R+}, D_{RN-}, D_{R-} and the freewheeling diode D_F for a modulation index of $M = 0.82$ (which corresponds to an output voltage of $U_0 = 400$ V for a line-to-line mains voltage of $U_{N,l-l,\mathrm{rms}} = 400$ V).

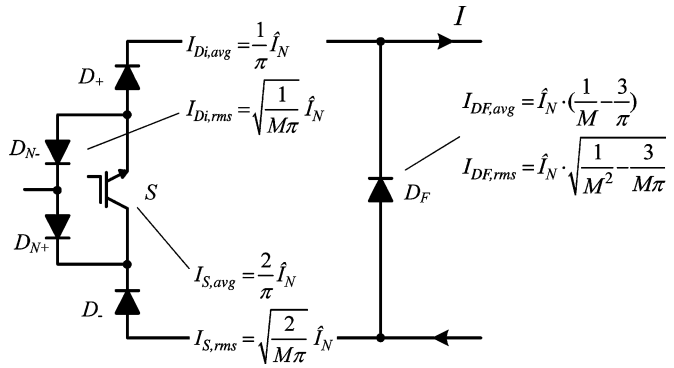

Fig. 6. Analytical approximations of average and rms values of the component currents for the three-phase three-switch buck rectifier in dependency on the mains phase current amplitude $\hat{I}_N$ and the current transformation ratio $M = \hat{I}_N/I$.

and the global rms value of the transistor current according to (17) are derived

$$I_{SR,\mathrm{rms}}^2 = \frac{1}{2\pi}\int_0^{2\pi} I^2 \cdot M \cdot |\cos\varphi_N| d\varphi_N = \frac{2}{\pi} I^2 \cdot M = \frac{2}{M\pi}\hat{I}_N^2. \tag{22}$$

In a similar way the average and rms values of the currents in the bridge leg diodes and in the freewheeling diode can be evaluated. The resulting average and rms values for all devices are given in Fig. 6.

4) Passive Component Current Stresses:

Inductor L_0: The dc output inductor L_0 is designed in such a manner that the peak-to-peak value of the dc output inductor current ripple $\Delta i_{L0,pp,\max}$ is limited to a given value, which is typically set to 20% of the dc output inductor current. The peak-to-peak value of the dc output inductor current ripple can be calculated via

$$\Delta i_{L0,pp} = \frac{U_0}{L_0} \cdot \frac{(1-M)}{f_S}. \tag{23}$$

With this, the dc output inductor L_0 can be selected according to

$$L_0 \geq \frac{U_0}{\Delta i_{L0,pp,\max}} \cdot \frac{(1-M_{\min})}{f_S} \tag{24}$$

where $M_{\min}$ is the minimum modulation index (occurring at maximum mains voltage). The rms value of the dc output inductor current ripple can be calculated through

$$\Delta I_{L0,\mathrm{rms}}^2 = \frac{1}{T_P}\int_0^{MT_P}\left(I - \frac{\Delta i_{\mathrm{L0,pp}}}{2} + \Delta i_{L0,pp}\cdot\frac{t}{MT_P}\right)^2 dt + \frac{1}{T_P}\int_0^{(1-M)T_P}\left(I + \frac{\Delta i_{L0,pp}}{2} - \Delta i_{L0,pp}\cdot\frac{t}{(1-M)T_P}\right)^2 dt \tag{25}$$

by using a dc–dc equivalent circuit of the rectifier system, i.e., assuming a linear increase of the inductor current during the active switching states and a linear decrease during the freewheeling state. Evaluation of (25) results in

$$\Delta I_{L0,\mathrm{rms}}^2 = I^2 + \frac{\Delta i_{L0,pp}^2}{12}. \tag{26}$$

Capacitor C_0: The output capacitor C_0 can either be selected according to the following three criterias:

i) C_0 is selected in order to limit the peak-to-peak value of the output voltage ripple $\Delta u_{C0,pp,\max}$ to a given value

$$C_0 \geq \frac{U_0}{L_0} \cdot \frac{(1-M_{\min})}{8 \cdot f_S^2 \cdot \Delta u_{C0,pp,\max}} \tag{27}$$

ii) C_0 is designed with respect to a maximum allowable voltage drop Δu_0 (e.g., 2% of the output voltage) occurring at a load current step ΔI_0 from 0 A to rated current ($I_0 = 12.5$ A). In order to limit the output capacitor to a reasonable value a load current feedforward scheme is considered in the control structure, wherefore the load current step causes an immediate change in the dc current reference i_{ref} of an inner current control loop. Due to the voltage across the dc link inductor

$$u_{L0} = U - U_0 = 1.5 \cdot \hat{U}_N - U_0 \tag{28}$$

the rate of rise of the dc link current[2] is limited to

$$\frac{\Delta I}{\Delta t} = \frac{u_{L0}}{L_0} \tag{29}$$

which causes an output voltage dip

$$\Delta u_0 = \frac{Q}{C_0} = \frac{\Delta I \cdot \Delta t}{2 \cdot C_0} = \frac{1}{2 \cdot C_0} \cdot \frac{(\Delta I)^2 \cdot L_0}{u_{L0}}. \tag{30}$$

[2]assuming a linear rate of rise of the dc link current.

With this, the output capacitor has to be selected according to

$$C_0 \geq \frac{(\Delta I)^2 \cdot L_0}{2 \cdot \Delta u_0 \cdot (1.5 \cdot \hat{U}_{N,\min} - U_0)}. \quad (31)$$

The output capacitor current ripple $\Delta i_{C0,pp}$ is equal to the dc output inductor current ripple, if a purely resistive load is assumed. Hence the rms value of the output capacitor is

$$\Delta I^2_{C0,\mathrm{rms}} = \frac{\Delta i^2_{L0,pp}}{12} \quad (32)$$

iii) C_0 is selected according to the hold-up time requirement, where a maximum output voltage dip Δu_0 for the case of a failure of one or more main phases during a time span Δt_{hold} is defined. For a constant output power and a voltage dip being much lower than the output voltage $\Delta u_0 \ll U_0$ the output capacitance value is derived by

$$C_0 = \frac{P_0}{U_0 \cdot \Delta u_0} \Delta t_{\mathrm{hold}}. \quad (33)$$

Filter Capacitor C_1: The input filter capacitor can be designed via the maximum peak-to-peak value of the filter capacitor voltage ripple

$$\Delta u_{C1,pp} = \frac{I \cdot M \cdot (1 - M)}{C_1 \cdot f_S} \quad (34)$$

where the dc inductor ripple is not considered. On the other hand, the reactive power Q_C usually has to be limited to (5...10)% of the rated power in order to ensure high power factor also in case of low power applications

$$C_1 \leq \frac{(0.05 \ldots 0.1) \cdot P_N}{\omega_N \cdot U^2_{N,l-l,\mathrm{rms}}}. \quad (35)$$

The rms value of the filter capacitor current consists of the high-frequency part of the rms value of the rectifier input current and the fundamental reactive current in the capacitor

$$\begin{aligned} I^2_{C_1,\mathrm{rms}} &= I^2_{\mathrm{rec},(HF),\mathrm{rms}} + I^2_{C1,(1),\mathrm{rms}} \\ &= I^2_{\mathrm{rec},\mathrm{rms}} - I^2_{\mathrm{rec},(1),\mathrm{rms}} + I^2_{C1,(1),\mathrm{rms}} \\ &= I^2_{S_i,\mathrm{rms}} - I^2_{N,(1),\mathrm{rms}} + I^2_{C1,(1),\mathrm{rms}} \\ &= \hat{I}^2_N \cdot \frac{2}{M \cdot \pi} - \left(\frac{\hat{I}_N}{\sqrt{2}}\right)^2 + (\omega_N \cdot C_1 \cdot U_{N,\mathrm{rms}})^2 \\ &= \hat{I}^2_N \cdot \left(\frac{2}{M \cdot \pi} - \frac{1}{2}\right) + (\omega_N \cdot C_1 \cdot U_{N,\mathrm{rms}})^2. \end{aligned} \quad (36)$$

Filter Inductor L_1: The input filter inductor is designed basically according to the following guidelines.

— EMC requirements: With a switching frequency outside of the audible range the harmonic requirements EN 61000-3-2 (until 2 kHz, [18]) are not the determining factor for the selection of the input filter inductor. However, the high frequency suppression of the input current harmonics (measured in dBμV at the 50-Ω LISN resistor) has to comply with the EMC requirements [19]. As shown in [16] the required suppression is around 93 dB, which translates to the necessity of a two-stage filter topology, where the first filter stage (that is mainly determining the filter volume and losses) formed by L_1 and C_1 has a cut-off frequency around 10% of the switching frequency. For a given input filter capacitor C_1 the input filter inductor can then be calculated by

$$f_{filt} = \frac{1}{2\pi \cdot \sqrt{L_1 C_1}} \approx 0.1 \cdot f_S. \quad (37)$$

— System Control: From the EMC point of view it is desirable to have a strong suppression of the high frequency harmonics, which means big values of L_1 and C_1. Apart from the fact that this is conflicting with the aim to achieve high power density it also limits the control bandwidth by a low filter cut-off frequency according to (37).

IV. Accuracy of the Calculations

It is important to ensure the accuracy of the calculations to be within a certain percentage range, i.e. that a certain deviance between the analytical expressions and the actual values is not exceeded. Mainly the calculation error arises from the negligence of the ripple values of the input capacitor voltage $\Delta u_{C1,pp}$ and the dc link current $\Delta i_{L0,pp}$. Therefore, it is analyzed in this section to what extent the neglect of the ripple values is taking influence on the accuracy of the formulas given in the previous section.

In order to determine the accurate values of the component stresses by digital simulations an appropriate switching frequency and the values of the passive components according to (23)–(36) have to be selected. The switching frequency shall be outside of the audible frequency range ($f_S > 20$ kHz) and sufficiently high for ensuring a high bandwidth of the system control (see selection of the input filter inductor in Section III-B4). On the other hand, the switching losses which are increasing for higher switching frequencies should be kept low in order to achieve high efficiency. Additionally, a lower switching frequency reduces the filtering requirements for fulfilling the EMC standards [16], [21]. The latter is an inherent behavior of buck-type topologies, since for lower switching frequencies the current spectrum is shifted to lower frequencies and the harmonics at the lower limit of the EMC measurement range at $f = 150$ kHz show lower amplitudes due to the decrease of the harmonics by $\sin(f)/f$.

Taking all this into account, a switching frequency of $f_S = 28$ kHz is selected in order to achieve a good compromise between high efficiency and high power density and in order to keep the fifth switching frequency harmonic (140 kHz) below the lower limit of the EMC measurement range (150 kHz) defined in CISPR 22 [19].

With $f_S = 28$ kHz the values of the passive components are selected as $L_0 = 2$ mH, $C_0 = 750$ μF, and $C_{1,i} = 6.8$ μF following the design rules given in Section III-C.

In Table I, the simulated values of the average and rms component stresses where ripple values are explicitly taking influence are compared with the values resulting from the formulas given in Section III for $U_{N,l-l,\mathrm{rms}} = 400$ V, $U_0 = 400$ V, $P_0 = 5$ kW, $f_S = 28$ kHz. It can be seen that the accuracy of all calculations is within a 6% range. Therefore, it is proven that the

TABLE I
COMPARISON OF PASSIVE AND ACTIVE COMPONENT STRESSES DETERMINED BY ANALYTICAL CALCULATIONS AND DIGITAL SIMULATIONS OF THE POWER CIRCUIT OF THE BUCK RECTIFIER

	Analytical Calculation [A]	Digital Simulation [A]	Deviation [%]
$i_{SR,avg}$	6.52	6.63	-1.7
$i_{SR,rms}$	9.03	9.12	-1.0
$i_{Di,avg}$	3.26	3.32	-1.8
$i_{Di,rms}$	6.39	6.45	-0.9
$i_{DF,avg}$	2.71	2.56	5.8
$i_{DF,rms}$	5.82	5.66	2.8
$i_{C1,rms}$	5.41	5.49	-1.4
$i_{L0,rms}$	12.51	12.51	0.0

formulas derived in Section III provide a correct basis for a converter dimensioning as carried out in the subsequent section.

V. DIMENSIONING OF THE CONVERTER

In order to exemplify the analytical considerations the rectifier is dimensioned according to the specifications given in Section I. For the selection of the components the worst case operating condition has to be considered. For the current stresses of the transistors and the bridge leg diodes (cf. Fig. 6 with $M = \hat{I}_N/I$) the worst case is given by the highest modulation index ($M_{\max} = 0.91$), hence, the minimum input voltage $U_{N,l-l,\mathrm{rms}} = 360$ V

$$I_{SR,\mathrm{rms,max}} = I \cdot \sqrt{\frac{2M_{\max}}{\pi}} = 9.51 \text{ A} \tag{38}$$

$$I_{Di,\mathrm{rms,max}} = I \cdot \sqrt{\frac{M_{\max}}{\pi}} = 6.73 \text{ A} \tag{39}$$

while for the current stresses of the free-wheeling diode (cf. Fig. 6) the worst case is given by the lowest modulation index $M_{\min} = 0.74$ ($U_{N,l-l,\mathrm{rms}} = 440$ V)

$$I_{DF,\mathrm{rms,max}} = I \cdot \sqrt{\left(1 - \frac{3M_{\min}}{\pi}\right)} = 6.77 \text{ A}. \tag{40}$$

According to (14) and considering a margin for the overvoltage due to the turn-off and for an overshoot of the rectifier input voltage in case of low passive damping of the input filter IGBTs and diodes with 1200-V blocking capability have been chosen. The selected power semiconductors are listed in Table II along with their specifications of the selected passive components. Finally, three power modules comprising each the components of one bridge leg (IGBT and four diodes) are utilized in order to reduce the mounting effort and reduce wiring inductances (cf. Fig. 7).

VI. PERFORMANCE EVALUATION

In the following, the performance of the rectifier, which has been designed in the previous section, is evaluated by calculation of the power losses. While conduction losses can be derived very accurately by means of analytical expressions based on the average and rms current stresses derived in Section III,

TABLE II
ACTIVE AND PASSIVE COMPONENTS SELECTED FOR THE REALIZATION OF THE POWER PART OF THE THREE-PHASE THREE-SWITCH BUCK RECTIFIER SYSTEM

Component	Specification
IGBT S_i	IGBT Module VUI31-12N1, 1200V,65A U_{CE0}=1V, r_{CE}=60mΩ
Diodes D_i,	Module Diode VUI31-12N1, 1200V,25A U_F=1.65V, r_D=18mΩ
Diode D_F	RHRP30120 Diode @1200V,30A U_F=0.97V, r_D=24mΩ
Output Inductor L_0	Honeywell Metglas Powerlite AMCC-16B 2 x 1mH@20A N = 56 turns, 14AWG
Output Capacitor C_0	Epcos B43501, 5 x 150µF@450VDC $ESR_{28kHz,60°C}$ = 310mΩ
Input Filter Capacitors C_I	Evox-Rifa PH840M, 6.8 µF @275/280VAC $ESR_{28kHz,\ 60°C}$ = 23mΩ
Input Filter Inductor L_I	Magnetics High Flux 58439-A2, 240µH N = 51 turns, 14AWG

Fig. 7. Power module IXYS VUI 31-12N1, integrating all semiconductors of one bridge leg (IGBT and four diodes) of the three-phase three-switch buck-type PWM rectifier.

switching losses have to be evaluated experimentally since they depend highly on the specific diode-switch combination, the utilized gate resistor and the hardware setup (length and shape of the commutation paths). With the knowledge of the dependency that the total losses of the active and passive components have on the operating parameters (input voltage, output power, switching frequency) the efficiency of the system can easily be predicted. Furthermore, the junction temperatures of the semiconductors can be checked in order to verify the design from a thermal point of view.

A. Conduction Losses

The forward characteristic of the semiconductors can be approximated, with good accuracy, by a forward voltage drop and a forward resistance, which are given in the datasheets of the components and are listed in Table II. With this, the conduction losses of the semiconductors can be derived by

$$P_{\mathrm{Cond,IGBT}} = U_{CE0} \cdot I_{S,\mathrm{avg}} + r_{CE} \cdot I^2_{S,\mathrm{rms}} \tag{41}$$

$$P_{\mathrm{Cond},D} = U_F \cdot I_{D,\mathrm{avg}} + r_D \cdot I^2_{D,\mathrm{rms}} \tag{42}$$

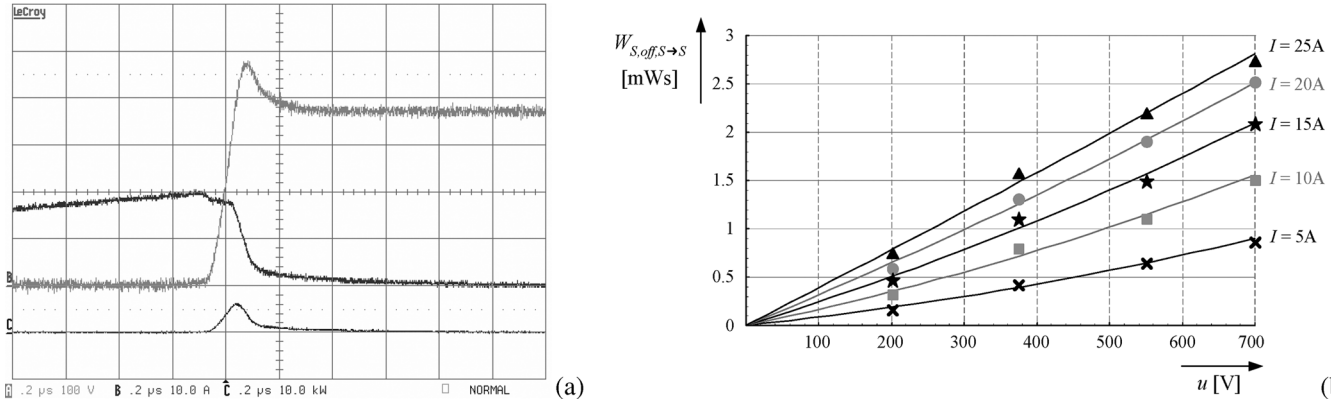

Fig. 8. (a) Commutation process of the switch S_T for a turn-off condition for a switched voltage of $U_{N,ST} = 375$ V and a switched current of $I = 20$ A (scales: 100 V/div, 10 A/div, 10 kW/div, 200 ns/div) and (b) dependency of the turn-off losses on the switched voltage and current.

utilizing the analytical expressions for the average and rms current stresses given in Fig. 6).

B. Switching Losses

Basically, there are four switching instants during every pulse period, where switching losses occur (cf. Fig. 3).

- Turn-off of one switch and commutation of the current to another phase (e.g., from (101) to (110) in Fig. 3), where turn-off losses $P_{S,\text{off},S\to S}$ in the switch occur. The current, voltage and power loss waveforms for this turn-off are depicted in Fig. 8(a) exemplarily for a switched voltage of $U_{N,ST} = 375$ V and a switched current of $I = 20$ A.
- Turn-off of a switch and commutation of the current to the freewheeling diode (e.g., from (110) to (010) in Fig. 3), where turn-off losses $P_{S,\text{off},S\to D}$ in the switch occur.
- Turn-on of a switch after freewheeling state and commutation of the current from the freewheeling diode to a switch (e.g., from (010) to (110) in Fig. 3), where turn-on losses $P_{S,\text{on},S\to D}$ in the switch, reverse recovery losses $P_{DF,\text{rev},D\to S}$ in the freewheeling diode and forward recovery losses $P_{D,\text{fwd},D\to S}$ in four bridge leg diodes occur.
- Turn-on of a switch and commutation of the current between two phases (e.g., from (110) to (101) in Fig. 3), where turn-on losses $P_{S,\text{on},S\to S}$ in the switch, reverse recovery losses $P_{D,\text{rev},S\to S}$ in one bridge leg diode and noteworthy forward recovery losses $P_{D,\text{fwd},S\to S}$ in two bridge leg diodes occur.[3]

With a linear dependency of the loss energy on current and voltage

$$w = k_1 \cdot u \cdot i \tag{43}$$

a first estimation of the switching losses based on manufacturer's data prior to a prototype build-up can be done. Usually the loss energies are given for one operating point in the datasheets whereby the parameter k_1 can be easily identified. However, these losses are always given for a specific diode-switch combination that can differ from the utilized combination. In the case at hand, the freewheeling behavior of the freewheeling diode together with the module IGBT is unknown. Additionally, the switching losses are strongly dependent on the specific selected gate resistor and also the PCB layout.

Therefore, if a prototype is available for measurements, for an exact calculation it is preferred to measure the loss energies for all switching actions and consider a function of higher complexity including linear and square terms of voltage and current and their products

$$w = k_1{\cdot}u{\cdot}i + k_2{\cdot}u{\cdot}i^2 + k_3{\cdot}u^2 + k_4{\cdot}u^2{\cdot}i + k_5{\cdot}u^2{\cdot}i^2 + k_6{\cdot}i + k_7{\cdot}i^2. \tag{44}$$

In this function also terms without direct physical meaning are taken into account in order to increase the accuracy of the loss calculations. This approximation is shown exemplarily in Fig. 8(b) for the turn-off losses of a switch along with the measured loss energy values. Due to the phase symmetry it is sufficient to integrate the loss energy of each loss term over a $\pi/6$ interval

$$P = f_S \cdot \frac{6}{\pi} \int_0^{\pi/6} w(u,i)\,d\varphi \tag{45}$$

e.g., the turn-off losses of a switch for a commutation of the current to another switch can be calculated with

$$P_{S,\text{off},S\to S} = f_S \cdot \frac{6}{\pi} \int_0^{\pi/6} w_{S,\text{off},S\to S}\left\{u_{RS}(\varphi), I\right\} d\varphi. \tag{46}$$

The other loss terms are determined in a similar manner. The total losses of the IGBTs and diodes are therefore given by

$$\begin{aligned} P_{Sw,\text{IGBTs}} &= P_{S,\text{off},S\to S} + P_{S,\text{off},S\to D} \\ &\quad + P_{S,\text{on},D\to S} + P_{S,\text{on},S\to S} \end{aligned} \tag{47}$$

$$\begin{aligned} P_{Sw,Di} &= P_{Di,\text{rev},S\to S} + 2\cdot P_{Di,\text{fwd},S\to S} \\ &\quad + 4\cdot P_{Di,\text{fwd},D\to S} \end{aligned} \tag{48}$$

$$P_{Sw,DF} = P_{DF,\text{rev},D\to S}. \tag{49}$$

C. Losses of the Passive Components

In addition to the losses of the active components the losses of the passive components have to be considered. Generally, the

[3]Only forward recovery losses caused by the dc inductor current plus the reverse recovery current are considered.

core losses of inductors are given for ferrite materials by the Steinmetz equation [22]

$$P_{L,\mathrm{core}} = C_m \cdot f_S^{\alpha} \cdot B_m^{\beta} \tag{50}$$

where B_m is the peak magnetic flux density and C_m, α and β are empirical parameters obtained from experimental measurement under sinusoidal excitation. For the selected core material [23] the core losses of the dc inductors L_{0+} and L_{0-} are given for dc application by

$$P_{L,\mathrm{core}}\,[\mathrm{W/kg}] = 6.5 \cdot (f_S\,[\mathrm{kHz}])^{1.51} \cdot \left(\frac{B_{\mathrm{sat}}[T]}{2}\right)^{1.74} \tag{51}$$

and the copper losses

$$P_{L,\mathrm{copper}} = \frac{\rho_{Cu,Ta} \cdot l_C}{A_C} \cdot I^2 \tag{52}$$

where the temperature dependency of copper has to be considered

$$\rho_{Cu,Ta} = \rho_{Cu,25^\circ\mathrm{C}} \cdot \left(1 + 3.93 \cdot 10^{-3} \cdot (T_a[^\circ\mathrm{C}] - 25)\right) \tag{53}$$

with

$$\rho_{Cu,25^\circ\mathrm{C}} = 16.8\ \mathrm{n\Omega m}. \tag{54}$$

The losses of the output capacitor C_0 can be calculated via

$$P_{L,C0} = ESR_{C0} \cdot I_{C0,\mathrm{rms}}^2 \tag{55}$$

and for the losses of the filter capacitors C_1 one receives

$$P_{L,C1} = 3 \cdot ESR_{C1} \cdot I_{C1,\mathrm{rms}}^2. \tag{56}$$

Furthermore, the losses of the input filter inductors L_1, which are included in the experimental setup as a part of the EMC input filter [16], are considered

$$P_{L,L1} = 3 \cdot ESR_{L1} \cdot I_{N,\mathrm{rms}}^2 \tag{57}$$

with

$$ESR_{L1} = 45\ \mathrm{m\Omega}. \tag{58}$$

Additionally, losses caused by resistances of printed circuit board conductors and of fuses are taken into account

$$P_{L,\mathrm{Cond}} = \rho_{C,Ta} \cdot \frac{l_{\mathrm{Cond}}}{A_{\mathrm{Cond}}} \cdot I^2 \quad \text{with } l_{\mathrm{Cond}} = 1\ \mathrm{m} \quad \text{and } A_{\mathrm{Cond}} = 5\ \mathrm{mm} \cdot 70\ \mu\mathrm{m} \tag{59}$$

$$P_{L,\mathrm{fuse}} = 3 \cdot R_{\mathrm{fuse}} \cdot I_N^2 \quad \text{with } R_{\mathrm{fuse}} = 10\ \mathrm{m\Omega}. \tag{60}$$

D. Breakdown of Total Losses

With the analytical equations for the losses of the active and passive components (41)–(60) the total losses of the converter can be evaluated easily, depending on the operating parameters. The breakdown of the total losses for $U_{N,l-l,\mathrm{rms}} = 400$ V, $U_0 = 400$ V and $f_S = 28$ kHz are depicted in Fig. 9 in dependency of the output power. Additionally, $P_{\mathrm{aux}} = 25$ W for the auxiliary power supply have been considered in order to have a complete composition of all relevant loss portions.

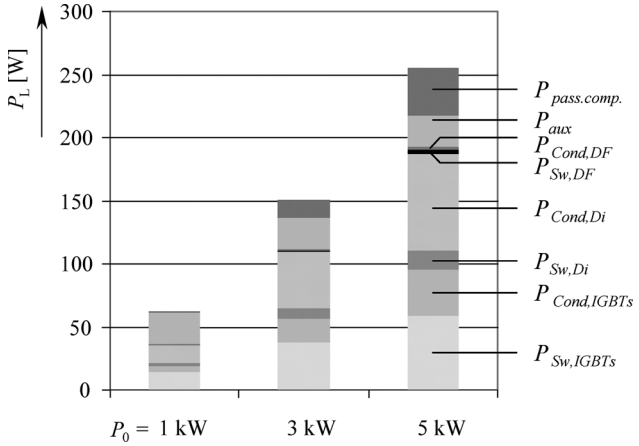

Fig. 9. Breakdown of the total losses for different output power levels, $U_{\mathrm{N,l-l,rms}} = 400$ V and $f_S = 28$ kHz.

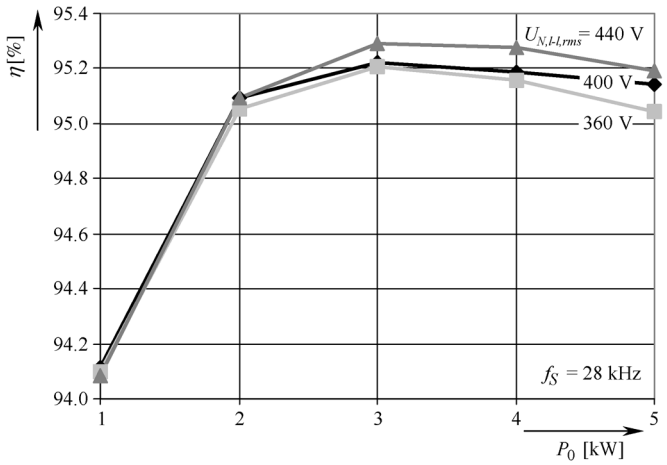

Fig. 10. Calculated total system efficiency for different output power levels and input voltages ($f_S = 28$ kHz).

E. Overall System Efficiency

In Fig. 10 the total efficiency is depicted, with dependency on the input voltage and the output power. The highest efficiency is given at $U_{N,l-l,\mathrm{rms}} = 440$ V due to a good balance between switching and conduction losses. For $P_0 = 5$ kW the efficiency is always higher than $\eta = 95\%$, while for low output power ($P_0 = 1$ kW) the efficiency is lowered to $\eta = 94.1\%$.

F. Junction Temperatures

Finally, the junction temperatures are checked in order to complete the design regarding the thermal aspects. Considering an ambient temperature of

$$T_a = 65^\circ\mathrm{C} \tag{61}$$

which corresponds to a value being commonly used in industry applications for the dimensioning of a power supply and utilizing a heat sink with a thermal resistance of

$$R_{th,hs} = 0.15\ \mathrm{K/W} \tag{62}$$

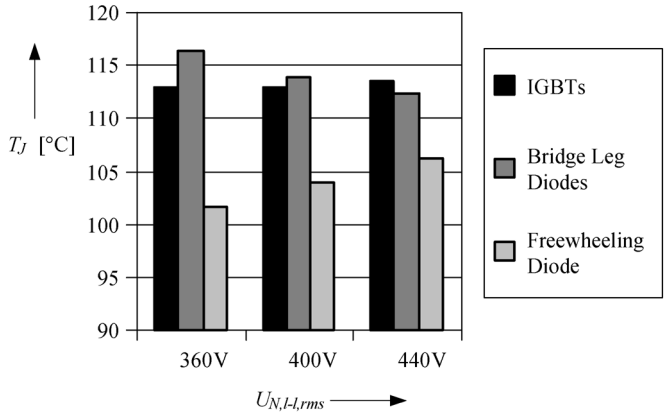

Fig. 11. Junction temperatures of the power semiconductors for different input voltages ($P_0 = 5$ kW, $f_S = 28$ kHz).

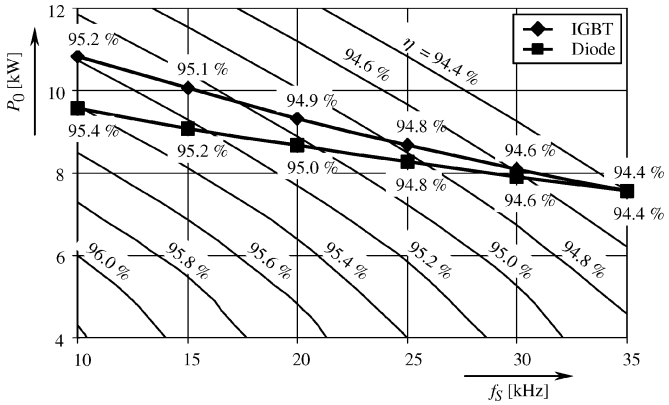

Fig. 12. Maximum allowable output power of the rectifier system shown in Fig. 1 according to the maximum junction temperatures of the module IGBTs and module diodes in dependency on the switching frequency. Furthermore shown: lines of constant efficiency under consideration of the total power losses.

the temperature of the heat sink can be calculated through

$$T_{hs} = T_a + R_{th,hs} \cdot (3 \cdot (P_{\mathrm{Cond,IGBT}} + P_{Sw,\mathrm{IGBT}}) + 12 \cdot (P_{\mathrm{Cond},Di} + P_{Sw,Di}) + P_{\mathrm{Cond},DF} + P_{Sw,DF}) . \quad (63)$$

With

$$T_{J,i} = T_{hs} + (R_{th,JC,i} + R_{th,CS,i}) \cdot (P_{\mathrm{Cond},i} + P_{Sw,i}) \quad (64)$$

the junction temperature of the semiconductor i can be derived, where the $R_{th,JC,i}$ indicates the thermal resistance of the component between junction and case and $R_{th,CS,i}$ between case and heat sink. If the following thermal resistances of the power semiconductors are considered

$$R_{th,JC,\mathrm{IGBT}} + R_{th,CS,\mathrm{IGBT}} = 0.3\,\mathrm{K/W} + 0.3\,\mathrm{K/W} \quad (65)$$

$$R_{th,JC,Di} + R_{th,CS,Di} = 1.3\,\mathrm{K/W} + 1.3\,\mathrm{K/W} \quad (66)$$

$$R_{th,JC,DF} + R_{th,CS,DF} = 1.2\,\mathrm{K/W} + 0.5\,\mathrm{K/W} \quad (67)$$

the junction temperatures illustrated in Fig. 11 are resulting. Obviously, the junction temperatures are all well below the maximum allowable junction temperature $T_{J,\max} = 150$ °C, therefore the thermal design is proven.

VII. Discussion

In the previous sections the active and passive components of the three-phase buck-type rectifier have been dimensioned according to given specifications and the design has been analyzed as regards the loss distribution and system efficiency. However, as the thermal analysis of the power module (cf. Fig. 11) shows, the system design would allow a higher output power from a thermal point of view, especially, if the switching frequency is reduced. Therefore, in this section it is investigated how the maximum output power changes as a function of the switching frequency for the selected components.

For fixed output voltage U_0 the maximum rectifier output power $P_{0,\max}$ is defined by the maximum allowable value of the inductor current I, and the switching and conduction losses, (41)–(60), in connection with the allowable thermal stress on the power semiconductors.

For the calculation of $P_{0,\max}$ we have to consider the maximum allowable value of the junction temperature $T_{J,\max}$ for each power semiconductor device of the module (transistor S_i and diodes D_i) and for the freewheeling diode D_F. With this, the maximum allowable semiconductor loss of one device i is given by

$$P_{L,i,\max} = \frac{T_{J,i,\max} - T_{hs}}{R_{th,i,JC} + R_{th,i,CS}} \quad (68)$$

where the heat sink temperature T_{hs} is given by (63) for a given ambient temperature T_a.

The semiconductor losses include terms showing a dependency on the inductor current I and on I^2, on the switching frequency f_S, on the input voltage $\hat{U}_N$ and on $\hat{U}_N^2$ as well as the output voltage U_0 and constant terms, therefore one can calculate the allowable inductor current for the respective considered device in dependency on the switching frequency for a fixed input voltage by solving the quadratic equation in I. *Remark*: Since the calculation of the heat sink temperature through (63) includes on the unknown current I this leads to an iterative computation procedure.

The calculation of the maximum allowable output power $P_{0,\max}$ which is given for constant output voltage U_0 directly by the maximum allowable inductor current I is carried out here for the nominal operating point ($U_{N,l-l,\mathrm{rms}} = 400$ V, $U_0 = 400$ V), for an ambient temperature of $T_a = 65$ °C, a maximum admissible junction temperature of $T_{J,\max} = 150$ °C for all power semiconductors, and the thermal resistances given in Section VI-F.

In Fig. 12 the results of the maximum allowable output power levels $P_{0,\max}$ according to the maximum junction temperatures of the module IGBTs and module diodes are shown. The obtainable output power of the rectifier system is limited within the considered switching frequency range ($f_S < 35$ kHz) by the thermal stress of the power module diode. The maximum output power level for the freewheeling diode is not shown since it is approximately 2 kW higher than the level for the IGBT and is therefore not relevant for the limitation of the output power. Hence, from a thermal point of view, D_F is slightly overdimensioned. However, it is preferable to choose a large freewheeling diode, since it is a single element in the system and it should be prevented that it is the limiting factor for the admissible power of the system.

Furthermore, in Fig. 12 lines of constant efficiency are shown which are calculated analytically considering all relevant loss portions $P_{L,\mathrm{tot}}$ discussed in Section VI

$$\begin{aligned} P_{L,\mathrm{tot}} = {} & 3 \cdot (P_{\mathrm{Cond,IGBT}} + P_{Sw,\mathrm{IGBT}}) + 12 \\ & \cdot (P_{\mathrm{Cond},Di} + P_{Sw,Di}) + P_{\mathrm{Cond},DF} + P_{Sw,DF} \\ & + P_{L,\mathrm{core}} + P_{L,\mathrm{copper}} + P_{L,C0} \\ & + P_{L,C1} + P_{L,L1} + P_{L,\mathrm{Cond}} + P_{L,\mathrm{fuse}} \end{aligned} \tag{69}$$

i.e., semiconductor losses (41)–(49), losses of the dc inductors (51), (52), losses of the output capacitor (55), losses of the input filter capacitors (56) and inductors (57), and resistive losses of the PCB and fuses (59), (60). The total system efficiency is then given by

$$\eta = \frac{I \cdot U_0}{I \cdot U_0 + P_{L,\mathrm{tot}}}. \tag{70}$$

Equations (69) and (70) again contain terms showing a dependency on the inductor current I and on I^2, on the switching frequency f_S, on the input voltage $\hat{U}_N$ and on $\hat{U}_N^2$, as well as on the output voltage U_0. For a certain constant value of the efficiency η (and constant input and output voltages) the quadratic equation in I (which again determines the output power) can be solved in dependency on the switching frequency. With this, the lines of constant efficiency in Fig. 12 are derived.

It has to be stated that the maximum achievable output power levels and all efficiency curves in Fig. 12 have been calculated with the passive components selected in Section V. Strictly speaking, for complying with the ripple requirements and/or EMC standards the passive components would have to be redesigned for different switching frequencies. However, for the calculation of the total efficiency (and also the power density) this is not necessary due to the following two reasons.

i) As depicted in Fig. 9 the losses of the passive components are only contributing about 14.5% to the total losses (for $P_0 = 5$ kW) and therefore the efficiency is mainly determined by the losses of the semiconductors.
ii) For decreasing switching frequencies on the one hand the input filter components L_1 and C_1 can be dimensioned smaller for complying with the EMC standards, as explained in Section IV. On the other hand, the dc link inductor L_0 has to be designed larger in order to maintain the same ripple values. Hence, the total size and the losses of the passive components are approximately constant for varying switching frequency.

Therefore, it is not necessary to redesign the filter components for the calculation of the efficiency in the considered switching frequency range.

VIII. Experimental Verification

Following the design steps detailed in the previous sections a hardware prototype that is shown in Fig. 13 has been built. The system is designed as a stand-alone system including auxiliary power supply, a DSP control board and an EMC input filter. In order to verify the loss and efficiency calculations of Section VI the total system efficiency has been measured and compared with the calculated values. Fig. 14 shows the good accordance between calculation and measurement for all power levels, with a deviation of $\Delta\eta = 0.1\% \ldots 0.3\%$. For the nominal operating point ($P_0 = 5$ kW, $U_{N,l-l,\mathrm{rms}} = 400$ V, $U_0 = 400$ V) the calculated total efficiency is 95.1%, where the measured value is 95.0%. With this, both the good performance of the three-phase three-switch buck rectifier and the correctness of the proposed design procedure have been proven.

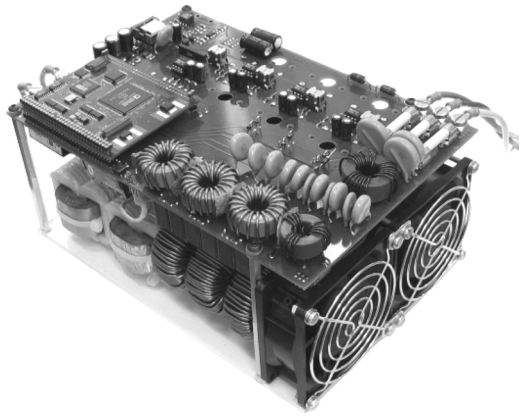

Fig. 13. Prototype of the three-phase buck-type PWM rectifier including DSP control board, auxiliary power supply and EMC input filter. Overall dimensions: 240 mm ×160 mm× 129 mm.

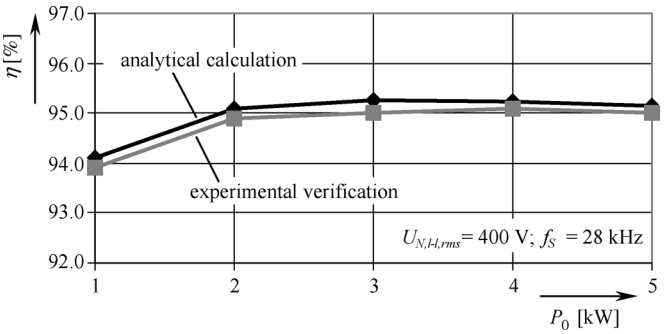

Fig. 14. Comparison of the measured and the calculated efficiency by (70) for different output power levels ($f_S = 28$ kHz, $U_{N,l-l,\mathrm{rms}} = 400$ V).

IX. Conclusion

This paper presents a complete design procedure of a three-phase three-switch buck rectifier based on analytical expressions of the current stresses of the active and passive power semiconductors. The accuracy of the given calculations is proven by digital simulations to be within a 6% range. Exemplarily, a system is dimensioned for specifications typically given for power supply modules in telecom applications. Based on the analytical expressions and on switching loss measurements the power loss distribution is ascertained and the total system efficiency is calculated. Furthermore, it is shown that for an existing design the maximum allowable output power can be derived with the analytical expressions under consideration of the maximum junction temperatures of the power semiconductors.

For the specifications of 5-kW output power, mains voltage of 400 Vrms and output voltage of 400 V a total efficiency of 95.1% is calculated, which is in good agreement with the measured efficiency of 95.0% of a hardware prototype that has been built according to the presented design procedure.

The presented analytical calculations can be used in the future as a basis for optimization routines, where, e.g., the total volume of the rectifier is minimized (including heat sink volume, EMC

input filter, and output filter) for a specific operating point. Together with a database including parameters of active and passive components it would be sufficient to specify the system specifications such as input and output voltage, output power, and switching frequency. The design could then be performed automatically by selecting appropriate components and calculating losses, the heatsink temperatures, and the total system efficiency. This constitutes an important step towards a virtual prototyping of the system.

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