Improving Mains Current Quality for Three-Phase Three-Switch Buck-Type PWM Rectifiers

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***Abstract*—Modulation schemes for three-phase three-switch buck-type pulsewidth modulation rectifiers where the switching state of one bridge leg is clamped within a $\pi/3$-wide interval of the mains period guarantee minimum switching losses as well as minimum input filter capacitor voltage ripple and minimum dc current ripple. However, as shown in this paper by a detailed analysis of the time behavior of the input filter capacitor voltages within a pulse period such modulation schemes are characterized by the occurrence of sliding intersections of the filter capacitor voltages which causes input current distortion. An advanced modulation scheme is proposed which prevents the input current distortion and allows it to maintain the optimum performance of conventional modulation schemes. The theoretical considerations are finally verified by measurements on a 5-kW hardware prototype.**

***Index Terms*—Pulsewidth modulation (PWM), rectifier.**

I. Introduction

THREE-PHASE buck-type pulsewidth modulation (PWM) rectifier systems (also known as current source rectifiers) are employed as front-end converters in utility interfaced systems such as power supplies for telecommunication systems, process technology, and ac drive applications. In [1], a novel three-phase three-switch buck-type unity power factor PWM rectifier with integrated dc–dc boost converter output stage has been presented. This topology combines the advantage of a wide input voltage range and/or output voltage range with a sinusoidal shape of the mains currents lying in phase with the mains phase voltages. Furthermore, the system allows operation also in case of heavily unbalanced mains and/or in case of a mains phase loss.

The buck-type input stage of this topology (see Fig. 1) has already been investigated in [2]–[4], where different off-line programmed PWM patterns have been discussed, but no optimization of the PWM has been considered. An optimized modulation method concerning switching losses has been proposed in [1], which has been further improved in [5] regarding the RMS value of the ripple component of the dc link current, and in [6] regarding the minimization of the RMS value of the input filter capacitor voltage ripple, where there is always one bridge leg remaining in the on-state and/or clamped within a $\pi/3$-wide interval of the mains period. However, digital simulations (see Fig. 10 in [1]) and the experimental verification (see Figs. 10 and 11 in [1]) have shown that at the beginning and at the end $\varphi_N = n\cdot\pi/3\,(n = 1,2,3\ldots)$ of the clamping intervals (see Fig. 2) distortions of the mains current occur [7]. This effect, which is also present for six-switch buck-type topologies (e.g., Fig. 5 in [8]) has not been investigated in the literature so far.

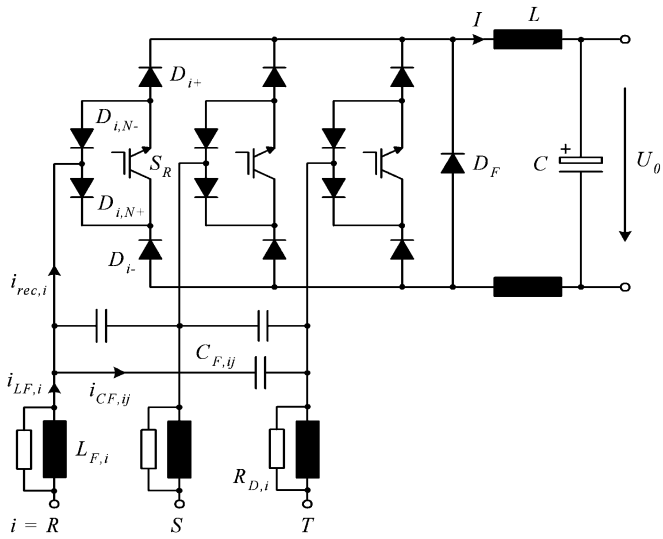

Fig. 1. Structure of the power circuit of a three-phase three-switch buck-type PWM rectifier.

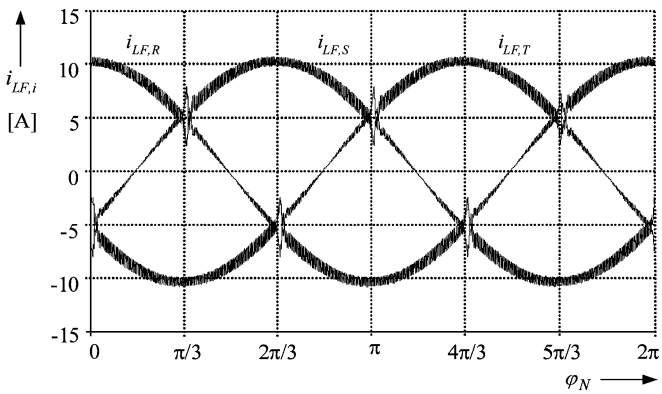

Fig. 2. Distortion of the mains phase currents of a three-phase three-switch buck-type PWM rectifier occurring for conventional PWM at the limits $\varphi_N = n\pi/3\,(n = 1,2,3\ldots)$ of bridge leg clamping intervals (see Fig. 3).

In this paper, an advanced modulation scheme is proposed which eliminates the input current oscillations but does maintain the optimum performance of clamping PWM schemes concerning the switching losses and the ripple of the input filter capacitor voltage and the dc link current. In Section II, the basic principle of operation of a three-phase three-switch buck-type PWM rectifier is reviewed briefly. The origin of the mains current distortion is clarified in Section III. An advanced modula-

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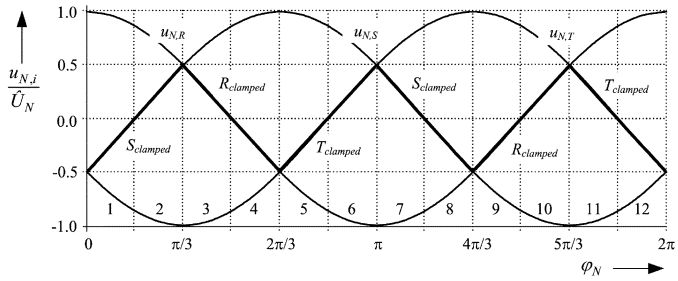

Fig. 3. Time behavior of the mains phase voltages $u_{N,i}, i = R, S, T$ and division of the mains period into 12 equal width ($\pi/6$) sectors . For the conventional modulation scheme the power transistor of the phase showing the lowest absolute instantaneous voltage value, e.g., S_S in $0 < \varphi_N < \pi/3$, is clamped in the on-state.

tion scheme preventing the mains current distortion at the beginning and/or end (boundaries) of the clamping intervals also in case of inaccurate detection of the clamping interval boundaries is proposed in Section IV and verified by measurements on a 5-kW hardware prototype in Section V.

II. Principle of Operation

In the following, a very brief description of the basic principle of operation of the three-phase three-switch buck-type PWM rectifier (see Fig. 1) shall be given. For a more detailed discussion we would like to refer to [1].

The dc current I being impressed by the dc-side inductor L and/or by an output current control is distributed to the three phases R, S, T, and/or to the freewheeling diode D_F depending on the switching state sequence which is determined by the mains voltage condition. For achieving a resistive fundamental mains behavior

$$i_{LF,i} \sim u_{N,i} \tag{1}$$

with

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cdot \cos(\omega_N t) \\ u_{N,S} &= \hat{U}_N \cdot \cos(\omega_N t - 2\pi/3) \\ u_{N,T} &= \hat{U}_N \cdot \cos(\omega_N t + 2\pi/3) \end{aligned} \tag{2}$$

(see Fig. 3) the relative on-times of the power transistors have to be set according to (32) in [1]. There, the modulation depth is characterized by a modulation index

$$M = \frac{\hat{I}_N}{I} = \frac{2}{3}\frac{U_0}{\hat{U}_N} \tag{3}$$

where $\hat{I}_N$ denotes the amplitude of the input currents $i_{LF,i}$.

The modulation methods for the three-phase three-switch buck rectifier that have been presented in literature are discussed briefly. For this purpose the mains period is divided into 12 equal $\pi/6$ wide sectors (see Fig. 3) according to the relationships of the instantaneous mains voltages. To be consistent with

TABLE I
Switching State Sequences Within a Switching Pulse Period for Different Modulation Methods. *Act1* and *Act2* Denote the Two Active Switching States (e.g., *Act1* is Realized by $j = (111)$ and *Act2* by $j = (011)$ in the Sector 2) and FW Denotes the Freewheeling State (e.g., FW is Realized by $j = (010)$ in the Sector 2); t_μ Denotes the Local Time Within the Pulse Period T_P

1	*Act1 – Act2 – FW*	*FW – Act2 – Act1*	
2	*Act2 – Act1 – FW*	*FW – Act1 – Act2*	
3	*Act1 – FW – Act2*	*Act2 – FW – Act1*	
4	*Act1 – Act2 – FW*	*Act1 – Act2 – FW*	
	$t_\mu = 0$	$t_\mu = T_P/2$	$t_\mu = T_P$

the explanations in Section III and Section IV the modulation methods are described exemplarily for the sector 2 ($u_{N,R} > u_{N,S} > 0 > u_{N,T}$ and/or $\pi/3 < \varphi_N < \pi/3$ with $\varphi_N = \omega_N t$).

In the literature, the modulation techniques for the three-phase three-switch buck rectifier have been analyzed only regarding switching losses [1], the dc current ripple [5], and the input filter capacitor voltage ripple [6]. The four basic switching state sequences that have been considered are depicted in Table I. All switching state sequences are characterized by two active switching states *Act1* and *Act2* (where the dc link current I is always switched to two input phases, i.e., rectifier input currents $i_{rec,i}, i = R, S, T$, occur) and one freewheeling state FW (where the current flow I is via the free-wheeling diode D_F and/or $i_{rec,i} = 0$ is valid) per pulse half period. *Act1* denotes the switching state that is causing the largest instantaneous input line-to-line voltage at the dc link (here $j = (111)$, where $j = (s_R\, s_S\, s_T)$ denotes the combination of phase switching functions $s_i, i = R, S, T$; $s_i = 1$ denotes the on-state and $s_i = 0$ denotes the off-state of the power transistor S_i) and *Act2* the switching state with the second largest instantaneous input line-to-line voltage at the dc link. The switching state with the lowest line-to-line voltage is not considered here since this would lower the achievable modulation and/or output voltage.

As can be seen in Table I, the switching states can be arranged symmetrically (1, 2, 3) or asymmetrically (4) with reference to the middle of the pulse period and the freewheeling state can be placed in the middle (3) or at the beginning/end of a pulse half period (1, 2, 4). Furthermore, the freewheeling state can be placed in the first half pulse period directly after the switching state *Act1* (2, 3), or after the switching state *Act2* (1, 4).

In [1], it was shown that only the switching state sequence 1 of Table I guarantees minimum switching losses, since here the sum of the switched voltages shows a minimum value. Furthermore, as a detailed analysis shows, the switching state sequence 1 is also superior to the other sequences 2, 3, and 4 regarding the rms values of the dc current ripple [5] and the input filter capacitor voltage ripple [6].

Therefore, the conventional modulation method that is ensuring minimum switching losses and minimum ripple values of the passive components is characterized by:

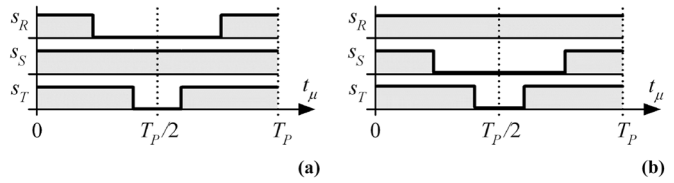

Fig. 4. Switching state sequences according to the conventional modulation scheme (see Table I, scheme 1) for one pulse period depicted for two different mains phase voltage conditions; (a) $u_{N,R} > u_{N,S} > 0 > u_{N,T}$ (sector 2), and (b) $u_{N,S} > u_{N,R} > 0 > u_{N,T}$(sector 3).

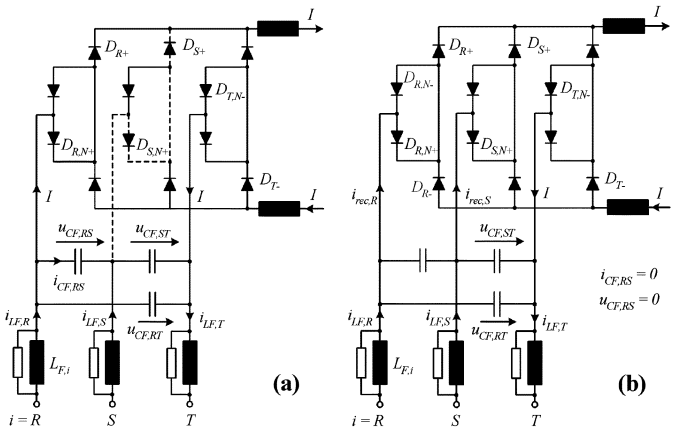

Fig. 5. System conduction states for (a) $u_{CF,RT} > u_{CF,ST}$ (sector 2, close to $\varphi_N = \pi/3$); in case the filter capacitor voltages would show no ripple, only phase S would carry current (indicated by a dashed line) for $s_S = 1$ in the pulse period following $\varphi_N = \pi/3$. Furthermore shown: conduction state (b) when a sliding intersection of the input capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ occurs (rectifier input currents are present simultaneously in the commutating phases R and S). Freewheeling diode D_F is not shown for the sake of clarity.

- two active switching states and one freewheeling state per pulse half period;
- a symmetric switching state sequence within each pulse period;
- the active switching state showing the larger line-to-line voltage located at the beginning/end and the freewheeling state located in the middle of the pulse period;
- clamping of the transistor of the phase leg showing the lowest absolute value of the corresponding mains phase voltage (see Fig. 3).

The corresponding switching state sequences are depicted for the sector 2 ($\pi/6 < \varphi_N < \pi/3$) in Fig. 4(a), and for the sector 3 ($\pi/3 < \varphi_N < \pi/2$) in Fig. 4(b).

As shown in Fig. 3, within the first two sectors ($0 < \varphi_N < \pi/3$) of a mains period the transistor S_S is remaining in the on-state. There, at the beginning of a pulse period all transistors are turned on, i.e., $j = (111)$ [see Fig. 4(a)]. Accordingly, the function of the bridge legs is equivalent to a three-phase diode bridge. If the voltage drops across the filter inductors are neglected, a current flow in phases R and T, $i_{rec,R} = -i_{rec,T} = I$ occurs for the mains voltage conditions $u_{N,R} > u_{N,S} > u_{N,T}$. When transistor S_R is turned off and/or $j = (011)$ is valid, the current I commutates from phase R to phase S and/or phases S and T are conducting current, $i_{rec,S} = -i_{rec,T} = I$. As always two active bridge legs are required for carrying the dc output current I, the system is forced into the freewheeling state for turning off transistor S_T and/or changing to switching state $j = (010)$.

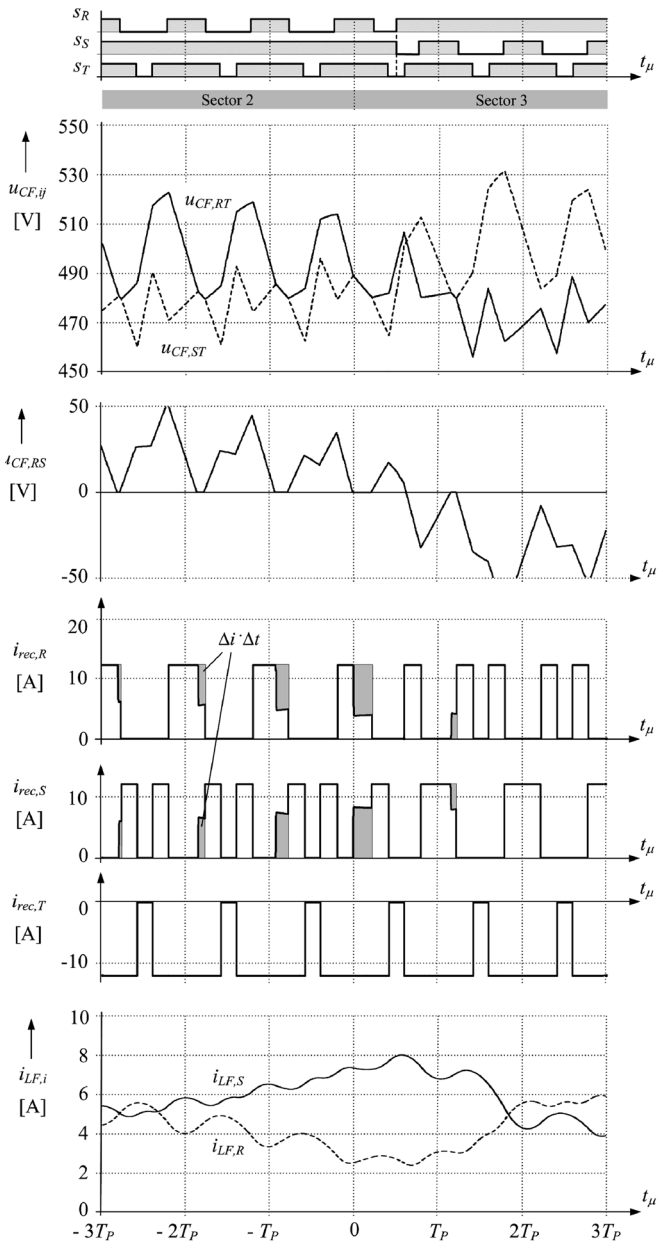

Fig. 6. Time behavior of the power transistor switching functions $s_i, i = R, S, T$, of the filter capacitor capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ occurring for the switching state $j = (111)$ can be clearly identified. voltages $u_{CF,RT}, u_{CF,ST}$, and $u_{CF,RS}$, of the rectifier input currents $i_{rec,R}, i_{rec,S}$, and $i_{rec,T}$, and of the mains filter inductor currents $i_{LF,R}$ and $i_{LF,S}$ for conventional modulation. The sliding intervals of the filter.

Since the relation of the instantaneous mains phase voltages $u_{N,R}$ and $u_{N,S}$ is reversed when entering from sector 2 into sector 3, the transistor S_R is clamped in the on-state (see Fig. 3) and S_S is switching and/or the switching patterns of phases R and S are exchanged [see Fig. 4(b)] as compared to the sector 2.

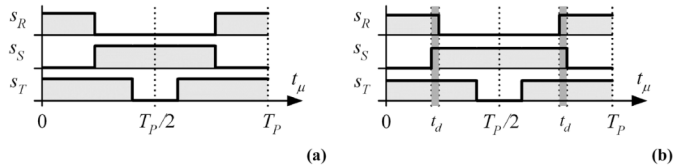

Fig. 7. Switching functions of the proposed advanced modulation scheme preventing sliding intersections of the filter capacitor voltages for the sector 2 [see Fig. 4(a)]; (a) ideal switching state sequence; (b) modified switching state sequence considering an overlapping time t_d when switching over from $j = (101)$ to $j = (011)$.

III. Sliding Intersections of the Input Filter Capacitor voltages

For all following considerations we will assume as specifications and/or operating parameters

$$P_0 = 5\,\text{kW} \quad \hat{U}_N = \sqrt{2} \cdot 230\,\text{V} \quad I = 12.5\,\text{A}$$
$$M = 0.82 \quad f_P = 20\,\text{kHz} \quad L_{N,i} = 150\,\mu\text{H}$$
$$L_{F,i} = 150\,\mu\text{H} \quad C_{F,ij} = 1.5\,\mu\text{F} \quad R_{D,i} = 3.9\,\Omega$$

where P_0 denominates the rated output power, $\hat{U}_N$ is the peak value of the mains phase voltage and f_P defines the system switching frequency; $R_{D,i}$ provides an optimum damping (see p. 398 in [9]) of the input filter formed by $L_{F,i}$ and $C_{F,ij}$ and the inner mains impedance $L_{N,i}$. (One has to note that passive damping is a strict requirement for an industrial application of the rectifier system as active damping schemes cannot prevent input filter oscillations caused, e.g., by mains voltage distortions at light load or in the turn-off state of the rectifier system.) Furthermore, we assume a constant value of the dc output current I in order to clearly show the effect of the sliding intersections of the input filter capacitor voltages on the rectifier input current formation.

As shown in Fig. 2 the input current distortion occurs at $\varphi_N = n \cdot \pi/3$, e.g., at the boundaries of a sector. For assuming ideal, ripple-free filter capacitor voltages lying in phase with the line-to-line mains voltages, i.e., for neglecting the phase shift due to the input filter inductors, the filter capacitor voltage $u_{CF,RS}$ would decrease to zero in $\varphi_N = \pi/3$. Accordingly, the two remaining capacitor line-to-line voltages $u_{CF,RT}$ and $u_{CF,ST}$ then would show equal values and the voltage relations of phases R and S would reverse when entering into sector 3. Considering the pulse pattern shown in Fig. 4 the rectifier input current $i_{rec,R} = I$ [see Fig. 5(a)] would therefore commutate immediately from phase R to phase S [dashed line in Fig. 5(a)].

However, due to the finite filter capacitance the filter capacitor voltage shows a ripple component. Therefore, in practice there is not a single crossover point, but in the vicinity of $\varphi_N = \pi/3$ in sections of the pulse periods $u_{CF,RT}$ and $u_{CF,ST}$ show equal values (such sections will be denoted as sliding intervals in the following). The resulting system behavior is shown in Fig. 6. For the considered sector transition the capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ assume equal values the first time when all switches are turned on, i.e., for $j = (111)$, already three pulse intervals before the actual sector limit $\varphi_N = \pi/3$. Accordingly, there the diodes D_{S+}, D_{SN+} of phase S start to conduct, while the diodes in phase R remain in conduction [see Fig. 5(b)]. Therefore, the capacitor voltage $u_{CF,RS}$ is clamped to zero and

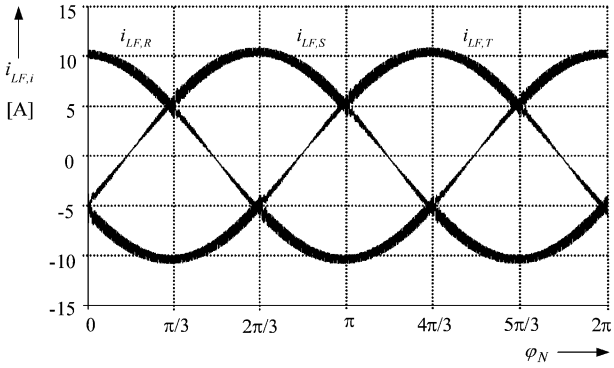

Fig. 8. Time behavior of the mains phase currents when employing the proposed modulation scheme.

$u_{CF,RT} = u_{CF,ST}$ is valid as long as $j = (111)$ is applied. Due to the equal rate of change of the filter capacitor voltages also the corresponding capacitor currents show equal values

$$i_{CF,RT} = C_F \cdot \frac{du_{CF,RT}}{dt} = i_{CF,ST} = C_F \cdot \frac{du_{CF,ST}}{dt}. \quad (4)$$

Therefore, rectifier input currents

$$i_{rec,R} = i_{LF,R} - i_{CF,RT}$$
$$i_{rec,S} = i_{LF,S} - i_{CF,ST}$$
$$i_{rec,R} + i_{rec,S} = I \quad (5)$$

are present simultaneously in the commutating phases R and S and/or as depicted in Fig. 6 segments of the current-time-areas $\Delta i\,\Delta t$ which should form the current in phase R occur in phase S. Hence, according to (4) and (5), $i_{LF,R}$ does continuously decrease and $i_{LF,S}$ does continuously increase (see Fig. 6) until the end of sector 2 is reached.

After changing from sector 2 into sector 3 the switching pattern shown in Fig. 4(b) is applied. There, for switching state $j = (101)$ where phases R and T are conducting the dc link current I the filter capacitor voltage $u_{CF,RT}$ is decreasing while $u_{CF,ST}$ is increasing due to $i_{LF,S}$. Accordingly, $u_{CF,RS}$ goes negative and for the subsequent switching state $j = (111)$ the current flow is via phase S until $u_{CF,RS}$ again reaches zero and a short sliding interval occurs. This however does not significantly change the time behavior of the rectifier input currents $i_{rec,i}$ and the distortion of mains currents $i_{LF,R}$ and $i_{LF,S}$ decays in form of a damped oscillation (due to the damping resistors $R_{D,i}$).

For the waveforms depicted in Fig. 6 the sector information has been derived from the inner mains voltages $u_{N,i}$ ($t_\mu = 0$ in Fig. 6 denotes the sector change according to the inner mains voltage conditions). For considering the phase displacement caused by the voltage drop across $L_{N,i}$ and $L_{F,i}$ the sector information is delayed by a half pulse period. Ideally, the sector should be determined based on the filter capacitor voltages which however contain a large switching frequency ripple component. Accordingly, in practice the filter capacitor voltage fundamentals have to be extracted by band-pass filtering. This prevents a phase shift at mains frequency which would result in erroneous sector detection.

In summary due to the capacitor voltage ripple and the continuous clamping of phase S in sector 2 a sliding intersection of the

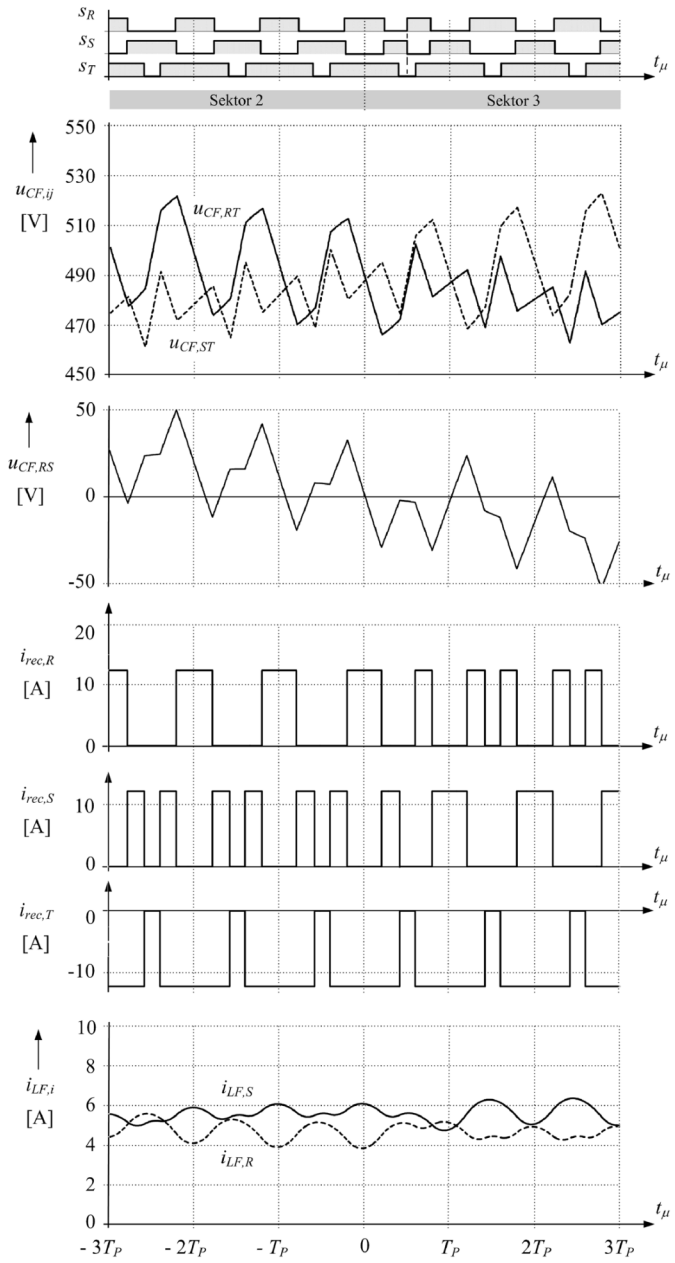

Fig. 9. Time behavior of the switching functions $s_i, i = R, S, T$, of the filter capacitor voltages $u_{CF,RT}, u_{CF,ST}$, and $u_{CF,RS}$, of the rectifier input currents $i_{rec,R}, i_{rec,S}$, and $i_{rec,T}$, and of the mains filter inductor currents $i_{LF,R}$ and $i_{LF,S}$ for the proposed modulation scheme ($t_u = 0$ denotes the sector change according to the inner mains voltage conditions) where the sliding intersections (see Fig. 6) of the filter capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ are prevented.

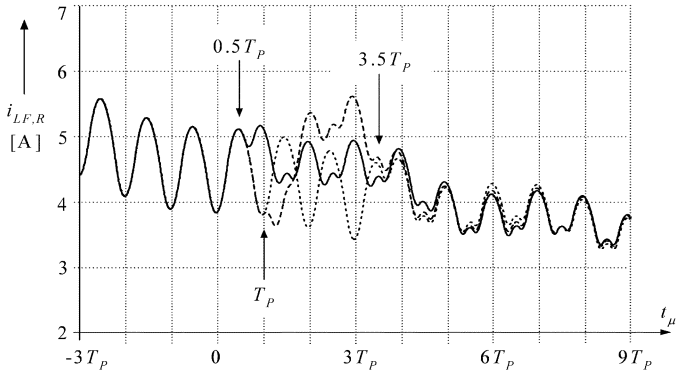

Fig. 10. Time behavior of the mains phase current $i_{LF,R}$ for considering the sector information with different delay times (the sector changes according to the relation of the inner mains voltages $u_{N,i}$ at $t_\mu = 0$); solid line: sector detection delay of $T_P/2$ and change of the switching pattern between two freewheeling states; dotted line: sector detection delay of $3(1/2)T_P$ and switching pattern change again during the freewheeling state; dashed line: sector detection delay of T_P and switching pattern change therefore between two active states.

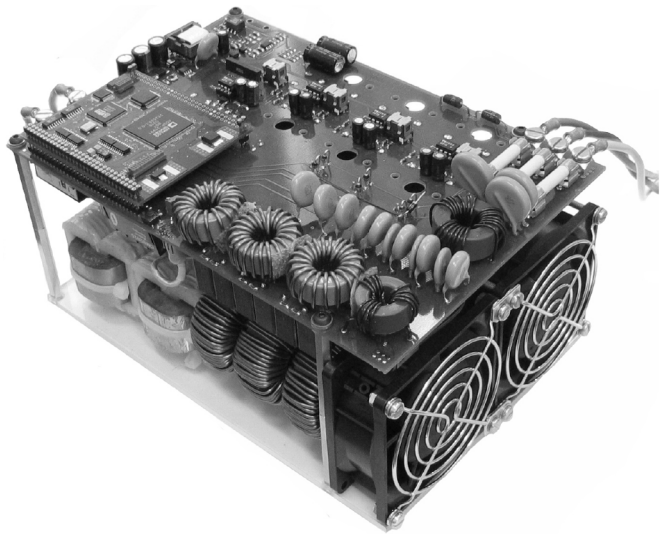

Fig. 11. Hardware prototype including DSP control board and EMC input filter (dimensions 240 mm × 160 mm × 120 mm).

filter capacitor voltages occurs which results in a distortion of the mains current. The current distortion could be reduced by increasing the capacitance of the filter capacitors or the switching frequency. However, this would result in a reduced power factor at low output power or in higher switching losses and therefore should not be considered further.

IV. Proposed Advanced Modulation Scheme

An advanced switching state sequence preventing sliding intersection of the filter capacitor voltages is depicted in Fig. 7(a) for assuming $\pi/6 < \varphi_N < \pi/3$ (sector 2, all following considerations will be limited to this case). There are no intervals where all transistors are turned on, accordingly, always only two bridge legs are carrying current (with the exception of the free-wheeling state) and no distortion of the mains currents $i_{LF,i}$ occurs.

In order maintain the minimum switching losses of the rectifier given for the conventional modulation, phase S has to be available for current conduction when phase R is turned off. This is ensured by introducing an overlapping time t_d of the turn-on states of both phases, i.e., by turning S_S on before turning S_R off. The overlapping time t_d is selected with respect to gate drive and signal electronics delay times and kept to minimum in order to avoid the occurrence of sliding intervals. If t_d would not be considered the differences between the gate drive time delays would cause short freewheeling states between the active switching states, which would increase the switching losses. As (for neglecting the switching frequency ripple of the

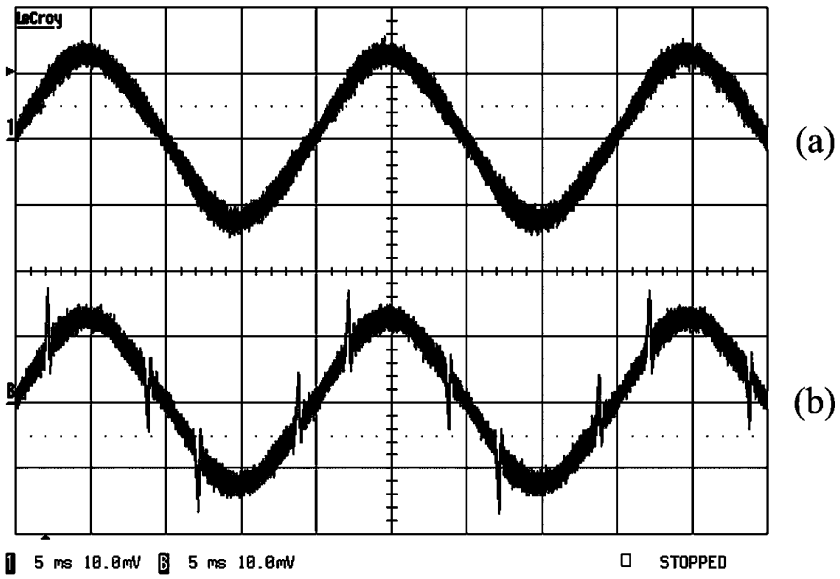

Fig. 12. Waveforms of the mains phase current $i_{LF,R}$ for the (a) advanced modulation method compared to the (b) conventional modulation. (current scale: 5 A/div, time scale: 5 ms/div).

filter capacitor voltages) $u_{CF,RT} > u_{CF,ST}$ is valid in sector 2, no turn-on losses of phase S occur, and the current I is commutated to phase S only at the turn-off of phase R.

Furthermore, the turn-off of phase S is delayed by t_d with reference to the turn-off of phase R, therefore, phase R also takes over the turn-off losses as given for the conventional pulse width modulation.

The system behavior resulting for employing the advanced modulation scheme is shown in Figs. 8 and 9. In contrast to the conventional modulation (see Fig. 6) no sliding intersection of the capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ occurs, accordingly the distribution of the dc link current I to the phases is in correspondence with the switching pattern and/or no distortion of the mains currents at sector boundaries occurs (see Fig. 8).

Now it shall be investigated to what extent a wrong, i.e., delayed detection of the end and/or beginning of a sector takes influence on the time behavior of the mains currents for application of the advanced PWM scheme. For considering the phase displacement caused by the voltage drop across the input filter inductor $L_{F,i}$ when entering into a new sector the sector information is updated and/or and considered for the PWM with a delay of half a pulse period, i.e., $T_P/2$. As depicted in Fig. 10 there is no significant difference of the mains current time behavior between updating the sector information with a delay of $T_P/2$ or, e.g., $3(1/2)T_p$ as long as the switching pattern is changed at the end of a freewheeling state and a free-wheeling state is also placed at the beginning of the subsequent pulse half period. If the switching pattern is changed at the end of a pulse sequence and/or pulse half period where an active switching state occurs and is continued in the subsequent sector with a switching state sequence showing an active state at the beginning a local distortion of the mains current occurs (see Fig. 10). As a more detailed analysis shows this oscillation is caused by an irregular distribution of the rectifier input current pulses at the sector boundary which results in a time behavior of the filter capacitor voltage ripple showing a non-zero local average value.

The improvement of the current quality is independent of asymmetries or sags in the supply voltage, since for the advanced modulation method the switching signals of the three phases are only different as compared to the conventional method, when the relationships between the instantaneous values of the filter capacitor voltages differ from the relationships between their fundamental components, which are considered for the sector detection. This is, as described above, only true in the vicinity of the sector boundaries due to the capacitor voltage ripple and will always avoid the input current oscillations, even if the sector information changes due to the new voltage conditions. However, ohmic behavior of the rectifier for asymmetric mains conditions cannot be guaranteed by any of the modulation schemes unless an appropriate control scheme is employed [10].

Furthermore, the improvement of the currents is not influenced by distortions of the mains voltages, unless the input filter is excited by the harmonics contained in the supply voltages. Due to this, the input filter has to be designed and damped (passively and/or actively) taking this into account [11].

V. Experimental Verification

The conventional (see Section II) and the proposed modulation method (see section IV) have been implemented on a DSP control board and tested on a 5-kW hardware prototype of the system (see Fig. 11). The measurement results in Fig. 12 clearly show the improvement of the current quality. The measured input current THD is improved from 16.6% for the conventional modulation to 6.9% for the advanced modulation method for open-loop operation at the nominal operating point ($U_{N,rms} = 230\,\mathrm{V}, U_0 = 400\,\mathrm{V}, P_0 = 5\,\mathrm{kW}$). If closed loop control is employed, the input current THD is improved to 0.9% at nominal load ($P_0 = 5$ kW) and 2.6% at $P_0 = 1$ kW, while for the conventional modulation the current THD cannot be improved significantly.

VI. Conclusion

It has been shown that sliding intersections of the input filter capacitor voltages and/or the resulting distortion of the mains current at sector boundaries which are characteristic for PWM schemes relying on the clamping of always one phase are eliminated by the proposed modulation scheme. There, the optimum properties of conventional modulation concerning switching losses and the switching frequency ripple of the filter capacitor voltages (excluding the immediate vicinity of sector limits) and the dc link current ripple are not impaired. Furthermore, the proposed PWM scheme is not sensitive to a delay of the consideration of changing sector information for the pulse pattern generation as far as the switching pattern is changed at the end of a free-wheeling state and a free-wheeling state is also placed at the beginning of the subsequent pulse half period. The proposed modulation concept is characterized by a slightly higher realization effort as compared to clamping PWM schemes as a continuous PWM has to be provided for all three phases. Experimental results on a DSP controlled 5-kW prototype of the PWM rectifier system confirm the theoretical considerations.

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