Differential Mode EMC Input Filter Design for a Three-Phase Buck-Type Unity Power Factor PWM Rectifier

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***Abstract.* − For a three-phase buck-type PWM rectifier input stage of a high-power telecommunications power supply module a differential mode EMC filter is designed which ensures compliance to EN 55022 Class B. The design is based on a harmonic analysis of the converter input current and a mathematical model of the measurement procedure including the LISN and the test receiver. Guidelines for a successful filter design are given and components for a 5kW prototype of the rectifier system are selected. There, the damping of filter resonances is optimized for given attenuation in order to facilitate a higher stability margin for the system control. Furthermore, the dependency of the filter input and output impedances and attenuation characteristic on the inner mains impedance is discussed. Finally, the theoretical considerations are verified by conducted emission measurements and the high quality sinusoidal shape of the resulting mains current is demonstrated.**

Keywords – EMC input filter, differential mode, PWM rectifier

I. Introduction

A three-phase three-switch current source (buck-type) PWM rectifier topology (cf. **Fig. 1**) features sinusoidal input current, direct start-up and overcurrent protection in case of output short circuits and therefore is of potential interest for the realization of the input stage of high-power telecommunications rectifier modules [1], [2]. There, the EMC input filter has to be designed for compliance to the European Standard EN 55022 Class B [3], where frequencies within the band 150 kHz – 30 MHz are considered for conducted emission (CE) measurements.

Considering a rectifier system with a rated output power of P_o = 5 kW operating at a rated mains voltage of $\hat{U}_{mains} = \sqrt{2}\cdot 230\text{V}$ (amplitude of the phase voltage) the input current spectrum depicted in **Fig. 2** is obtained. There, a modulation scheme resulting in minimum high frequency input current distortion [4] is employed and the switching frequency is selected as f_s = 28kHz, so that the first multiple of the switching frequency within the EMC measurement band is located at 168kHz. A zoom around f_s = 28kHz (cf. Fig. 2b) shows that harmonics are only present at frequencies $f_{harm} = m\cdot f_s \pm n\cdot f_{mains}$ with m = 1,2,3,… and n = 1,2,4,5,7,8,… and f_{mains} = 50Hz.

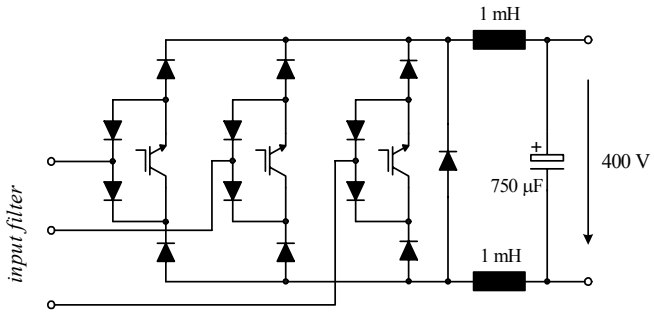

Fig. 1: Three-phase buck-type converter topology.

For other modulation methods the harmonics would vary in amplitude and phase and/or a different distribution of the harmonic power would occur. As Fig. 2(c) illustrates, for increasing m the amplitudes of the harmonics are decreasing and the width of the sidebands is increasing, i.e. the harmonic power is spread over a wider frequency range.

In this paper, based on Fig. 2 the design of a differential mode (DM) EMC filter of the rectifier system ensuring compliance to EN 55022 Class B is described following a procedure proposed in [5]. The filter components are selected in **section II** and are optimized in **section III**. Furthermore, the damping of filter resonances is discussed, considering the influence on the filter attenuation, and the filter input and output impedance and/or the stability of the system control. In **section IV** the theoretical considerations are verified by measurements of the DM conducted emissions and the resulting sinusoidal shape of the rectifier mains current is demonstrated.

II. Input Filter Design

Due to the phase symmetry of the converter and filter topology the design of the DM input filter can be restricted to a single phase equivalent circuit [5]. There, calculated filter parameters can be di-

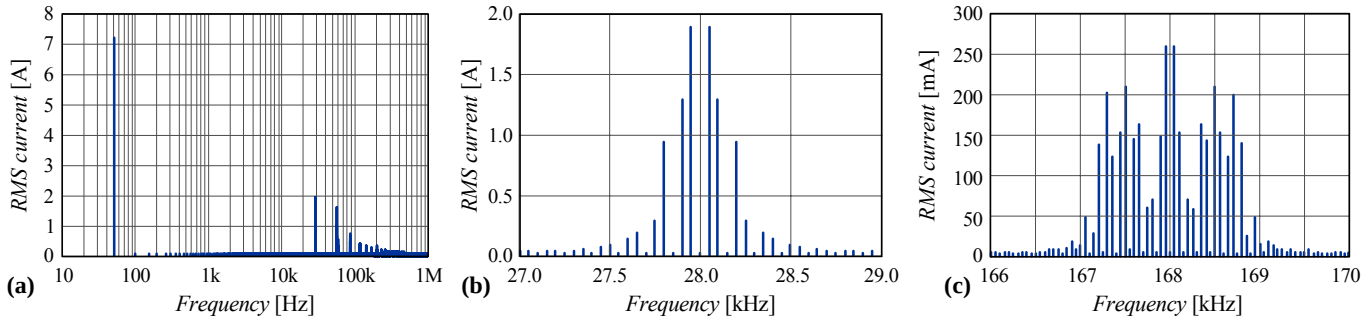

Fig. 2: **(a)** Frequency spectrum of the converter input current I_{dm}; **(b)** zoom around the switching frequency (at 28 kHz); **(c)** zoom around the first multiple of the switching frequency located in the frequency band 150kHz – 30MHz (at 168kHz).

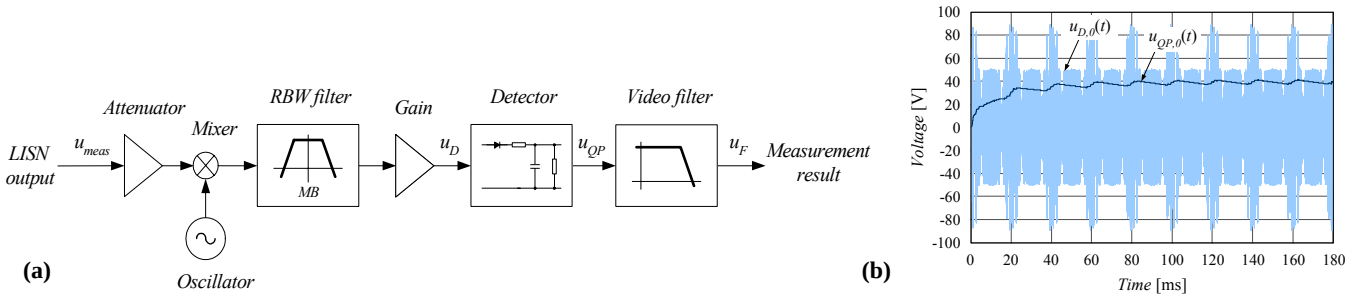

Fig.3: (a) Block diagram of measurement chain and QP detection. **(b)** Simulation of the quasi-peak detection in case no input filter would be present: waveform of the voltage $u_{D,0}$ at the input and voltage $u_{QP,0}$ at the output of the QP detector.

rectly applied if the capacitors of the actual filter are arranged in star connection; for a delta-connection of the filter capacitors the calculated capacitances have to be reduced by a factor of three.

For determining the filter attenuation the parasitics of the filter components, i.e. the series resistance and series inductance of the capacitors and the series resistance and parallel capacitance of inductors have to be considered (cf. section II.2). However, as practical experience shows such equivalent modeling of the components is only valid up to several MHz. At higher frequencies also the physical arrangement of the filter elements takes influence on the filter attenuation. For this reason a safety margin should be considered when defining the required filter attenuation; in the case at hand a margin of 6dB has been selected.

II.1 Calculation of the Required Filter Attenuation

According to the filter design procedure proposed in [5], first the LISN output voltage $u_{\text{meas},0}$[1] and/or the voltage occurring at the 50Ω input of the test receiver is calculated by filtering the input current spectrum according to the transfer function $U_{\text{meas},0}(\text{j}\omega)/I_{\text{dm}}(\text{j}\omega)$. This is done in a first step without any input filter in order to determine the required filter attenuation which is required for fulfilling the EMC regulations. The voltage at the LISN output is applied to the test receiver model (see **Fig. 3**(a), discussed in [5]) which comprises a gain/attenuator block, an oscillator[2], a resolution bandwidth (RBW) filter, a quasi peak (QP) detector and a low pass video filter. In the case at hand, the mid-band (MB) frequency of the RBW filter is set to the first integer multiple of the switching frequency harmonic within the frequency band 150kHz – 30MHz, i.e. to MB = 168kHz. As can be easily proven and will be verified by measurements in section IV, this is the worst case condition concerning the detected spectral power; accordingly it is sufficient to restrict the filter design to the consideration of MB = 168kHz. For shifting MB up in frequency, lower attenuation requirements do result. In Fig.3(b) the RBW filter output is compared to the subsequent QP detector output. According to CISPR 16 the time constant of the video low-pass filter is 160ms, therefore the measured voltage $u_{F,0}$ at the video filter output is close to the average value of $u_{QP,0}$; in the case at hand, $U_{F,0}$ = 39.3V and/or 151.9dBµV. By comparing $U_{F,0}$ to the EN 55022 Class B limit at $f = 168\,\text{kHz}$,

$$Limit_{CISPR,168kHz}\left[\text{dB}\mu\text{V}\right] \cong 65.1\text{dB}\,, \tag{1}$$

the required attenuation of the input filter including a margin of Margin[dB] = 6dB for accommodating common mode noise (assuming in a first approximation equal magnitudes of common and differential mode noise) is

$$\begin{aligned} Att_{req}\left[dB\right] = U_{F,0,168kHz}\left[\text{dB}\mu\text{V}\right] - Limit_{CISPR,168kHz}\left[\text{dB}\mu\text{V}\right] \\ + \text{Margin}\left[\text{dB}\right] \cong 92.8\text{dB}. \end{aligned} \tag{2}$$

II.2 Selection of the Filter Components

For achieving the required attenuation a two-stage filter is employed (cf. in **Fig. 4**), where *Section 1* is formed by C_1-L_1-L_{1d}, and *Section 2* is formed by C_2-Z_{LISN}. An explicit inductor could be placed in series on the mains side and/or in series to the LISN impedance resulting in a slightly higher attenuation. However, as shown in the following, the desired attenuation (2) can be achieved without additional inductance and in practice always an inner mains impedance is present forming the second filter stage in combination with C_2. Hence, aiming for a compact input filter and/or high system power density and minimum costs an explicit inductor is omitted.

The cut-off frequencies of the two filter sections are positioned such that the required attenuation (2) is achieved. For selecting the filter component values several additional design aims and nonlinear restrictions, like type and extent of damping, discrete available capacitance values, the influence of the parasitics of the filter components, low output impedance, low filter volume, low reactive power caused by the filter at no load and maximum current and voltage stresses, have to be considered.

Obviously, not all design aims can be fulfilled in the first design step. Therefore, a recursive design procedure is followed for determining the component values [5]. The filter components selected in the case at hand under consideration of the above mentioned design goals are detailed in Fig. 4 along with their parasitics which were determined by measurements of the real components. For the sake of clarity a refinement of the filter concerning the damping of the filter resonances and/or stability improvements is discussed separately in section III.

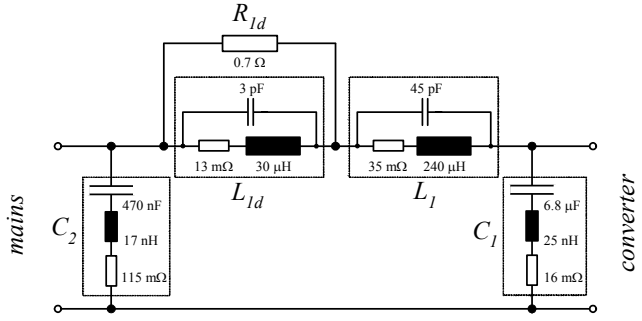

Fig. 4: Input filter performing the required attenuation plus margin; besides the main filter components also the parasitics of capacitors and inductors are shown.

[1] The index 0 indicates that no input filter is inserted.

[2] The mixer shifts the spectrum to be measured according to the oscillator frequency; this allows a scanning of the frequency range with constant mid-band frequency of the RBW filter by varying the oscillator frequency. For the modeling of the test receiver in the simulation the spectrum can be directly evaluated for different MB frequencies.

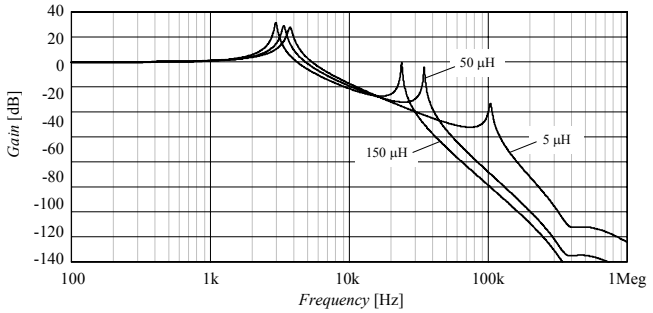

Fig. 5: Input filter attenuation characteristic according to Fig. 4 for three different mains impedances (inductances) L_{mains}.

The capacitor C_1 = 6.8µF placed directly at the rectifier input is selected such that the voltage ripple peak-to-peak value is limited to about 60 V which ensures a correct operation of the input voltage sector detection [4] providing the basis for the PWM of the converter. The inductor L_1 = 240µH is defining a cut-off frequency of *Filter Section 1* sufficiently below the switching frequency. The damping components L_{1d} = 30µH and R_{1d} = 0.7Ω are selected under consideration of low filter volume, low output impedance and optimum damping of the filter resonance at $\omega = 1/\sqrt{(L_1 C_1)}$ [6],[7],[8]. Finally, the capacitor C_2 is directly determined by the required attenuation remaining for *Filter Section 2* which is formed by C_2 in combination with the LISN impedance Z_{LISN}.

III. Filter Optimization

Employing the input filter designed in the previous section the converter would already comply to the EMC standard concerning differential mode noise emissions. However, for ensuring a satisfactory operation of the converter in combination with the input filter, e.g. also control-oriented aspects have to be considered as discussed in the following.

III.1 Additional Damping of the Filter Resonances

The influence of the inner mains impedance on the input filter attenuation characteristic is shown in **Fig. 5**. There, for limiting to the essentials the mains impedance is considered as purely inductive with an inductance in a range of L_{mains} = 5…150µH.

The filter characteristic exhibits two main resonances where the upper resonant frequency, i.e. the resonance of *Filter Section 2* shows a pronounced dependency on L_{mains}. Both resonances could be excited by harmonics contained in the feeding mains voltage which would result in voltage and current oscillations of large amplitudes. Also, the filter could be excited by the rectifier itself, e.g. if the upper filter resonance coincides with the switching frequency (which is true for L_{mains} = 150µH, cf. Fig. 5) or with multiples of the switching frequency. Therefore, a sufficient damping of the filter resonances without substantially influencing the high frequency attenuation has to be provided.

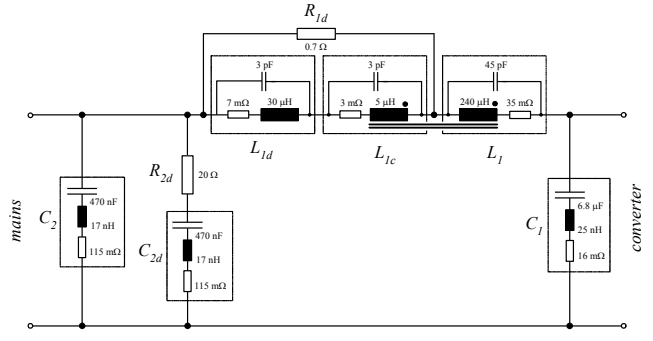

Fig. 6: Optimized filter topology including a damping of *Filter Section 1* (by coupled inductors, k = 0.981) and *Filter Section 2* (by a parallel RC path).

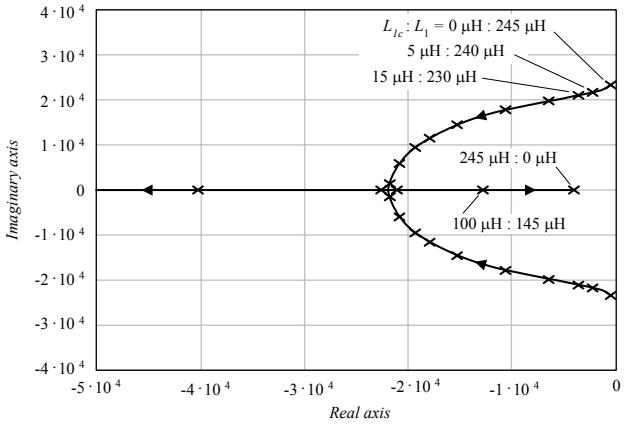

Fig. 7: Location of the dominant low-frequency input filter poles (being mainly determined by *Filter Section 1*, i.e. L_1-L_{1d}-L_{1c}-R_{1d} and C_1) in dependency of the inductance ratio of the coupled inductors L_{1c} and L_1.

A damping of *Filter Section 1* without increasing the filter volume or impairing the high frequency attenuation can be achieved by inserting an inductor L_{1c} coupled to L_1 in series to L_{1d} (cf. **Fig. 6**). With this, R_{1d} is effective also for L_1, dependent on the winding ratio and the magnetic coupling k of L_1 and L_{1c}. There, the filter damping could be increased by increasing the inductance ratio $n_L = L_{1c}/L_1$, however, at the same time the high frequency attenuation would be reduced. **Fig. 7** shows the location of the two dominant poles of the third-order system formed by *Filter Section 1* for different inductance ratios n_L (the third pole is located at high frequencies and therefore does not take significant influence on the filter behavior). For higher values of L_{1c} the distance of the poles to the imaginary axis and/or the filter damping does increase, while the attenuation at high frequencies is decreasing (cf. **Fig. 8**), resulting finally in a first-order (PT_1) system behavior for a wide frequency range (cf. Figs. 7 and 8 for n_L = 0µH : 245µH). There, n_L = 5µH : 240µH represents a good compromise where the resonance peak is lowered by 12dB and the reduction of the filter attenuation at 168 kHz is only 1.2dB compared to the original filter depicted in Fig.4. It can be shown that R_{1d} = 0.7Ω still provides optimum damping at maximum losses of $P_{R1d,max}$ = 0.11W, which facilitates a realization of R_{1d} by SMD resistors. Also the effort for realizing the coupled inductor L_{1c} = 5µH is very low, in the case at hand only 7 turns have to be added on the magnetic core of L_{mains}.

In case an equal reduction of the resonance peak and the same attenuation at 168 kHz would have to be achieved with the filter topology shown in Fig.4, L_1 = 210µH, L_{1d} = 130µH, and R_{1d} = 2.15 Ω would have to be selected. This clearly shows the advantage of a coupling of inductors (cf. Fig. 6) concerning the resulting filter volume.

The resonance of *Filter Section 2* can be damped by adding an *RC* series connection in parallel to C_2 (cf. Fig.6). There, the damping elements C_{2d} = 470nF, R_{2d} = 20Ω are selected such that sufficient damping is achieved for all inner mains inductances without

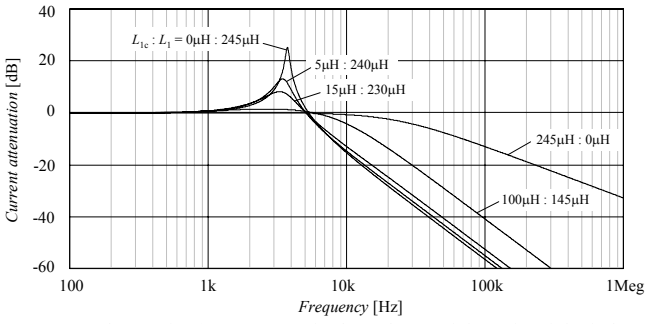

Fig. 8: Impedance of *Filter Section 1* in dependency of the ratio of the inductances of the coupled inductors L_{1c} and L_1.

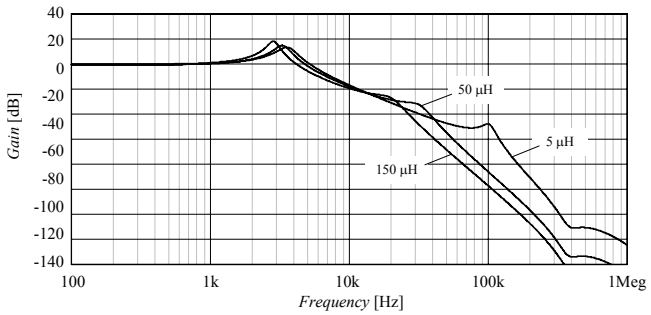

Fig. 9: Attenuation characteristic of the optimized input filter according to Fig. 6 for three different inner mains impedances (inductances) L_{mains}.

significantly affecting the high frequency filter attenuation (in the case at hand the attenuation at 168 kHz is even increased by 0.2 dB). Due to the low capacitance of $C_{2\text{d}}$ the filter volume is only slightly increased and the maximum losses of the damping resistor $R_{2\text{d}}$ amount to $P_{\text{R2d,max}} = 0.1\text{W}$, which again allows again a realization with SMD resistors.

The resulting filter attenuation characteristic is depicted in **Fig. 9**. The minimum attenuation of switching frequency input current harmonics occurs for $L_{\text{mains}} = 50\mu\text{H}$, where the upper filter resonance coincides with the switching frequency $f_{\text{s}} = 28$ kHz. There, the filter attenuation amounts to $|Att_{Filt}| = 26.3\text{dB}$, which means that the harmonics around f_{s} (cf. Fig. 2) are attenuated by a factor of 20, which still results in a very good mains current quality. This can be seen in **Fig. 10**, where a rectifier input current and the corresponding mains phase current are depicted.

In summary, the additional damping measures are reducing the attenuation of high frequency harmonics by 1dB and/or are resulting in a remaining margin of 5dB at 168 kHz.

III.2 Filter Input Impedance

The filter input impedance given for different inner mains inductances is depicted in **Fig. 11**. Compared to the impedance characteristic resulting for the first filter design (cf. Fig. 4, shown in Fig. 11 for $L_{\text{mains}} = 50\mu\text{H}$) the damping measures described in section III.1 are increasing the input impedance to $|Z_{i,Filt,min}| = 1\Omega$ at the first (series) resonant frequency.

Accordingly, for a sudden step $\Delta\hat{U}$ of the mains phase voltage amplitudes a well damped response of the filter output voltages and/or of the rectifier input phase voltages does occur (cf. **Fig. 12**). One has to note that the overshoot of the rectifier input voltage (70V in Fig.12) cannot be prevented by passive damping at reasonable losses. Also active damping measures would not allow a voltage limitation due to the limited control bandwidth (cf. Section III.3) and/or would not be applicable for no-load operation of the rectifier system.

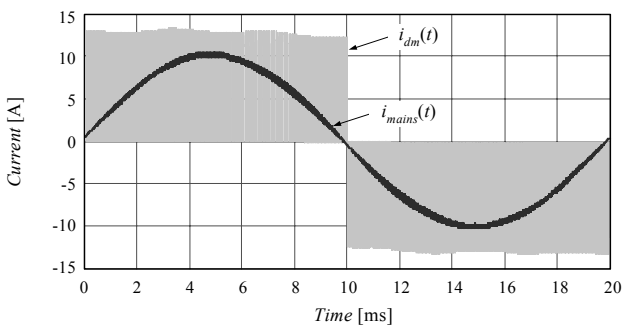

Fig. 10: Simulated time behavior of rectifier input current $i_{\text{dm}}(t)$ and resulting mains current $i_{\text{mains}}(t)$; assumed inner mains impedance: $L_{\text{mains}} = 50\mu\text{H}$.

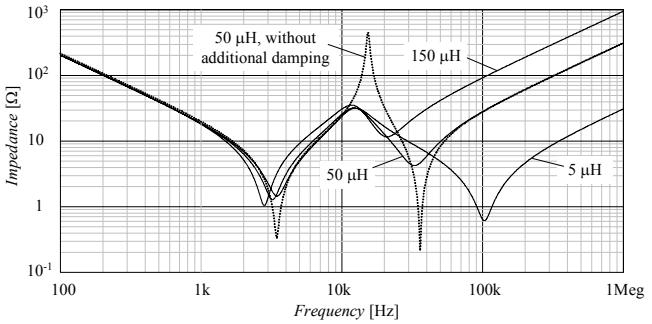

Fig. 11: Filter input impedance for open circuit filter output and three different mains impedances (inductances) L_{mains}.

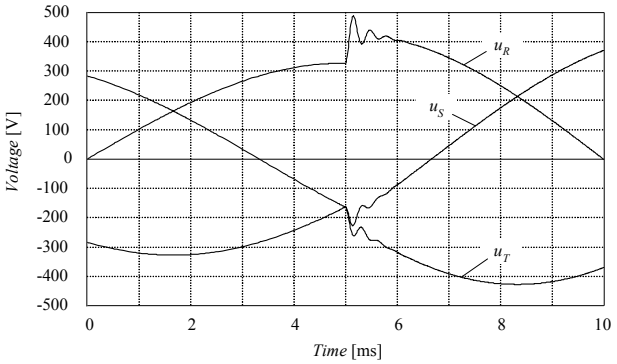

Fig. 12: Filter output voltage time behavior for a step-like change $\Delta\hat{U} = 100\text{V}$ of the input voltage amplitude (filter output in open circuit, like given for no-load operation of the rectifier system).

III.3 Filter Output Impedance

The filter output impedance is important for the stability of the converter in combination with the input filter. For ensuring stability within the whole control bandwidth, among other requirements the condition

$$\left|Z_{o,Filt}\right| \ll \left|Z_{i,Rect}\right| \tag{3}$$

has to be fulfilled, i.e. the magnitude of the filter output impedance has to be significantly lower than the rectifier input impedance [7],[6], which is approximated for perfect control by

$$\left|Z_{i,Rect}\right| = \left|-\frac{U_o^2}{P_o}\cdot\frac{1}{M^2}\right| \tag{4}$$

where $M = \hat{I}_N/I$ is the modulation index, P_o the output power and U_{o} the rectifier output voltage. The magnitude plot of the output impedance is shown in **Fig. 13** for different mains impedances. With the minimum rectifier input impedance magnitude $|Z_{i,Rect,min}| = 32\Omega$ occurring at maximum modulation index $M = 1$ and rated output power, the bandwidth of the system control (i.e. of the inner current control loop of the cascaded output voltage control) has to be limited to

$$B_{w,\max} \approx 2\ kHz\ . \tag{5}$$

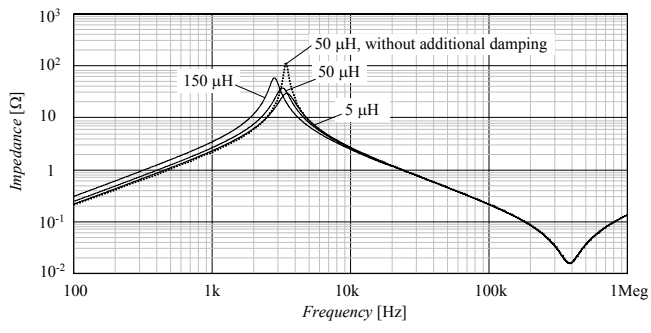

Fig. 13: Magnitude of the filter output impedance for three different inner mains impedances (inductances) L_{mains}.

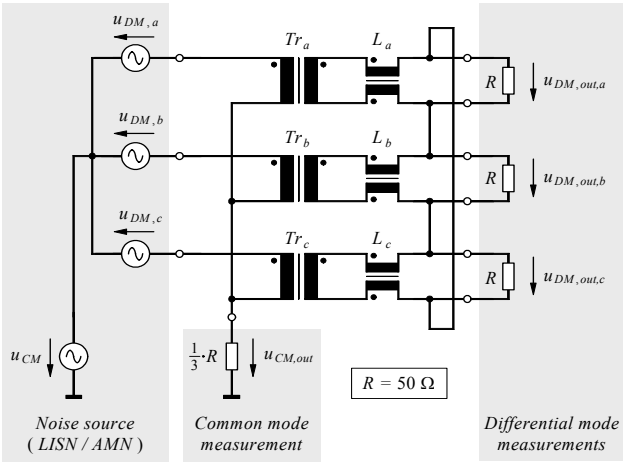

Fig. 14: Circuit schematic of the three phase CM/DM mode noise separator.

(cf. (3) and Fig. 13). Introducing the additional filter damping described in section III.1 does slightly reduce $Z_{o,Filt}$ around the first resonant frequency (cf. Fig. 13). A substantial reduction of $Z_{o,Filt}$ and/or increase of the control bandwidth could only be achieved by increasing C_1 in capacitance (and lowering the series inductances) what, however would result in a higher reactive power consumption at light load.

IV. Experimental Verification

IV.1 Measurement Setup

For the EMC measurements the following system operating condition was considered:

Input (3-ϕ AC)

Input RMS line-to-line voltages	$U_{rms,l\text{-}l}$ = **3 x 400 V**
Input RMS phase current	$I_{N,rms,,max}$ = **7.6 A**
Mains frequency	f_{mains} = **50 Hz**

Output (DC)

Output voltage	U_o = **400 V**
Rated output power	P_o = **5 kW**

Switching frequency f_s = **28 kHz**

The components employed in the input filter are compiled in **Table I**.

Conventional EMC measurements are only providing information on the total electromagnetic emissions and/or do not allow a separation into a common-mode (CM) and a differential-mode (DM) component. Therefore, for validating the DM input filter design, a three-phase CM/DM noise separator [5] has to be employed (cf. **Fig. 14**). The separator requires simultaneous access to all phase outputs of the LISN which, however, is typically not provided by commercial four-line networks. Therefore, in the case at hand two two-line LISNs (Rohde & Schwarz – ESH3-Z5) and a four-line LISN (Rohde & Schwarz – ESH2-Z5) were employed (three identical two-line LISNs were not available at the time of the measurements). There, no remarkable difference of the noise levels of the three phases could be noticed.

IV.2 EMC Compliance Measurements

Fig. 15 shows the result of the DM noise measurement using a Rohde & Schwarz – ESPI test receiver for one phase in the frequency range relevant for the DM conducted emissions, i.e. for 150kHz – 3MHz. The predictions by simulations (cf. section II) are indicated by "x", and are in good accordance with the measured

Table I – Input Filter Components.

Qty.	Component	Specification
3	C_1, X2 capacitor	Evox-Rifa – PHE840M 6.8 μF – 275/280V$_{ac}$
6	C_2, C_{2d} X2 capacitor	Evox-Rifa – PHE840M 470nF – 275/280V$_{ac}$
30	R_{1d}, SMD resistor	6.8Ω – 0805
9	R_{2d}, SMD resistor	62Ω – 0805
3	L_1, L_{1c}, Coupled inductor	Magnetics, High Flux 58439-A2 – 51:7 turns – 14AWG
3	L_{1d}, Inductor	Magnetics, MPP 55894-A2 – 22 turns – 14AWG

noise level. Especially the first peak occurring in the measurement range at f = 168kHz,

$$u_{F,sim} = 60.7\text{dB}\mu\text{V}\ , \tag{6}$$

which served as basis for the whole input filter design (cf. section II), is very close to the measured result

$$u_{F,meas} = 61.8\text{dB}\mu\text{V} \tag{7}$$

what clearly verifies the dimensioning procedure. The small difference to the simulation results (which is also changing by ± 0.5dB for the three phases) is due to tolerances of filter parameters and small asymmetries of the CM/DM separator and the LISN arrangement. The increase of the noise level around 500kHz, 1MHz and 1.2MHz is caused by parasitics of the rectifier power circuit resulting, e.g. in a ringing of the rectifier output inductor current at each switching instant.

IV.3 Mains Current Quality

Besides the DM noise level also the measured mains current waveform is in good correspondence with the simulations (cf. **Fig. 16**). The deviations from a purely sinusoidal shape are originating from delays of the AD-conversion of the rectifier input voltages which provide the basis for the sector detection [4] and the PWM generation and remain limited to small values due to the proper filter damping.

The measured low frequency mains current harmonics are presented in **Fig. 17** and are well below the limits defined in the IEC 61000-3-2 for Class A equipment being relevant in the case at hand.

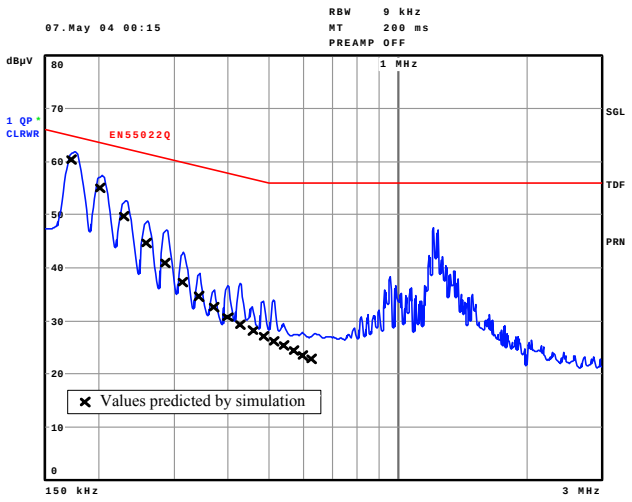

Fig. 15: Conducted emission measurements at one DM output of the CM/DM mode noise separator (cf. Fig.14).

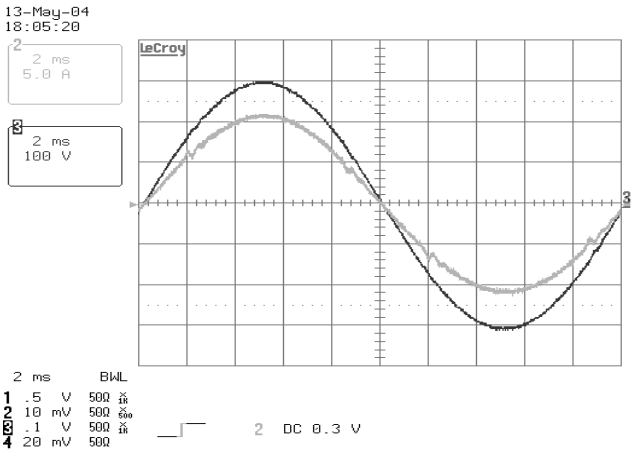

Fig. 16: Measured rectifier mains current (gray line, 5A/div) and mains phase voltage (black line, 100V/div) resulting for the proposed input filter when connecting the system to an artificial mains formed by a high power analog amplifier at the operating parameters as specified in section IV.1.

V. Conclusions

In this paper the DM input filter of a three-phase buck-type PWM rectifier has been designed and optimized based on a simulation model of the system, the LISN and the test receiver. For the considered two stage filter topology a coupling of the inductors of the first stage and a parallel damping of the second stage has been employed in order to provide sufficient damping of the filter resonances without decreasing the attenuation in the frequency range considered for the EMC measurements. The filter damping avoids the amplification of harmonics at multiples of the switching frequency, reduces the amplitudes of oscillating currents and voltages resulting from mains voltage distortions and decreases the filter output impedance at parallel resonant frequencies what facilitates the design of the system control. As verified by DM measurements the proposed dimensioning procedure ensures compliance to EN55022 and therefore constitutes an important step towards a virtual prototyping of the rectifier system.

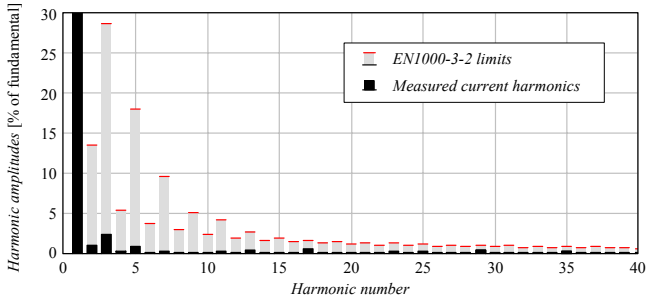

Fig. 17: Measured low frequency harmonics of the mains current in comparison to the IEC 61000-3-2 limits.

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