Design and Comparative Evaluation of Three-Phase Buck+Boost and Boost+Buck Unity Power Factor PWM Rectifier Systems for Supplying Variable DC Voltage Link Converters

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***Abstract* – A three-phase boost+buck PWM rectifier system formed by series connection of a boost-type rectifier input stage and a DC/DC buck converter output stage and a three-phase buck+boost PWM rectifier system comprising a three-switch rectifier input stage with integrated DC/DC boost converter output stage are presented and comparatively evaluated. Both systems are characterized by sinusoidal input current and wide output voltage control range. Analytical expressions for the calculation of the current stresses on the power components and results of transistor switching loss measurements are provided as guidelines for the system design. Furthermore, the overall efficiency, the loss contributions and the volume and weight of the main components are given for 6kW rated system output power at 400V$_{rms}$ line-to-line input. In combination with an assessment of the realization effort this provides a basis for the selection of the appropriate topology for an industry application.**

I. INTRODUCTION

For industrial applications like variable speed six-step inverter drives or pulsed plasma power supplies a variable DC voltage has to be provided which could be generated using a buck+boost converter concept (**Fig.1**(a)), formed by the integration of a three-switch buck-type input stage and a boost-type output stage [1]. Alternatively, a three-level boost-type PWM (Vienna) rectifier [2] with series connected three-level buck-type output stage (cf. Fig.1(b)) could be employed. Up to now, no comparison of both systems has been given in the literature.

In this paper, the converter concepts are compared for a 6kW plasma power supply application with 400V three-phase line-to-line input and a DC output voltage range of U_{out} = 200…600V. In **section II** results of measurements of the power semiconductor switching losses of the buck+boost topology are compiled. There, in part A a realization of the three buck-type bridge legs with power modules is considered, while in part B a realization based on discrete semiconductor components is discussed. In **section III** the same procedure is followed for the boost+buck alternative, again for a module-based and a discrete realization. Finally, in **section IV** the concepts are compared concerning total efficiency, power component size and volume, realization effort and system aspects.

II. BUCK+BOOST TOPOLOGY

The principle of operation, the derivation of the analytical expressions for the current stresses of the buck+boost rectifier power components and the system design procedure have been described in detail in a prior publication [1], and are therefore omitted here for the sake of brevity.

II.A Realization using Power Modules

As a basis for determining the overall performance and the system efficiency which show a strong dependency on the employed power semiconductors and on the gate-drive and the modulation scheme are determined by measurements. There, the buck+boost stage bridge-legs are realized using novel multi-chip power modules (IXYS VUI 31-12N1) [3] (cf. **Fig.2**), which result in a very compact design, low manufacturing effort and low parasitic wiring inductances and/or allow high switching speeds resulting in low switching losses. The prototype of the power part PCB is shown in **Fig.3**. For all further considerations, a modulation method showing minimum switching losses and minimum ripple amplitudes of the input filter capacitor voltage and output inductor current [1] and minimum input current distortions [4] is employed.

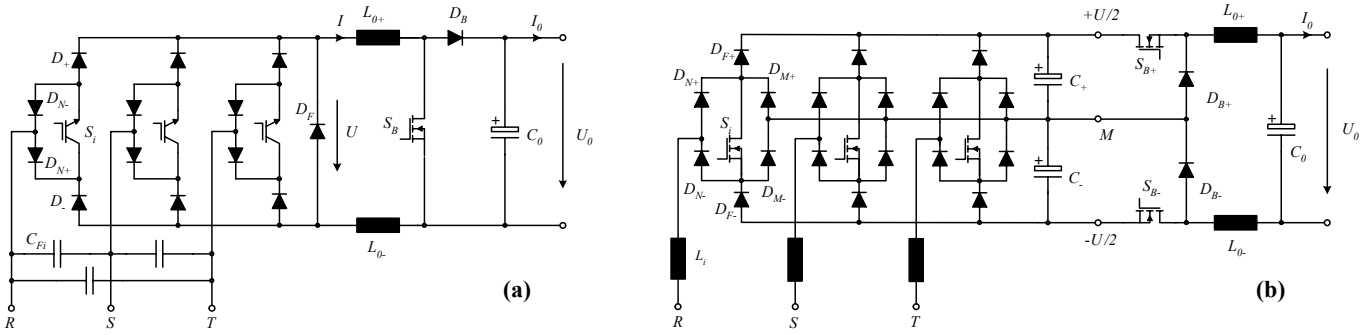


Fig.1: (a) Three-phase/switch buck-type PWM rectifier with integrated two-level boost-type output stage; **(b)** three-phase/level/switch-boost-type PWM (Vienna) rectifier with three-level buck-type output stage.

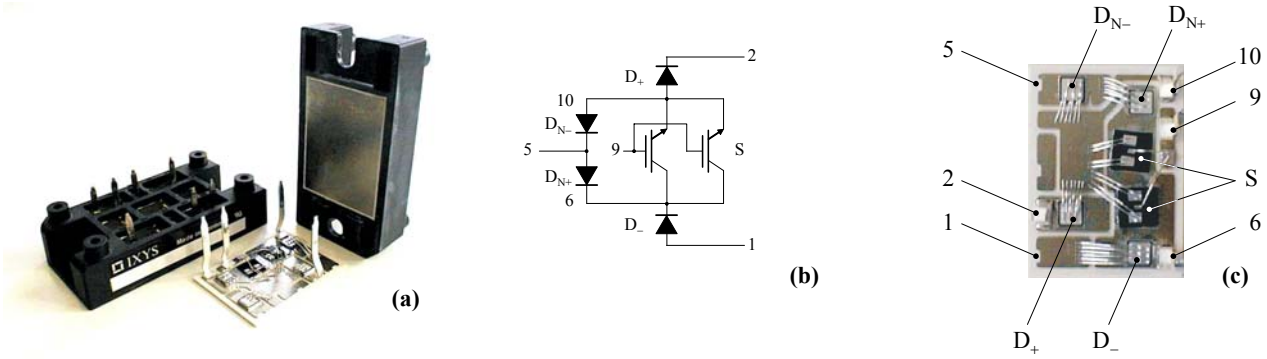


Fig. 2: Novel power module **(a)** IXYS VUI 31-12N1, integrating all semiconductors of one bridge leg of the three-phase three-switch buck-type PWM rectifier; internal structure **(b)** and internal layout **(c)** of the power module.

Once the dependency of the switching losses on the switched voltage and current is given, the total efficiency can be calculated for different operating points where the conduction losses can be included based on data sheet specifications and the losses of the passive power components and the auxiliary power (control electronics, fans) have to be considered.

II.A.1 Switching Loss Measurements

The switching losses of the power module IXYS VUI 31-12N1 are measured using the the experimental setup shown in **Fig.4**(a) were the instantaneous values of the AC mains line-to-line voltages are simulated by DC voltage sources. Due to the phase symmetry it is sufficient to determine the losses for a single combination of signs of the phase voltages and/or in a π/6-wide interval of the mains period (cf. (7)). In the case at hand, the DC voltages are varied in the range $u_{RS} \in (0;\hat{U}_{N,LL})$ and $u_{ST} \in (0;\hat{U}_{N,LL})$ with $u_{RS} + u_{ST} = \hat{U}_{N,LL} = 750\text{V}$ for simulating the voltage condition $u_R > 0 > u_S > u_T$.

In order to cover all switching actions occurring within one pulse period the switching state sequence depicted in Fig.4(b) is employed. There, t_{rise} is a variable time which can be adjusted dependent on the current to be switched, $t_d = 3.3\mu\text{s}$ is a constant time in between the switching actions. The switching pattern can be directly used for the analysis of the losses occurring for the above-mentioned optimum modulation method. Due to the voltage condition $u_R > 0 > u_S > u_T$ given within t_{rise} the phases *R* and *T* are conducting. At t_1 the current is commutated from phase *R* to phase *S* and at t_2 from the transistors S_S and S_T to the freewheeling diode D_F. At t_3 the current is commutated back to phases *S* and *T*, and at t_4 from phase *S* to phase *R*.

Due to the low repetition rate of the switching sequence the power semiconductor junction temperature can be considered equal to the heat sink temperature which is 25°C or increased above room temperature by heating resistor R_T of the heat sink. For the measurements described in the following the junction temperature was set to 125°C.

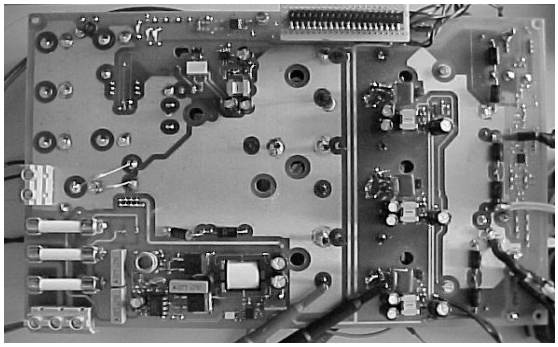


Fig.3: Top view of the power part PCB

The measurements are carried out using a digital storage oscilloscope LeCroy WavePro 950SW (4GS/s), high voltage differential probes LeCroy DA1855A and a purpose-built flat AC current probe, cf. **Fig.5**).

For explaining the basic switching behaviour, switching actions are shown for $U_{RS} = U_{ST} = 375\text{V}$ and $I = 20\text{A}$ adjusted by proper selection of t_{rise}.

Fig.6(a) shows the turn-off behaviour of switch S_R at t_1. The rate of change of the current directly defines the switching overvoltage in combination with the commutation path inductance $L_{\text{RT}\rightarrow\text{ST}}$ (commutation of *I* from phase *R* to phase *S*).

Hence, besides an advantageous selection of the gate resistor defining the switching speed a low commutation inductance $L_{\text{RT}\rightarrow\text{ST}}$ (cf. **Fig.7**(a)) is required for achieving low switching losses which are measured for the final power PCB layout. Fig.7(b) shows the commutation path at t_2. There, the current is commutated from phase *S* and phase *T* to the freewheeling diode. Switching losses are occurring in S_T. Since the inductance $L_{\text{ST}\rightarrow\text{DF}}$ is only insignificantly higher than $L_{\text{RT}\rightarrow\text{ST}}$ the switching behavior is very similar to Fig.6(a) and therefore omitted for the sake of brevity.

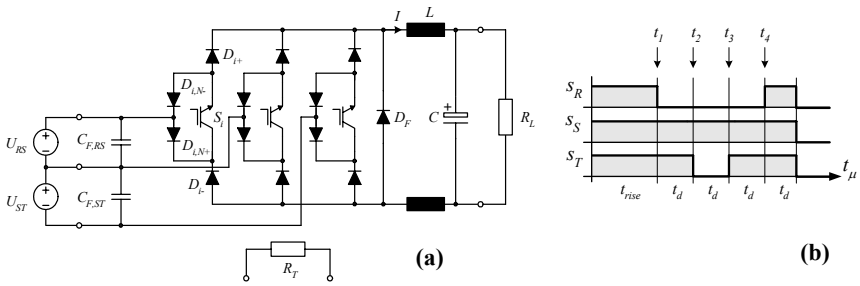
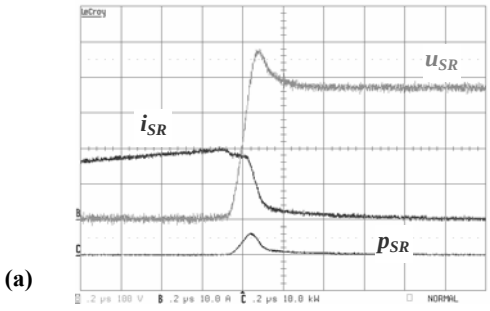
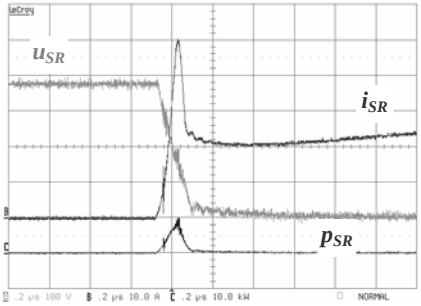


Fig.4: (a) Experimental setup for measuring the switching losses; **(b)** applied switching pattern



(a)



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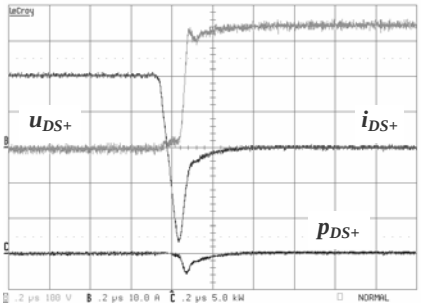

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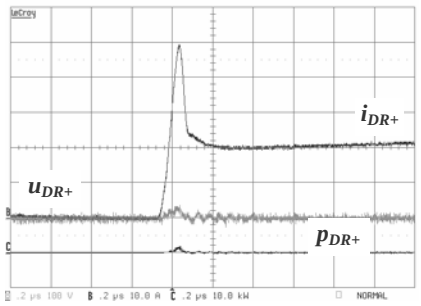


(d)

Fig.6: (a) Switching losses of S_R for turn-off at t_1; **(b)** switching losses of S_R for turn-on at t_4; **(c)** reverse recovery behaviour of the module diode D_{S+} for turn-on of S_R at t_4; **(d)** forward recovery behaviour of module diodes $D_{N,R+}$ and D_{R+} for turn-on of S_R at t_4. Scales: 100V/div, 10A/div, 10kW/div, 200ns/div.

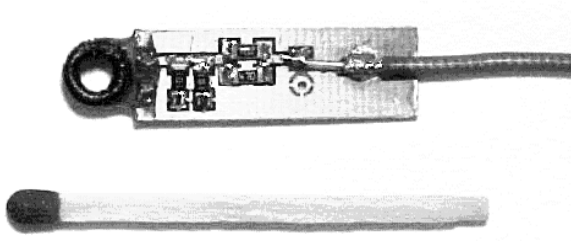
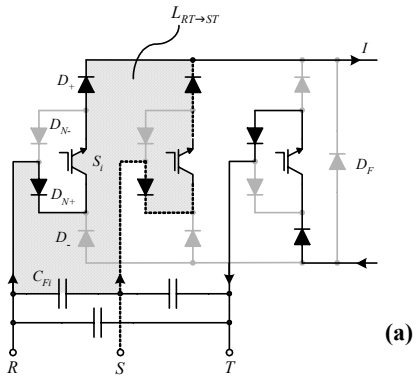


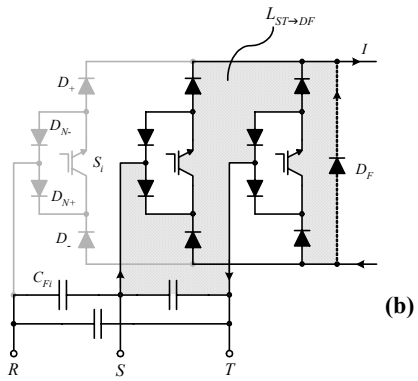
Fig. 5: AC current probe used for module current measurements.

In Fig.6(b) the switching waveforms are depicted for the turn-on of phase R in t_4. The high reverse recovery current ($I_{rr,max}$ = 48A) is originating from module diode D_{S+} and takes significant influence on the IGBT turn-on losses, while the diode reverse-recovery losses are relatively small (cf. Fig. 6(c)). The reverse recovery current is also causing forward recovery losses in the module diodes in the current path of phase R, namely D_{NR+} and D_{R+}.

Likewise, in t_3 the reverse recovery current of the free-wheeling diode D_F (cf. Fig.6 (c)) results in IGBT turn-on losses, reverse recovery losses of D_F, and forward recovery losses in the module diodes D_{S+}, $D_{S,N+}$, D_{T-} and $D_{T,N-}$. Due to the presence of four diodes in the current path the forward recovery losses cannot be neglected in this case.



(a)



(b)

Fig.7: Current commutation paths, where the current path before the switching action is indicated using a solid line and the current path after the switching action is shown by a dotted line; **(a)** commutation between two active states ($R+/T\rightarrow S+/T-$) with a commutation inductance of $L_{RT\rightarrow ST}$ = 111nH; **(b)** switching from an active state into the freewheeling state ($S+/T- \rightarrow D_F$) with a commutation inductance of $L_{ST\rightarrow DF}$ = 115nH.

Time	Switching Loss Parameters							
		k_1	k_2	k_3	k_4	k_5	k_6	k_7
t_1	$S_{off,S\rightarrow S}$	153.7	$32 \cdot 10^{-3}$	$241 \cdot 10^{-3}$	$123 \cdot 10^{-3}$	$-5 \cdot 10^{-3}$	-	-
t_2	$S_{off,S\rightarrow D}$	222.8	-3.5	$769 \cdot 10^{-3}$	$-131 \cdot 10^{-3}$	$5.3 \cdot 10^{-3}$	-	-
t_3	$S_{on,D\rightarrow S}$	116.2	-2.2	5.3	-213	$5.4 \cdot 10^{-3}$	-	-
t_4	$S_{on,S\rightarrow S}$	91.5	-1.9	1.4	$19 \cdot 10^{-3}$	$3.7 \cdot 10^{-3}$	-	-
t_3	$D_{F,rev,D\rightarrow S}$	24.5	$61 \cdot 10^{-3}$	$-909 \cdot 10^{-3}$	$93 \cdot 10^{-3}$	$-2.3 \cdot 10^{-3}$	-	-
t_4	$D_{M,rev,S\rightarrow S}$	44.9	$-625 \cdot 10^{-3}$	$-164 \cdot 10^{-3}$	$-10 \cdot 10^{-3}$	$1.8 \cdot 10^{-3}$	-	-
t_3	$D_{M,fwd,D\rightarrow S}$	-	-	-	-	-	$4.8 \cdot 10^{3}$	80.8
t_4	$D_{M,fwd,S\rightarrow S}$	12.1					$3.5 \cdot 10^{3}$	192.1
	Units	$nWS(VA)^{-1}$	$nWs(VA^2)^{-1}$	$nWs(V^2)^{-1}$	$nWs(V^2A)^{-1}$	$nWs(V^2A^2)^{-1}$	$nWS(A)^{-1}$	$nWs(A^2)^{-1}$

Tab.1: Loss parameters for turn-on, turn-off, reverse recovery and forward recovery losses. The index S→S indicates the commutation from one switch (e.g. of phase *R* at t_1) to another switch (e.g. of phase *S* at t_1), S→D indicates the commutation from a switch (e.g. of phase *S* at t_2) to a diode (e.g. the freewheeling diode at t_2). D_M indicates one of the module diodes.

In order to determine a general dependency of the switching energy losses on the switched current and voltage, measurements for currents I = (5A, 10A, 15A, 20A, 25A) and voltages U_{ij} = (200V, 375V, 550V, 700V) with $ij = RS, ST, TR$ were carried out and combined in least square approximations,

$$w = k_1 \cdot u \cdot i + k_2 \cdot u \cdot i^2 + k_3 \cdot u^2 + k_4 \cdot u^2 \cdot i + k_5 \cdot u^2 \cdot i^2 + k_6 \cdot i + k_7 \cdot i^2 \quad (1)$$

where the parameters $k_1 \ldots k_7$ are listed in **Tab.1** for all relevant loss contributions.

In **Fig.8** the results of the switching loss measurements and the polynomial approximations are depicted for the IGBT turn-off and turn-on (at t_1 and t_4, respectively, cf. Figs.(a), (b)), and for the reverse recovery losses of the module diode D_{S+} for the turn-on of S_R at t_4 (cf. Fig.8(c)) and for the forward recovery losses of the module diodes $D_{N,R+}$ and D_{R+} for the turn-on of S_R at t_4.

II.A.2 Calculation of Switching Losses

The calculation of the switching losses for a certain operating point is based on the general switching loss function (1). The switched current $i = I$ is impressed by the output inductor and shows a constant value determined by the output power

$$I = \frac{P}{U} = \frac{2}{3}\frac{P}{M \cdot \hat{U}_N}. \quad (2)$$

where $M = \hat{I}_N / I$ denotes the modulation index ($\hat{I}_N$ is the amplitude of the mains phase current). Due to the buck-type characteristic of the topology the modulation index is limited to $M = M_{\max} = 1$ and/or the maximum DC link voltage is given by

$$U_{\max} = \frac{3}{2} \cdot \hat{U}_N \cdot M_{\max} = 490V. \quad (3)$$

If an output voltage $U_0 > U_{\max}$ is required, the boost stage is activated. The modulation index of the buck input stage is

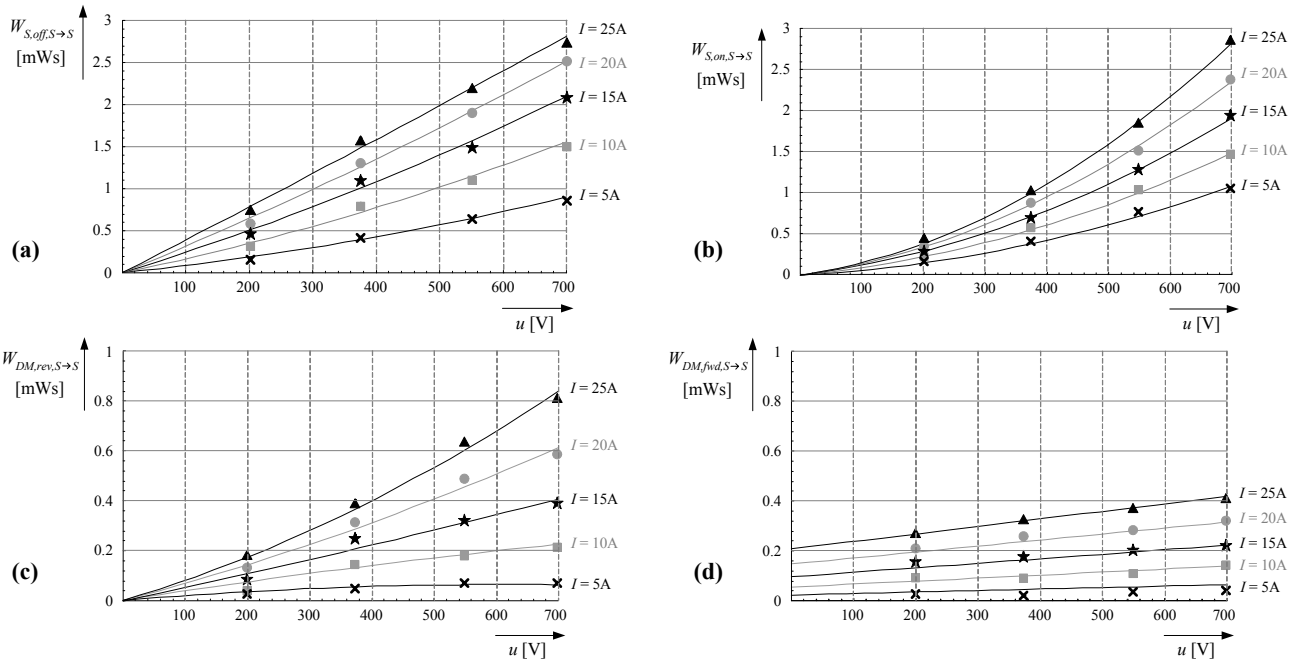


Fig.8: Switching loss measurement data (for junction temperature T_j = 125°C) and least-square approximations showing the dependency on switched voltage and current. **(a)** IGBT turn-off power loss $W_{S,off,S\rightarrow S}$ (at t_1); **(b)** IGBT turn-on power loss $W_{S,on,S\rightarrow S}$ (at t_4); **(c)** reverse recovery loss of the module diode $W_{DM,rev,S\rightarrow S}$ (occurring for D_{S+}) for the turn-on of S_R (at t_4); **(d)** forward recovery loss of the module diode $W_{DM,fwd,S\rightarrow S}$ (occurring for $D_{N,R+}$ and D_{R+}) for the turn-on of S_R (at t_4). The index $S\rightarrow S$ indicates the commutation from one switch (of phase *R* at t_1) to another switch (of phase *S* at t_1) and should not be confused with the index *S* denominating phase *S*.

$$M = \frac{2}{3}\frac{U_0}{\hat{U}_N} \quad \text{for} \quad U_0 = 200...490V$$

and (4)

$$M = 1. \quad \text{for} \quad U_0 = 490...600V$$

The switched voltage u in (1) is time-dependent and equal to a line-to-line voltage

$$u = u_{RS}(\varphi) = \sqrt{3}\cdot\hat{U}_N \cos(\varphi + \frac{\pi}{6}) \quad \text{for} \quad t = t_1 \text{ and } t = t_4 \quad (5)$$

or

$$u = u_{ST}(\varphi) = \sqrt{3}\cdot\hat{U}_N \cos(\varphi - \frac{\pi}{2}) \quad \text{for} \quad t = t_2 \text{ and } t = t_3 \quad (6)$$

(cf. Fig.4(b)). Due to the considered voltage condition $u_R > 0 > u_S > u_T$ which is valid for $0 < \varphi < \pi/6$ (φ denotes a position within the mains period where the mains phase voltage is defined as $u_R = \hat{U}_N \cos(\varphi)$, $\varphi = \omega t$) the average switching losses can be calculated by integration over a $\pi/6$-wide interval

$$P = f_S \cdot \frac{6}{\pi}\int_0^{\pi/6} w(u,i)d\varphi \ . \quad (7)$$

E.g. we have for the IGBT turn-off losses $P_{S,off,S\to S}$ in t_1

$$P_{S,off,S\to S} = f_S \cdot \frac{6}{\pi}\int_0^{\pi/6} w_{S,off,S\to S}\{u_{RS}(\varphi), I\}d\varphi \quad (8)$$

The switching losses of other power semiconductors of the buck-type input stage follow in an analogue manner.

Power Module IGBTs

Referring to (2) - (5) and the switching loss parameters given in **Tab.1** one can calculate the total switching losses of the three IGBTs of the input stage

$$P_{Sw,IGBTs} = P_{S,off,S\to S} + P_{S,off,S\to D} + P_{S,on,D\to S} + P_{S,on,S\to S} \ . \quad (9)$$

Due to the phase symmetry the considerations can again be restricted to the considered input voltage condition.

Diodes

Power Module Diodes

The total switching losses of the module diodes are the sum of the reverse and forward recovery losses

$$P_{Sw,DM} = P_{DM,rev,S\to S} + 2\cdot P_{DM,fwd,S\to S} + 4\cdot P_{DM,fwd,D\to S} \ . \quad (10)$$

Free-wheeling Diode

For the switching losses of the freewheeling diode only the reverse recovery losses are considered

$$P_{Sw,DF} = P_{DF,rev,D\to S} \ . \quad (11)$$

Boost Stage MOSFET

The calculation of the switching losses of the boost converter can be performed with good accuracy by only considering the turn-on and turn-off losses of the switch and the reverse-recovery losses of the output diode. According to measurement results a linear dependency of the switching losses on the switched current can be assumed for a given switched voltage. The switching parameters for the utilized diode-switch combination are given in **Tab.2** for U_{sw} = 400V. We then have for the losses of the boost-stage power MOSFET [5]

$$P_{Sw,SB} = f_S \cdot (k_{ON} + k_{OFF}) \cdot I \quad (12)$$

for a constant current I.

Boost Stage Diode

For the reverse recovery losses of the boost diode [6] one receives

$$P_{Sw,DB} = f_S \cdot k_{rr} \cdot I \ . \quad (13)$$

II.A.3 Calculation of the Conduction Losses

The forward characteristics of the employed power semiconductors are well specified in the datasheets and are compiled in Tab.2. The analytical approximations for the calculation of the average and rms-values of the diode and transistor currents [1] are shown in **Fig.9**.

Power Module IGBTs

The forward characteristic of the IGBTs is approximated by

$$u_{CE} = U_{CE,0} + r_{CE,on} \cdot i_S \ . \quad (14)$$

Therefore, we have for the losses of the IGBTs

$$P_{Fw,IGBT} = U_{CE,0} \cdot I_{S,avg} + r_{CE,on} \cdot I^2_{S,rms} \ . \quad (15)$$

Diodes

The module diodes and the freewheeling diode are showing forward losses

$$P_{Fw,D} = U_F \cdot I_{D,avg} + r_D \cdot I^2_{D,rms} \ , \quad (16)$$

where the corresponding diode parameters U_F and r_D have to be inserted.

Boost MOSFET

Since the forward voltage drop of a power MOSFET is

$$u_{DS} = R_{DS,on} \cdot i_{SB} \ , \quad (17)$$

the forward losses follow via

$$P_{Fw,MOSFET} = R_{DS,on} \cdot I^2_{SB,rms} \ . \quad (18)$$

Boost Diode

The conduction losses of the boost diode can be calculated using

$$P_{Fw,DB} = U_{F,DB} \cdot I_{DB,avg} + r_{DB} \cdot I^2_{DB,rms} \quad (19)$$

in analogy to the diodes of the modules or the free-wheeling diode.

Component	Specifications		
Module IGBT S_i	IGBT @1200V,20A, U_{CE0}=1V , r_{CE}=60mΩ,		
Module Diodes D_{Ni}, D_i, D_F	Diode @1200V,30A U_F=1.65V , r_D=180mΩ,		
Discrete IGBT S_i	SGH20N120RUF, U_{CE0}=1.28V , r_{CE}=35mΩ,	IGBT @1200V,20A, $k_{I,on}$=42µJ/A, $k_{I,off}$=66µJ/A,	
Discrete Diodes D_{Ni}, D_i, D_F	RHRP30120 U_F =0.97 , r_D=24mΩ,	Diode @1200V,30A $k_{I,rr}$=5µJ/A	
S_{Boost}	SPW47N60C3 $R_{DS,ON}$=70mΩ,	MOSFET @600V,47A $k_{I,on}$=39µJ/A,	$k_{I,off}$=8.3µJ/A
D_{Boost}	30EPH06 U_F=0.67V , r_D=150mΩ,	Diode @600V, 30A $k_{I,rr}$=3.2 µJ/A	
C_{Fi}	PHE840M	C=4.7µF@280VAC	ESR=23mΩ
C_0	B43501	C=2*470µF@420VDC	ESR=140mΩ
L_{0+}, L_{0-}	METGLAS	L=450µH@30A	AMCC16B, N=58

Tab.2: Specifications of the utilized components for the module-based and discrete realization of the buck+boost rectifier.

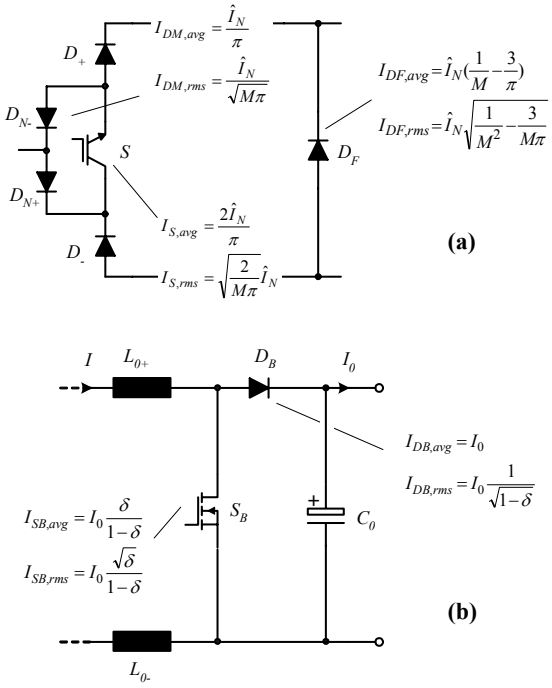


Fig.9: Analytical approximations of average and rms values of the component currents for the three-phase buck+boost PWM rectifier including the dependency on the mains phase current amplitude $\hat{I}_N$ and the current transformation ratio $M = \hat{I}_N / I$; **(a)** rectifier input stage; **(b)** boost output stage.

II.A.4 Additional Losses

For the determination of the total system efficiency in addition to the power semiconductor losses also the auxiliary power (control electronics and cooling fans) and the power losses of the passive components have to be considered.

Input Capacitors

Assuming a constant DC inductor current I and sinusoidally shaped mains phase currents i_N (which can be achieved by a single- or two-stage low-pass LC input filter not shown in Fig.1(a)) the rms value of the input capacitor currents i_{CF} of each phase can be derived by

$$I_{CF,rms}^2 = I_{rec,rms}^2 - I_{N,rms}^2 \tag{20}$$

with

$$I_{rec,rms}^2 = I_{Si,rms}^2 \ . \tag{21}$$

what provides a basis for the filter capacitor selection. The losses of the foil capacitors can be neglected due to the low value of the equivalent series resistance (cf. Tab.2).

Output Inductor

The design of an inductor is under consideration of limiting the peak-to-peak current ripple to

$$\Delta i_{L,p-p,\max} = 0.4 \cdot I \ , \tag{22}$$

(±20%) within the whole operating range. This results in an inductor value of L = 900µH which is split into two individual inductors L_{O+} and L_{O-} in order to allow a compact realization and to reduce the common-mode component of the output voltage.

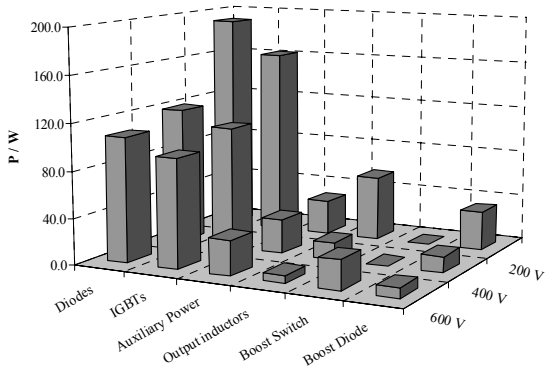


Fig.10: Losses of the power components of the buck+boost PWM rectifier for different output voltage values U_O; operating parameters: 6kW output power, f_S = 25kHz switching frequency.

The selected inductor magnetic core specified in Tab.2 ensures an about equal partitioning of the total losses into core losses [8]

$$P_{L,core}\left[W/kg\right] = 6.5 \cdot \left(\frac{B_{sat}\left[T\right]}{2}\right)^{1.74} \cdot \left(f\left[kHz\right]\right)^{1.51} \tag{23}$$

and copper losses

$$P_{L,Cu} = \frac{l_{Cu}}{\sigma_{Cu} \cdot A_{Cu}} \cdot I^2 \ . \tag{24}$$

Output Capacitor

For limiting the output voltage ripple to

$$\Delta u_{C,p-p,\max} = 0.005 \cdot U_0 \ , \tag{25}$$

an output capacitance of C_0 = 220µF[1] would be required. In order to furthermore accommodate the maximum rms current stress $I_{C,rms,max}$ = 4.74A occurring for operation at U_0 = 600V two 470µF capacitors are employed in parallel. The losses of the output capacitors amount to only P_{C0} = 1.57W (ESR = 140mΩ) and therefore they are therefore neglected for the power loss distribution given in Fig. 10.

Auxiliary Power Supply

For the cooling fans, the power transistors gate-drives and the control electronics a total power consumption of P_{aux} = 30W is assumed.

II.A.5 Power Loss Distribution

In **Fig.10** the loss contributions of the main power components are shown for f_S = 25kHz switching frequency, a mains voltage of $\hat{U}_N$ = √2.230V and different output voltage values in the specified range U_O = 200…600V. For lower output voltages a higher DC link current I is present, accordingly higher losses of the inductors and power semiconductors (mainly conduction losses) do occur.

[1] For active boost output stage and/or discontinuous charging of the output capacitor the output voltage ripple is mainly determined by the equivalent series resistance ESR

II.B Discrete Realization

If low converter volume and low manufacturing effort are not of main importance the bridge legs of the buck-type input stage can also be realized using discrete power semiconductors. This allows a further increase of the system efficiency as latest power semiconductor technology could be employed. In the following, the buck-stage modules are replaced by selected discrete components [10],[11], while the same boost switch and diode as for the module realization are used. The specifications of the selected components are compiled in Tab.2.

The calculations of the switching and conduction losses are based on the same set of formulas as for the module realization in section II.A. However, one has to point out that all calculations are based on datasheet specifications instead of measurements results. Therefore, influences like the actual design of the power PCB and/or the switching loss optimum selection of the gate-drive resistance are not taken into account. In order to compensate for such inaccuracies additional losses of $P_{\text{add}} = 20\text{W}$ are considered.

II.C Overall Efficiency Comparison

Fig.11 shows the overall efficiency for the module-based and the discrete realization of the system for 6kW output power in dependency on the output voltage for different switching frequencies. For the realization with discrete components the efficiency is approximately 0.5% higher than for employing power modules. It also can be seen that an increase of the switching frequency by 5kHz results in a decrease of the efficiency of about 0.2% … 0.5% due to the increasing switching losses of the 1200V IGBTs which have to be employed in the input stage. Therefore, $f_S = 30\text{kHz}$ represents a sensible upper limit for selecting the switching frequency.

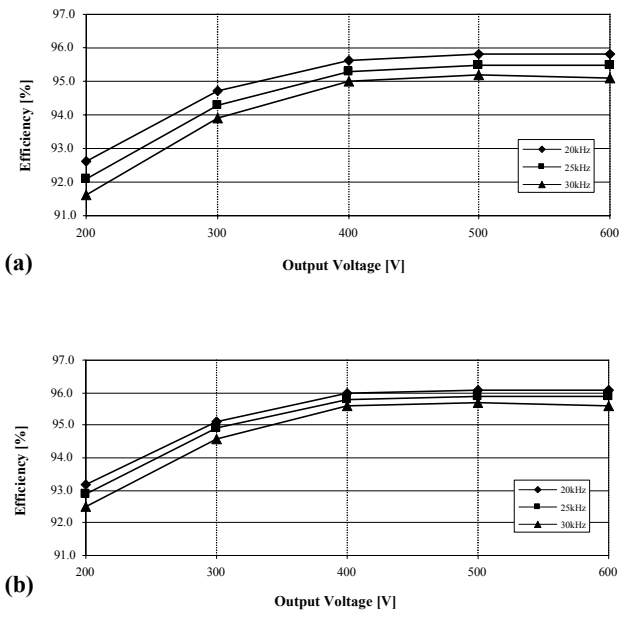


Fig.11: Efficiency characteristics of the buck+boost PWM rectifier operating at 6kW output power for different output voltages and switching frequencies, where **(a)** modules and **(b)** discrete components are employed for the realization of the bridge legs.

III. Boost-Type Rectifier and Series Connected 3-Level Buck Converter

The performance of the three-phase/level/switch boost-type (Vienna) rectifier with a three-level output buck-type converter is investigated in the following. Since for the rectifier phase legs also power modules (IXYS VUM 25-E) comprising a power MOSFET and six diodes [12] are available, again a module-based realization is compared with a discrete solution using latest semiconductor technology.

III.A Realization with Power Modules

III.A.1 Calculation of Switching Losses

Since the switched voltage shows a constant value, $u_{sw}=U_O/2$, the calculation of the power semiconductor switching losses only has to consider the dependency on the switched current. There, according to [13], a linear approximation

$$w = k_1 \cdot i \,. \tag{26}$$

ensures sufficient accuracy. The factors k_1 characterizing the turn-on, turn-off and the reverse recovery losses are compiled in **Tab.3**. The losses are determined using

$$P_{Sw,MOSFET} = f_S \cdot (k_{1,ON} + k_{1,OFF}) \cdot I_{S,avg} \,, \tag{27}$$

$$P_{DF,rr} = f_S \cdot k_{1,rr} \cdot I_{DF,avg} \,. \tag{28}$$

The mains and diodes D_{N+}, D_{N-} and the center-point diodes D_{M+}, D_{M-} are not involved in the switching loss calculations as the commutation of the current is between the power transistors and the free-wheeling diodes. The forward recovery losses of the center point diodes are not considered here, in compensation additional losses of 20W are included in the determination of the system efficiency.

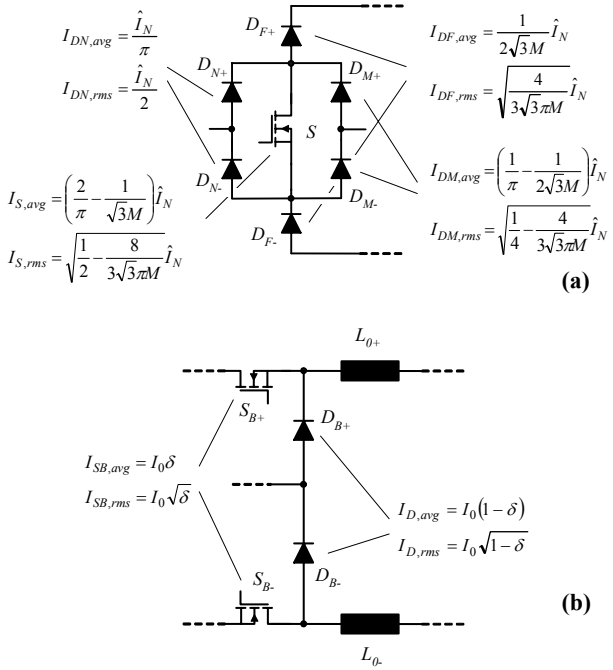


Fig.12: Compilation of the average and rms values of the device currents of the boost+buck PWM rectifier in dependency on the mains current amplitude $\hat{I}_N$ and the voltage transformation ratio $M = U_0/\sqrt{3}\hat{U}_N$; **(a)** rectifier input stage; **(b)** buck-type output stage.

As for the output stage of the buck+boost system (cf. section II) a linear dependency of the switching power losses on the switched current is also assumed for the switch - diode combination of the buck converter [14],[15]. The corresponding parameters k_1 are given in Tab.3 for a switched voltage of $u_{sw}=U/2=400V$. Therefore, one receives for the total switching losses of the three-level buck converter power MOSFETs and the diodes

$$P_{Sw,SB} = f_S \cdot (k_{ON} + k_{OFF}) \cdot I_{SB,avg}\,, \tag{29}$$

$$P_{Sw,D} = f_S \cdot k_{rr} \cdot I_{DB,avg}\,. \tag{30}$$

The switching losses of the whole system are then given by

$$P_{Sw} = 3 \cdot P_{Sw,MOSFET} + 6 \cdot P_{DF,rr} + 2 \cdot P_{Sw,SB} + 2 \cdot P_{Sw,D}\,, \tag{31}$$

where the factor 2 arises from the fact that the three-level buck output stage is formed by two partial converters.

III.A.2 Calculation of Conduction Losses

The power semiconductor conduction losses can be calculated like discribed in section II, where the diode and the transistor losses are determined by (16) and (18). The rms and average current values of the boost-type input and the buck-type output stage are compiled in analytical form in **Fig.12** [13]. The forward characteristics required for the calculation of the conduction losses are extracted from datasheets and listed in Tab.3.

III.A.3 Additional Losses

The calculation of the losses of the input inductors, of the DC link capacitors C_+, C_-, the output inductors L_{0+} and L_{0-}, and the output capacitors C_{0+}, C_{0-} can be performed in a similar way as shown in section II for the buck+boost system. For details we would like to refer to [16] for the sake of brevity. In order to ensure a fair comparison of the two systems the passive components are chosen with respect to equal design guidelines, such as maximum ripple amplitudes of I and U_0 (cf. (22) and (25)) and current and/or voltage stresses (cf. section II.A.4). The selected components are listed along with their specifications in Tab.3.

III.A.4 Power Loss Distribution

In **Fig.13** the system loss distribution is depicted for different output voltages in the specified range $U_O = 200\ldots600V$ for 6kW output power, a mains voltage of $\hat{U}_N = \sqrt{2}\cdot230V$ and $f_S = 50kHz$ switching frequency. As for the buck+boost system the system efficiency decreases significantly with decreasing output voltage.

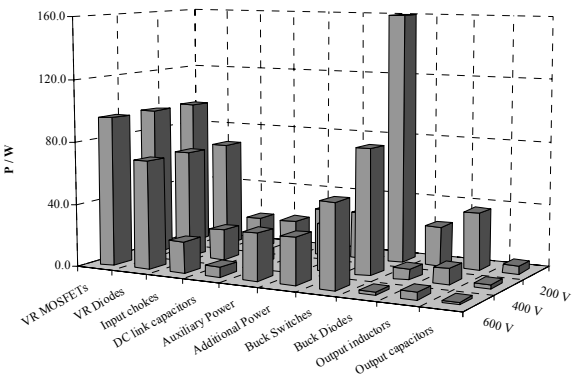


Fig.13: Losses of the power components for the boost+buck PWM rectifier system for different output voltages; operating parameters: 6kW output power, $f_S = 50kHz$ switching frequency.

III.B Discrete Realization

Alternative to using the power module IXYS VUM25-E for the realization of the input stage bridge legs, discrete power semiconductors representing latest power semiconductor technology [5],[17],[18] could be employed (cf. Tab.3). There, the calculations of conduction and switching losses providing the basis for the efficiency comparison are performed in the same way as for the module-based realization.

III.C Overall Efficiency Comparison

As the blocking voltage stress on all power semiconductors of the bosst+buck rectifier is defined by only half the DC link voltage $U/2 = 400V$, 600V power MOSFETs can be employed for realizing the turn-off power semiconductors of the boost input and buck output stage. The effect of the system switching frequency on the efficiency of the energy conversion is detailed in **Fig.14**. Accordingly, switching both stages at $f_S = 50kHz$ ensures a good compromise between power density and efficiency.

Component	Specifications		
Module *MOSFET* S_i	MOSFET @600V,20A, $R_{DS,ON}$=225mΩ		
Module *Diodes* D_{Fi},D_N	Diode @600V,30A U_F=1.15V , r_D=10mΩ		
Module *Diode* D_M	Diode @600V,30A U_F=1.25V , r_D=10mΩ		
Discrete *MOSFET* S_i	SPW47N60C3 @125°C, $R_{DS,ON}$=70mΩ,	MOSFET @600V,47A, $k_{1,on}$=28.5µJ/A, $k_{1,off}$=8.3µJ/A	
Discrete *Diode* D_F	HFA25PB60 @150°C, U_F=0.95 , r_D=24mΩ,	Diode @600V,25A $k_{1,rr}$=3.2µJ/A	
Discrete *Diodes* D_M,D_N	GBPC2506 @150°C, U_F=0.75 , r_D=12mΩ,	Diode @600V,25A	
S_{Boost}	IXKN 75N60C @130°C $r_{DS,ON}$=70mΩ,	MOSFET @600V,75A $k_{1,on}$=39µJ/A, $k_{1,off}$=8.3µJ/A	
D_{Boost}	DSEP 2x91-06A @120°C U_F=1V , r_D=11mΩ,	Diode @600V, 91A $k_{1,rr}$=3.2 µJ/A	
L_{Fi}	METGLAS	L=350µH@20A	AMCC10, N=45
C_+, C_-	B43501	C=4*470µF@420VDC	ESR=140mΩ
L_{0+}, L_{0-}	METGLAS	L=130µH@30A	AMCC8, N=32
C_0	B43501	C=1*470µF@420VDC	ESR=140mΩ

Tab.3: Specifications of the utilized components for the module-based and discrete realization of the boost+buck converter.

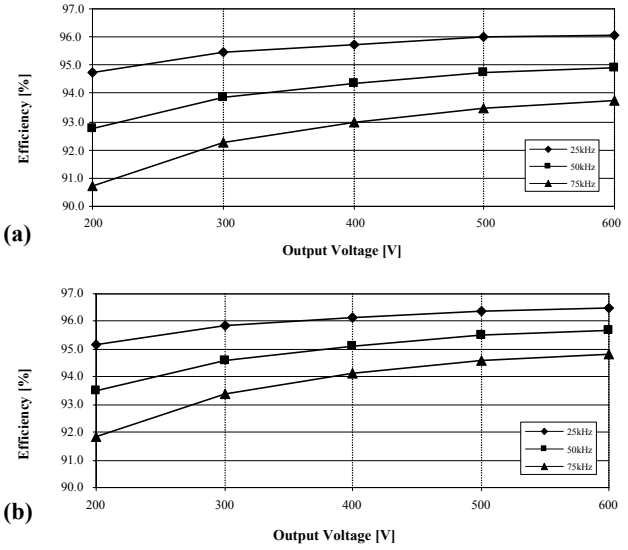


Fig.14: Efficiency characteristics for the boost+buck converter for different output voltages and switching frequencies, where **(a)** modules, and **(b)** discrete components are employed for the realization of the input stage.

IV. COMPARATIVE EVALUATION OF THE SYSTEMS

The buck+boost and the boost+buck systems designed in the foregoing sections are compared in the following concerning

- overall efficiency,
- weight, and
- volume.

In order to ensure a balance a between power density and overall efficiency and a high utilization of the employed semiconductor technology, the switching frequency of the buck+boost system (comprising an IGBT input stage) has been defined as

$$f_{S,BuBo} = 25kHz\ , \tag{32}$$

and as

$$f_{S,BoBu} = 50kHz \tag{33}$$

for the boost+buck system where all turn-off power semiconductors are realized by power MOSFETs.

IV.A Overall Efficiency

The dependency of the efficiency of the buck+boost and the boost+buck rectifier on the output voltage is depicted in **Fig.15.** For each system a realization of the input stage with power modules or discrete power semiconductors is considered. For U_0 = 200V the boost+buck topology shows slightly lower losses than the buck+boost converter where an IGBT is lying in each input phase current path. Due to the relatively high conduction losses (originating from the high output current I at low U_0) and the fast reverse recovery behaviour of the power diodes in combination with the low switching frequency (f_S = 25kHz), switching losses are not taking significant influence on the efficiency despite devices with 1200V blocking capability are employed.

For $U_0 \approx$ 400V the buck+boost topology exhibits the highest efficiency. There, both power transistors of the buck output stage of the boost+buck system are switching half the rectifier stage output voltage, i.e. $u_{sw} = U/2$, therefore, the total buck-stage switching losses are proportional to the full DC link voltage, $P_{sw} \sim U_0 =$ 800V.

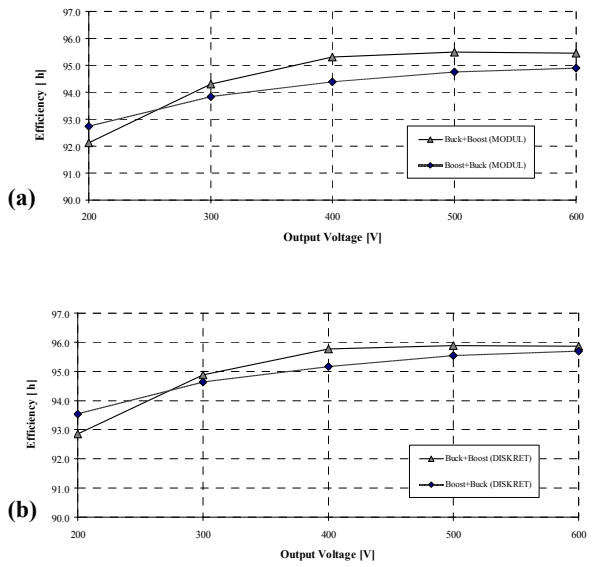


Fig.15: Comparison of the overall efficiencies of the two topologies for different output voltages, where the design is based on (a) modules (b) discrete components for the realization of the 3phase bridge legs.

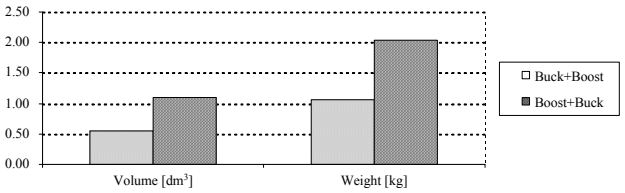


Fig.16: Comparison of volume and weight of the passive components of the buck+boost and the boost+buck PWM rectifier system (heat sink, cooling fans, power semiconductors, auxiliary supply, etc. are not included).

In contrast, always one power transistor of the buck input stage of the buck+boost system remains clamped over a π/3-wide mains interval and the two remaining transistors are switching only a fraction of the highest mains line-to-line voltage. Accordingly, for the *total* input stage switching losses in a rough approximation[2] the peak value of the line-to-line voltage has to be considered only a single-time, i.e. $P_{sw} \sim \hat{U}_{N,l\text{-}l} = \sqrt{2}\cdot 400\text{V} = 565\text{V}$. Furthermore, there are only conduction losses in the diode of the buck+boost converter boost stage as the boost power transistor is activated only for $U_0 > 490$V, while the input (boost) stage of the boost+buck rectifier is operating continuously in order to maintain the PFC function of the system.

IV.B Volume and Weight

The volume and weight of the rectifier systems is mainly determined by the passive components and the heat sink. Since the power losses are comparable for both topologies (cf. Fig.15), volume and size of the required heat sink will show little difference. Assuming an ambient temperature of

$$T_a = 45°C \tag{34}$$

and considering a maximum heat sink temperature of

$$T_h = 95°C \tag{35}$$

being sufficiently lower than the maximum admissible power semiconductor junction temperatures, we have for the thermal resistance of the heatsink

$$R_{th,h} = \frac{T_h - T_a}{(1-\eta)\cdot P_{in}} = 0.1\,\text{K/W} \tag{36}$$

(η denotes the overall efficiency) resulting in a heatsink volume of $V_{hs} = 2.1\text{dm}^3$ and/or a heatsink weight of $m_{hs} = 2.5$kg [19].

In order to highlight the differences of both topologies the heatsink is not included in the comparison depicted in **Fig.16**. The buck+boost topology is advantageous over the boost+buck system concerning weight and volume of the passive power components. This is due to the larger number of inductors required for the boost+buck system where the input inductors despite the higher switching frequency already show a volume comparable to the output inductors L_{0+}, L_{0-} of the buck+boost system. Furthermore, a relatively large DC link capacitor is required for the boost+buck topology in order to accommodate the rms current stress originating from the discontinuous boost stage output and buck stage input currents (advantageously, the switching of both stages is synchronized for minimizing the capacitor current stress). In comparison, the input filter capacitors of the buck+boost rectifier are showing a considerably lower volume.

[2] This approximation shall only show a main characteristic, the dependency of the switching losses on voltage and current according to (1) is not considered here. The actual averaged switched voltage results from integration of (5) and (6) over a π/6-wide interval of the mains period.

IV.C System Aspects

Besides efficiency, weight and volume also system aspects like the behaviour in case of an

- output short-circuit or
- mains voltage unbalance

has to be included in a system evaluation. Furthermore, complexity/reliability and manufacturing effort constitute important aspects.

According to **Tab.4** the buck+boost system shows a considerably lower realization effort/complexitiy of the power and control circuits than the boost+buck topology. Furthermore, it does allow a direct system start-up and/or does not rely on a precharging of a DC link capacitor.

Both systems could be operated in current limiting mode in case of an output short circuit and could maintain unity power factor input behaviour also in case of heavily unbalanced mains and/or loss of a mains phase.

An aspect which has to be given main attention in case of mains voltage distortions and operation of multiple systems in parallel is the proper damping of the input filter of the buck+boost system which should be implemented using passive and active (control) means.

V. CONCLUSIONS

Two three-phase unidirectional unity power factor PWM rectifier topologies, i.e. a buck+boost and a boost+buck system were comparatively evaluated concerning efficiency, volume, weight and system aspects. Both systems are designed for 6kW rated power, $400V_{rms}$ line-to-line input and wide output voltage range U_O=200…600V where a realization of the input stages based on power modules and discrete power semiconductors is considered.

The three-phase buck+boost rectifier shows a slightly higher overall efficiency in a main part of the operating range and is characterized by lower weight and volume of the passive power components. This is also given for including the input filter inductors required for the buck+boost system into the considerations. Reducing the switching frequency of the boost+buck system from 50kHz to 25kHz would reduce the system losses but would also further increase the weight and volume drawback.

A further main advantage of the buck+boost converter over the boost+buck approach is the lower complexity of the power circuit and the lower sensing effort and the soft-start capability. Both concepts do allow an active current limitation in case of an output short circuit and could continue in operation also for heavily unbalanced mains and/or loss of a mains phase (two-phase operation).

	Buck+Boost	**Boost+Buck**
Power transistors	4	5
Power diodes	13	20
Energy storage capacitors	1	3
Voltage sensors	3	4
Current sensors	1	3

Tab.4: Number of components needed for the realization and control of the buck+boost and the boost+buck converter topology, respectively.

With reference to the aforementioned advantages the buck+boost rectifier system will be analyzed in the course of further research for applications in future More Electric Aircrafts which are characterized by high reliability requirements, $115V_{rms}$ rated mains voltage, 400…800Hz mains frequency, and extreme peak to average load ratios.

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