Advanced Modulation Scheme for Three-Phase Three-Switch Buck-Type PWM Rectifier Preventing Mains Current Distortion Originating from Sliding Input Filter Capacitor Voltage Intersections

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***Abstract* – Modulation schemes for three-phase three-switch buck-type PWM rectifiers where the switching state of one bridge leg is clamped within a π/3-wide interval of the mains period do guarantee minimum switching losses as well as minimum input filter capacitor voltage ripple and minimum DC current ripple. However, as shown in this paper by a detailed analysis of the time behavior of the input filter capacitor voltages within a pulse period such modulation schemes are characterized by the occurrence of sliding intersections of the filter capacitor voltages which do cause input current distortion. An advanced modulation scheme is proposed which does prevent the input current distortion and does allow to maintain the optimum performance of conventional modulation schemes.**

I. INTRODUCTION

Three-phase buck-type PWM rectifier systems (also known as current source rectifiers) are employed as front-end converters in utility interfaced systems such as power supplies for telecommunication systems, process technology, and AC drive applications. In [1] a novel three-phase three-switch buck-type unity power factor PWM rectifier with integrated DC/DC boost converter output stage has been presented. This topology combines the advantage of a wide input voltage range and/or output voltage range with a sinusoidal shape of the mains currents lying in phase with the mains phase voltages. Furthermore, the system does allow operation also in case of heavily unbalanced mains and/or in case of a mains phase loss.

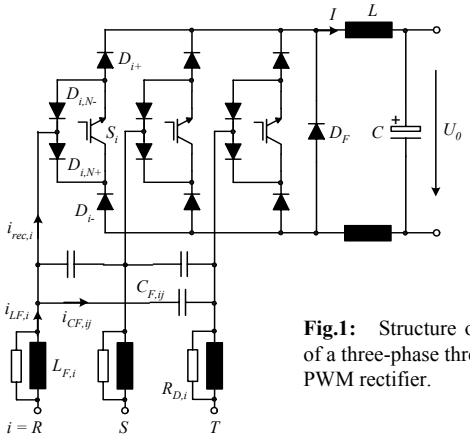

Fig.1: Structure of the power circuit of a three-phase three-switch buck-type PWM rectifier.

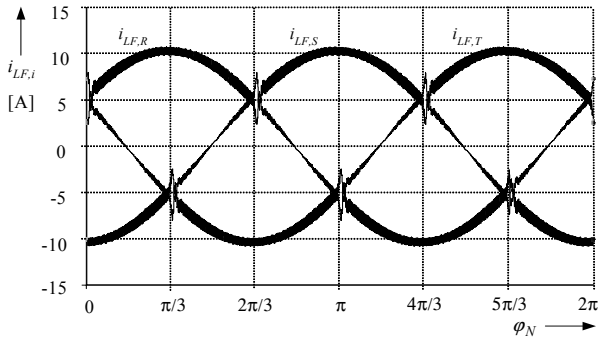

Fig.2: Distortion of the mains phase currents of a three-phase three-switch buck-type PWM rectifier occurring for conventional PWM at the limits $\varphi_N = n\cdot\pi/3$ (n = 1,2,3…) of bridge leg clamping intervals (cf. Fig. 3).

The buck-type input stage of this topology (**cf. Fig.1**) has already been investigated in [2] - [4]. There, different off-line programmed PWM patterns have been discussed, but no optimization of the PWM has been considered. An optimized modulation method concerning switching losses has been proposed in [1], which has been further improved in [5] regarding the minimization of the RMS value of the input filter capacitor voltage ripple, and in [6] regarding the RMS value of the ripple component of the DC link current. There, always one bridge leg is remaining in the on-state and/or clamped within a π/3-wide interval of the mains period. However, digital simulations (cf. Fig.10 in [1]) and the experimental verification (cf. Figs.10 and 11 in [7]) have shown that at the beginning and at the end $\varphi_N = n \cdot \pi/3$ (n = 1,2,3…) of the clamping intervals (cf. **Fig.2**) distortions of the mains current do occur. This effect, which is also present for six-switch buck-type topologies, (cf. e.g. Fig. 5 in [8]) has not been investigated in the literature so far.

In this paper an advanced modulation scheme is proposed which does eliminate the input current oscillations but does maintain the optimum performance of clamping PWM schemes concerning the switching losses and the ripple of the input filter capacitor voltage and the DC link current. In **section II** the basic principle of operation of a three-phase three-switch buck-type PWM rectifier is reviewed briefly.

The origin of the mains current distortion is clarified in **section III**. An advanced modulation scheme preventing the mains current distortion at the beginning and/or end (boundaries) of the clamping intervals also in case of inaccurate detection of the clamping interval boundaries is proposed in **section IV** and verified by digital simulations.

II. Principle of Operation

In the following, a very brief description of the basic principle of operation of the three-phase three-switch buck-type PWM rectifier (cf. Fig.1) shall be given. For a more detailed discussion we would like to refer to [1].

The DC current I being impressed by the DC-side inductor L and/or by an output current control is distributed to the three phases R, S, T, and/or to the freewheeling diode D_F depending on the switching state sequence which is determined by the mains voltage condition. For achieving a resistive fundamental mains behavior

$$i_{LF,i} \sim u_{N,i} \tag{1}$$

with

$$\begin{aligned} u_R &= \hat{U}_N \cdot cos(\omega_N t) \\ u_S &= \hat{U}_N \cdot cos(\omega_N t - 2\pi/3) \\ u_T &= \hat{U}_N \cdot cos(\omega_N t + 2\pi/3) \end{aligned} \tag{2}$$

(cf. **Fig.3**) the relative on-times of the power transistors have to be set according to Eq.(32) in [1]. There, the modulation depth is characterized by a modulation index

$$M = \frac{\hat{I}_N}{I} = \frac{2}{3}\frac{U_0}{\hat{U}_N}, \tag{3}$$

where $\hat{I}_N$ denotes the amplitude of the input currents $i_{LF,i}$.

In [1], [6] and [7] a PWM scheme has been proposed which does allow to simultaneously achieve

- minimum switching losses [1],
- minimum filter capacitor voltage ripple [6], and
- minimum DC inductor current ripple [7].

This scheme is characterized by

- two active switching states (where the DC link current I is switched to always two input phases, i.e. rectifier input currents $i_{rec,i}$, i=R,S,T, do occur) and one freewheeling state (where the current flow I is via the freewheeling diode D_F and/or $i_{rec,i} = 0$ is valid), a
- symmetric switching state sequence within each pulse period, and by the clamping of the transistor of the phase leg showing the lowest absolute value of the corresponding mains phase voltage (cf. Fig.3).

The corresponding switching state sequences are depicted in **Fig. 4** for $0 < \varphi_N < \pi/3$ (sector 1, cf. **(a)**), and $\pi/3 < \varphi_N < 2\pi/3$ (sector 2, cf. **(b)**).

As shown in Fig.3, within the first $\pi/3$ - wide interval $0 < \varphi_N < \pi/3$ of a mains period the transistor S_S is remaining in the on-state. There, at the beginning of a pulse period all

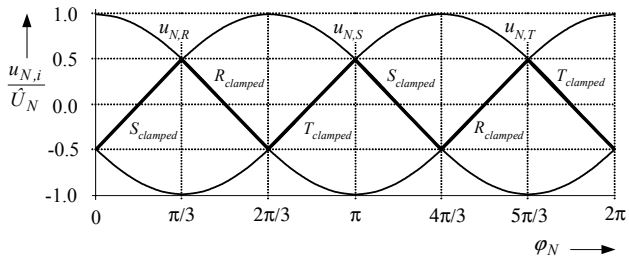

Fig.3: Time behavior of the mains phase voltages $u_{N,i}$, i=R,S,T; the power transistor of the phase showing the lowest absolute instantaneous voltage value, e.g. S_S in $0 < \varphi_N < \pi/3$, is clamped in the on-state.

transistors are turned on, i.e. j = *(111)* (cf. Fig. 4, $j = (s_R\ s_S\ s_T)$ denotes the combination of phase switching functions s_i, i=R,S,T, where $s_i = 1$ denotes the on-state and $s_i = 0$ denotes the off-state of the power transistor S_i). Accordingly, the function of the bridge legs is equivalent to a three-phase diode bridge. For neglection of the voltage drops across the filter inductors, therefore according to the mains voltage conditions $u_{N,R} > u_{N,S} > u_{N,T}$ a current flow in phases R and T, $i_{rec,R} = -i_{rec,T} = I$ does occur. When transistor S_R is turned off and/or j = *(011)* is valid, the current I commutates from phase R to phase S and/or phases S and T are conducting current, $i_{rec,S} = -i_{rec,T} = I$. As always two active bridge legs are required for carrying the DC output current I, the system is forced into the freewheeling state for turning off transistor S_T and/or changing to switching state j = *(010)*.

Since the relation of the instantaneous mains phase voltages $u_{N,R}$ and $u_{N,S}$ is reversed when entering from sector 1 into sector 2, transistor S_R is clamped in the on-state (cf. Fig.3) and S_S is switching and/or the switching patterns of phases R and S are exchanged (cf. Fig. 4(b)).

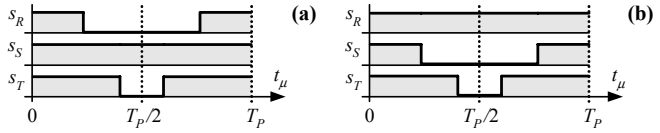

Fig. 4: Switching state sequences for one pulse period depicted for two different mains phase voltage conditions; **(a)** $u_{N,R} > u_{N,S} > u_{N,T}$ and/or $0 < \varphi_N < \pi/3$ (sector 1), and **(b)** $u_{N,S} > u_{N,R} > u_{N,T}$ and/or $\pi/3 < \varphi_N < 2\pi/3$ (sector 2).

III. Sliding Intersections of the Input Filter Capacitor Voltages

For all following considerations we will assume as specifications and/or operating parameters

$$\begin{aligned} &P_0 = 5kW & &\hat{U}_N = \sqrt{2} \cdot 230V & &I = 12.5A \\ &M = 0.82 & &f_P = 20kHz & &L_{N,i} = 150\mu H \\ &L_{F,i} = 150\mu H & &C_{F,ij} = 1.5\mu F & &R_d = 3.9\Omega \end{aligned}$$

where P_0 denominates the rated output power, $\hat{U}_N$ is the peak value of the mains phase voltage and f_P defines the system switching frequency; R_d provides an optimum damping (cf. p. 398 in [9]) of the input filter under consideration of the inner

mains impedance $L_{F,i}$. (One has to note that passive damping is a strict requirement for an industrial application of the rectifier system as active damping schemes cannot prevent input filter oscillations caused e.g. by mains voltage distortions at light load or in the turn-off state of the rectifier system.) Furthermore, we do assume a constant value of the DC output current I in order to clearly show the effect of the sliding intersections of the input filter capacitor voltages on the rectifier input current formation.

As shown in Fig.2 the input current distortion does occur at $\varphi_N = n \cdot \pi /3$, e.g. at the boundaries of a sector. For assuming ideal, ripple-free filter capacitor voltages lying in phase with the line-to-line mains voltages i.e. for neglecting the phase shift due to the input filter inductors, the filter capacitor voltage $u_{CF,RS}$ would decrease to zero in $\varphi_N = \pi/3$. Accordingly, the two remaining capacitor line-to-line voltages $u_{CF,RT}$ and $u_{CF,ST}$ then would show equal values and the voltage relations of phases R and S would reverse when entering into sector 2. Considering the pulse pattern shown in Fig. 4 the rectifier input current $i_{rec,R} = I$ (cf. **Fig.5**(a)) would therefore commutate immediately from phase R to phase S (dashed line in Fig.5(a)).

However, due to the finite filter capacitance the filter capacitor voltage does show a ripple component. Therefore, in practice there is not a single crossover point, but in the vicinity of $\varphi_N = \pi/3$ in sections of the pulse periods $u_{CF,RT}$ and $u_{CF,ST}$ do show equal values (such sections will be denoted as *sliding intervals* in the following). The resulting system behavior is shown in **Fig. 6**. For the considered sector transition the capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ assume equal values the first time when all switches are turned on, i.e. for *j=(111)*, already three pulse intervals before the actual sector limit $\varphi_N = \pi/3$.

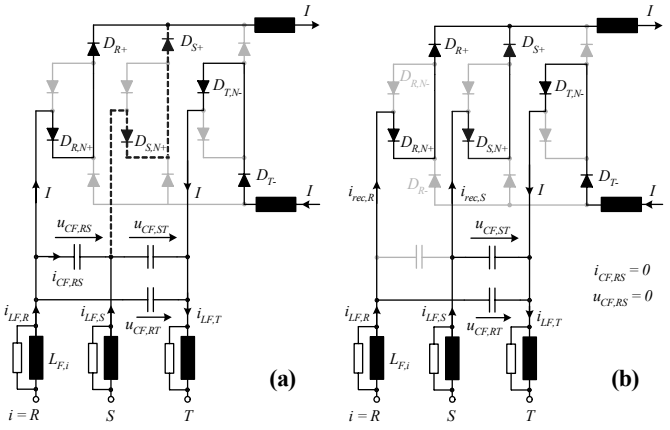

Fig.5: System conduction states for **(a)** $u_{CF,RT} > u_{CF,ST}$ (sector 1, close to $\varphi_N = \pi/3$); in case the filter capacitor voltages would show no ripple, only phase S would carry current (indicated by a dashed line) for $s_S = 1$ in the pulse period following $\varphi_N = \pi/3$. Furthermore shown: conduction state **(b)** when a sliding intersection of the input capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ does occur (rectifier input currents are present simultaneously in the commutating phases R and S). Free-wheeling diode D_F not shown for the sake of clearness.

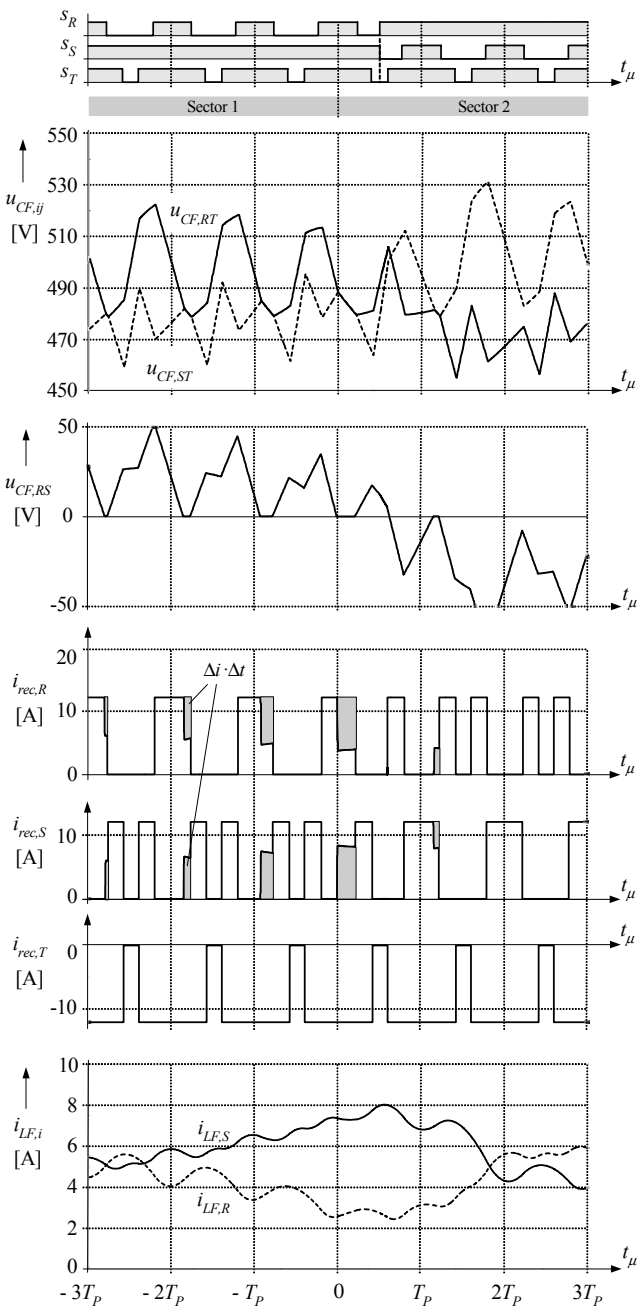

Fig. 6: Time behavior of the power transistor switching functions s_i, i=R,S,T, of the filter capacitor voltages $u_{CF,RT}$, $u_{CF,RT}$, and $u_{CF,RS}$, of the rectifier input currents $i_{rec,R}$, $i_{rec,S}$, and $i_{rec,T}$, and of the mains filter inductor currents $i_{LF,R}$ and $i_{LF,S}$ for conventional modulation. The sliding intervals of the filter capacitor voltages $u_{CF,RT}$ and $u_{CF,RT}$ occurring for switching state j = *(111)* can be clearly identified. **Remark:** In the case at hand the sector information is derived from the inner mains voltages $u_{N,i}$ ($t_\mu = 0$ denotes the sector change according to the inner mains voltage conditions). There, for considering the phase displacement caused by the voltage drop across $L_{N,i}$ and $L_{F,i}$ the sector information is delayed by a half pulse period. Ideally, the sector should be determined based on the filter capacitor voltages which however do contain a large switching frequency ripple component. Accordingly, in practice the filter capacitor voltage fundamentals have to be extracted by band-pass filtering. This does prevent a phase shift at mains frequency which would result in an erroneous sector detection.

Accordingly, there the diodes D_{S+}, D_{SN+} of phase *S* start to conduct, while the diodes in phase *R* remain in conduction (cf. Fig.5(b)). Therefore, the capacitor voltage $u_{CF,RS}$ is clamped to zero and $u_{CF,RT} = u_{CF,ST}$ is valid as long as $j = (111)$ is applied. Due to the equal rate of change of the filter capacitor voltages also the corresponding capacitor currents show equal values

$$i_{CF,RT} = C_F \cdot \frac{du_{CF,RT}}{dt} = i_{CF,ST} = C_F \cdot \frac{du_{CF,ST}}{dt}. \qquad (4)$$

Therefore, rectifier input currents

$$\begin{aligned} i_{rec,R} &= i_{LF,R} - i_{CF,RT} \\ i_{rec,S} &= i_{LF,S} - i_{CF,ST} \\ i_{rec,R} + i_{rec,S} &= I \end{aligned} \qquad (5)$$

are present simultaneously in the commutating phases *R* and *S* and/or as depicted in Fig. 6 segments of the current-time-areas $\Delta i \cdot \Delta t$ which should form the current in phase *R* do occur in phase *S*. Hence, according to (4) and (5), $i_{LF,R}$ does continuously decrease and $i_{LF,S}$ does continuously increase (cf. Fig. 6) until the end of sector 1 is reached.

After changing from sector 1 into sector 2 the switching pattern shown in Fig.4(b) is applied. There, for switching state $j = (101)$ the where phases *R* and *T* are conducting the DC link current *I* the filter capacitor voltage $u_{CF,RT}$ is decreasing while $u_{CF,ST}$ in increasing due to $i_{LF,S}$. Accordingly, $u_{CF,RS}$ goes negative and for the subsequent switching state $j = (111)$ the current flow is via phase *S* until $u_{CF,RS}$ again reaches zero and a short sliding interval does occur. This however does not significantly change the time behavior of the rectifier input currents $i_{rec,i}$ and the distortion of mains currents $i_{LF,R}$ and $i_{LF,S}$ does decay in form of a damped oscillation (damping resistors R_D).

In summary due to the capacitor voltage ripple and the continuous clamping of phase *S* in sector 1 a sliding intersection of the filter capacitor voltages does occur which results in a distortion of the mains current.

The current distortion could be reduced by increasing the capacitance of the filter capacitors or the switching frequency. However, this would result in a reduced power factor at low output power or in higher switching losses and therefore should not be considered further.

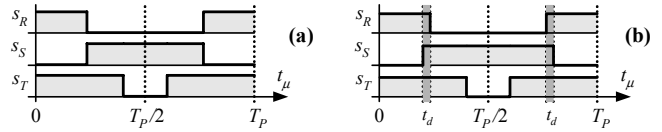

Fig. 7: Switching functions of the proposed advanced modulation scheme preventing sliding intersections of the filter capacitor voltages; assumed relations of the mains voltages according to $0 < \varphi_N < \pi/3$ (cf. also Fig. 4(a)). **(a)** ideal switching state sequence; **(b)** modified switching state sequence considering an overlapping time t_d when switching over from $j = (101)$ to $j = (011)$.

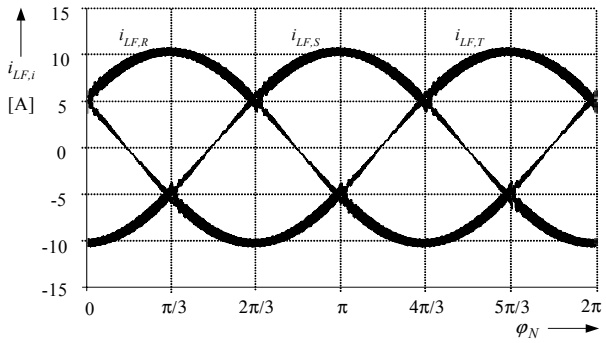

Fig.8: Time behavior of the mains phase currents when employing the proposed modulation scheme. When entering into a new sector, the changing sector information can only be considered at the beginning of a the subsequent pulse half period. Accordingly, a switching state sequence which is not in accordance with the voltage conditions does occur in principle at sector boundaries for half a pulse period. This does result in oscillations of the mains phase currents with low amplitude as can be seen from the time behavior of the phase currents.

IV. Proposed Advanced Modulation Scheme

An advanced switching state sequence preventing sliding intersection of the filter capacitor voltages is depicted in **Fig. 7**(a) for assuming $0 < \varphi_N < \pi/3$ (sector 1, all following considerations will be limited to this case). There are no intervals where all transistors are turned on, accordingly, always only two bridge legs are carrying current (with the exception of the free-wheeling state) and no distortion of the mains currents $i_{LF,i}$ does occur.

In order to maintain the minimum switching losses of the rectifier given for conventional modulation, phase *S* has to be available for current conduction when phase *R* is turned off. This is ensured by introducing an overlapping time t_d of the turn-on states of both phases which is selected with respect to gate drive and signal electronics delay times and kept to minimum in order to avoid the occurrence of sliding intervals. As for neglecting the switching frequency ripple of the filter capacitor voltages $u_{CF,RT} > u_{CF,ST}$ is valid in sector 1, there no turn-on losses of phase S do occur, and the current *I* is commutated to phase S only at the turn-off of phase R.

Furthermore, the turn-off of phase *S* is delayed by t_d with reference to the turn-on of phase *R*, therefore, phase *R* also takes over the switching losses as given for the conventional pulse width modulation.

The system behavior resulting for employing the advanced modulation scheme is shown in **Fig.8** and **Fig.9**. In contrast to conventional modulation (cf. Fig.6) no sliding intersections of the capacitor voltages $u_{CF,RT}$ and $u_{CF,ST}$ do occur, accordingly the distribution of the DC link current *I* to the phases is in correspondence with the switching pattern and/or no distortion of the mains currents at sector boundaries does occur (cf. Fig.8).

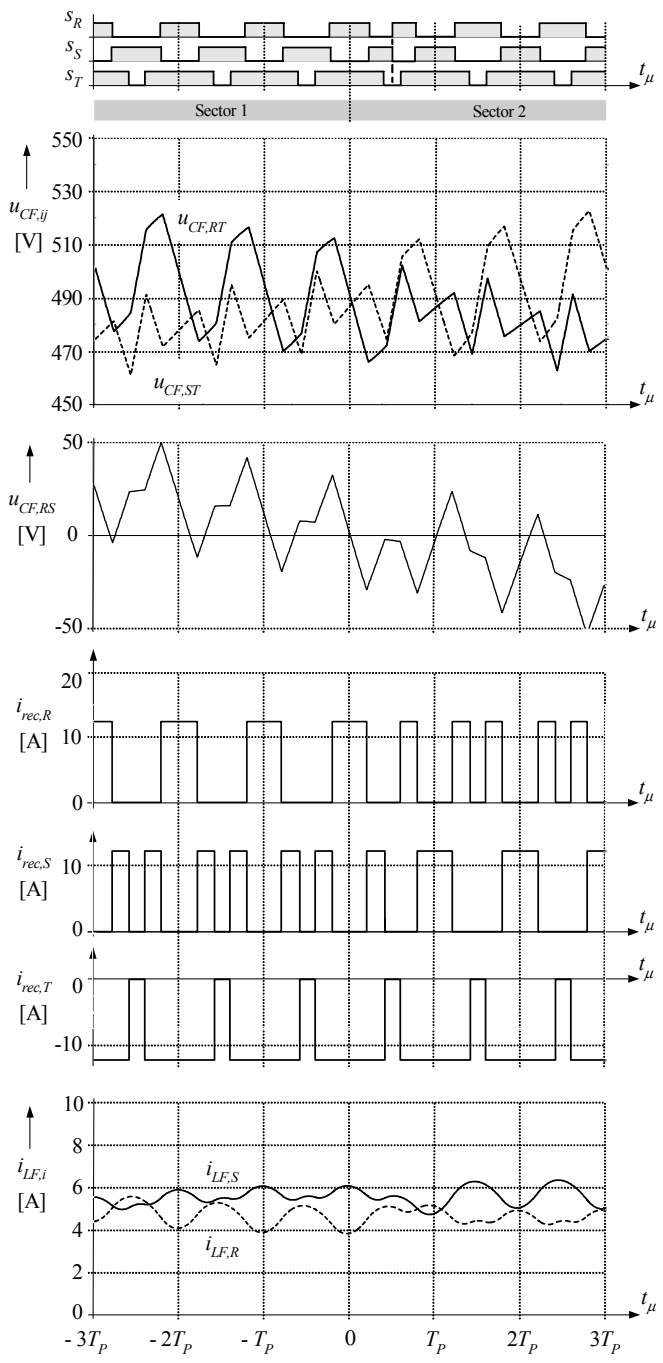

Fig. 9: Time behavior of the switching functions s_i, $i=R,S,T$, of the filter capacitor voltages $u_{CF,RT}$, $u_{CF,RT}$, and $u_{CF,RS}$, of the rectifier input currents $i_{rec,R}$, $i_{rec,S}$, and $i_{rec,T}$, and of the mains filter inductor currents $i_{LF,R}$ and $i_{LF,S}$ for the proposed modulation scheme ($t_\mu = 0$ denotes the sector change according to the inner mains voltage conditions); sliding intersections (cf. Fig. 6) of the filter capacitor voltages $u_{CF,RT}$ and $u_{CF,RT}$ are prevented as for excluding the overlapping time intervals t_d always only two bridge legs are in the on-state. **Remark:** The leading phase of the mains currents $i_{LF,i}$ with reference to the crossing of the corresponding inner mains phase voltages (end of sector 1, $t_\mu = 0$) is due to reactive current drawn by the filter capacitors $C_{F,i}$.

Finally, it shall be investigated to what extent a wrong, i.e. delayed detection of the end and/or beginning of a sector does take influence on the time behavior of the mains currents for application of the advanced PWM scheme. For considering the phase displacement caused by the voltage drop across the input filter inductor $L_{F,i}$ when entering into a new sector the sector information is updated and/or considered for the PWM with a delay of half a pulse period, i.e. $T_P/2$. As depicted in **Fig.10** there is no significant difference of the mains current time behavior between updating the sector information with a delay of $T_P/2$ or, e.g. $3½T_P$, as long as the switching pattern is changed at the end of a freewheeling state and a free-wheeling state is also placed at the beginning of the subsequent pulse half period. If the switching pattern is changed at the end of a pulse sequence and/or pulse half period where an active switching state does occur and continued in the subsequent sector with a switching state sequence showing an active state at the beginning a local distortion of the mains current does occur (cf. Fig.10). As a more detailed analysis shows this oscillation is caused by an irregular distribution of the rectifier input current pulses at the sector boundary which does result in time behavior of the filter capacitor voltage ripple showing a non-zero local average value.

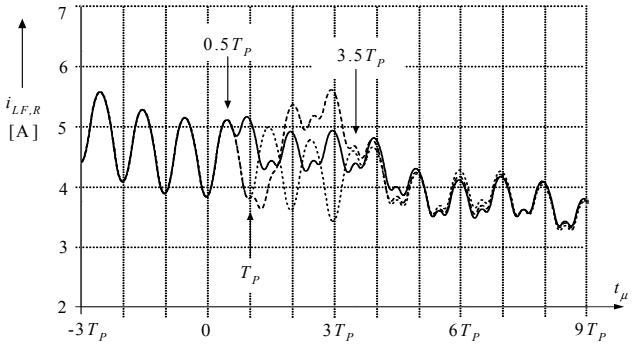

Fig.10: Time behavior of the mains phase current $i_{LF,R}$ for considering the sector information with different delay times (the sector does change according to the relation of the inner mains voltages $u_{N,i}$ at $t_\mu = 0$); **solid line**: sector information considered for the PWM with a delay of $T_P/2$ and change of the switching pattern at the end of a pulse half period where a free-wheeling state does occur; a free-wheeling state takes also place at the beginning of the following pulse half period in the subsequent sector; **dotted line**: sector information delayed by $3½T_P$ and switching pattern change again during the freewheeling state; **dashed line**: sector information delayed by T_P and switching pattern change therefore between two active states.

V. CONCLUSIONS

It has been shown that sliding intersections of the input filter capacitor voltages and/or the resulting distortion of the mains current at sector boundaries which are characteristic for PWM schemes relying on the clamping of always one phase are eliminated by the proposed modulation scheme. There, the optimum properties of conventional modulation

concerning switching losses and the switching frequency ripple of the filter capacitor voltages (excluding the immediate vicinity of sector limits) and the DC link current ripple are not impaired.

Furthermore, the proposed PWM scheme is not sensitive to a delay of the consideration of a changing sector information for the pulse pattern generation as far as the switching pattern is changed at the end of a free-wheeling state and a free-wheeling state is also placed at the beginning of the subsequent pulse half period. The proposed modulation concept is characterized by a slightly higher realization effort as compared to clamping PWM schemes as a continuous PWM has to be provided for all three phases.

The theoretical considerations given in this paper will be verified in the course of further research experimentally on a DSP controlled 5kW prototype of the PWM rectifier systems.

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