Low Cost High Power Factor Electronic Ballast with no Input Filter

*Claudinor B. Nascimento & Arnaldo José Perin
Federal University of Santa Catarina
Power Electronics Institute (INEP)
Department of Electrical Engineering
Florianópolis, Brazil

Eduardo Inácio Pereira
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronics System Laboratory (LEM)
ETH-Zentrum ETL H.14 CH-8092 Zurich
Switzerland/Europe

Abstract— A new topology of electronic ballast for fluorescent lamps employing the charge pump concept but with no LC input filter is presented in this paper. The use of magnetic coupled boost inductors together with the connection of the resonant capacitor directly at the input stage assures high power factor even with no filtering stage for the input current. Thereby, the proposed electronic ballast presents high input power factor and arises as an interesting solution for large scale production since the component count is reduced. With the operating principle and the mathematical analysis developed the unity power factor condition is obtained easily. Proving the results of the design methodology, experimental results coming from a prototype with fixed switching frequency and also with self oscillating drive technique are presented in a 2x40W electronic ballast.

I. INTRODUCTION

The advent of the high frequency electronic ballasts brought excellent results in terms of energy savings and also several advantages when compared with previous electromagnetic ballasts like light weight, reduced volume, improved efficiency and absence of audible noise and flickering. In other way, the natural solution for the input stage in electronic ballasts does not present good results on power factor correction aspects and, normally, this drawback is solved in such a way that the costs of production are raised turning the final product more expensive[1, 2].

An interesting solution to obtain a low cost power factor correction stage (PFC) is the integration of the input rectifier with the resonant inverter in a single stage [3, 4]. One of the most efficient techniques employs the charge pump concept like: voltage source - charge pump power factor correction (VS-CPPFC), current source - charge pump power factor correction (CS-CPPFC) and the continuous input current - charge pump power factor correction (CIC-CPPFC) [5-7]. Input stages with this kind of integration presents low harmonic contents at the input current and besides it, the component count is relatively low, comparing with an active PFC solution, making this circuits very attractive for large scale production.

Good results with the charge pump concept are only obtained employing a bulky and voluminous input LC filter in order to minimize the high frequency harmonics at the input current and also for electromagnetic interference (EMI) requirements.

Therefore, topologies that allow an even bigger reduction on the component count and/or in volume and mass causing low impacts on the mains side are always some steps ahead for industrial applications.

This paper presents new topologies derived from the CS-CPPFC concept but with a significant reduction on the component count, including the total absence of an input filter stage. With the electrical connection of the resonant capacitors directly at the ac side of the rectifier high power factor is obtained without employing any filtering. These capacitors together with the magnetic coupled boost inductors play the role of the traditional LC filter.

II. PROPOSED TOPOLOGIES

With no PFC circuit as shown in Fig. 01, electronic ballasts naturally presents a reduced component count and low prices compared with that ones that include the PFC stage, but the input current's harmonics exceeds the IEC 61000-3-2 for Class C lighting applications limits.

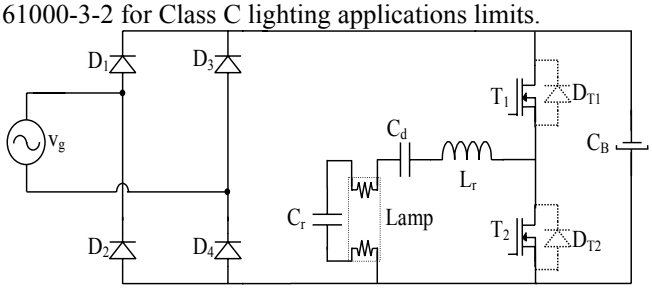


Fig. 01 – Typical electronic ballast circuit with no PFC stage.

The proposed electronic ballast also presents a reduced component count and the difference is the input power factor that is increased in order to fulfill the IEC 61000-3-2 requirements.

Fig. 02(a) shows the symmetrical CIC-CPPFC topology with the input filter L_f-C_f [5]. Splitting the "s" node in "s_1" and "s_2", allows direct connection of the resonant tank at the ac side of the boost inductors L_{in1} and L_{in2}, as shown in Fig. 02(b). These boost inductor assures symmetrical operation for the structure. In consequence, there is a direct path connecting the input voltage source and the resonant circuits of each lamp allowing C_{d1} and C_{d2} to play the same role of C_f. Fig. 02(c) shows the circuit with no C_f. Since L_{in1} and L_{in2} should be magnetically coupled the input current will not show instantaneous variations and the L_f inductor can be eliminated of the circuit, Fig. 02(d).

* Claudinor B. Nascimento is a lecturer at the Federal Center for Technological Teaching of Paraná (CEFET). He is currently working on his Ph.D. thesis at the Federal University of Santa Catarina.

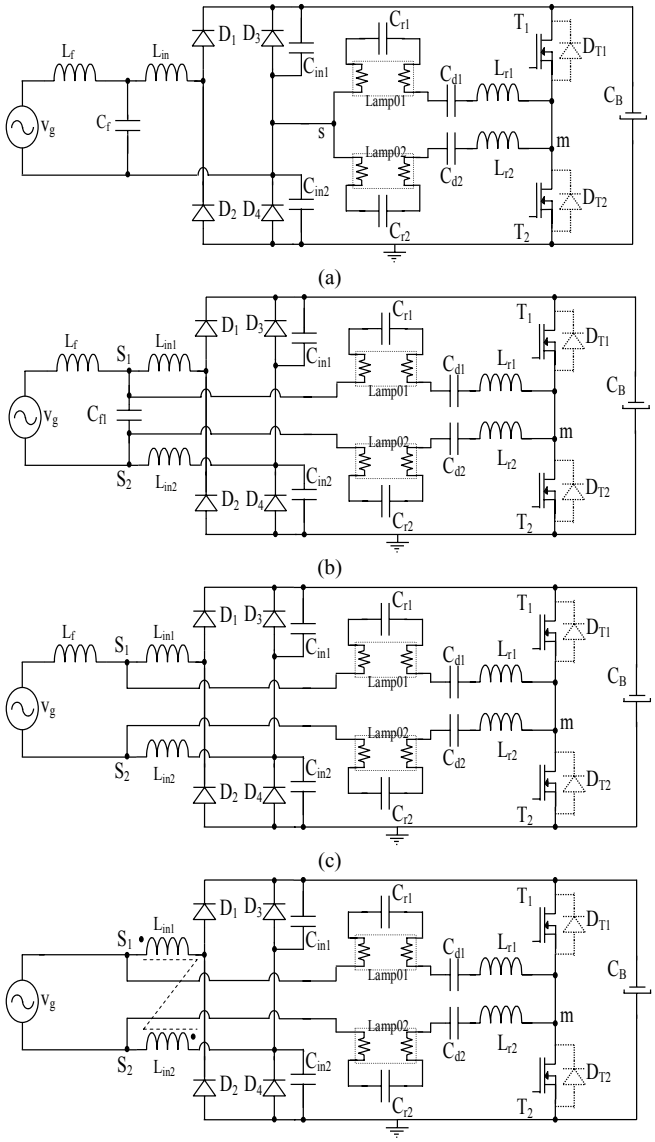


Fig. 02- (a) CIC-CPPFC electronic ballast. (b) electronic ballast with the input inductor separated in L_{in1} and L_{in2} and with resonant tanks connected to the AC side. (c) same as (b) but with no input filter capacitor C_f; (d) resulting topology with no input filter L_f.

A topological variation of the Fig. 02(d) is shown in Fig 03(a) where two input capacitors C_{f1} and C_{f2} are directly connected to the resonant circuit. Fig. 03(b) shows other variation where the capacitors C_{in1} and C_{in2} are directly connected to the resonant circuit too. Another topological variation is presented in Fig 03(c) even with only one capacitor C_{in}; this structure keeps the same characteristics of a CS-CPPFC circuit and this way, it will be analyzed in this work.

III. STEADY-STATE ANALYSIS AND DESIGN CONSIDERATIONS

A. Operating stages

The operating stages are shown for the positive half period of the mains, and the results can be extended for the negative part.

The following considerations are taken into account when analyzing the structure:

- The voltage ripple at the dc bus will be neglected;
- Since the switching frequency is much higher than the mains frequency, the input voltage will be assumed constant during a switching period;
- The resonant tank will be modeled as an ideal high frequency sinusoidal current source:
- All components will be considered to be ideal.

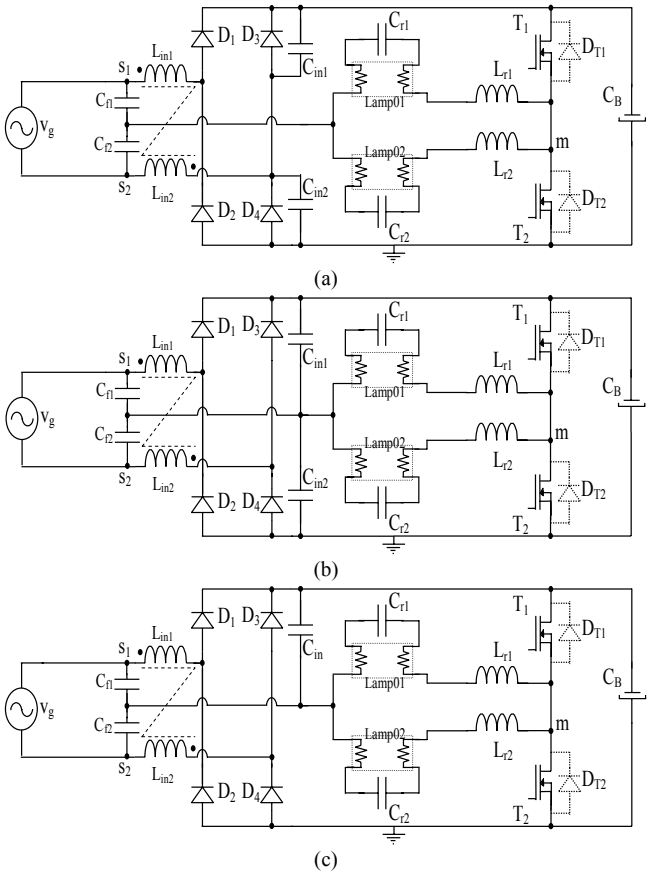


Fig. 03 – (a) Electronic ballast with 2 filtering capacitor and with no resonant capacitors, C_{d1} and C_{d2}. (b) topological variation of (a) with the input capacitor connected to the resonant tank. (c) structure with a single input capacitor.

First stage - (t_0, t_1): before t_0, D_1, and T_1 where conducting, C_{in} was discharging trough D_4 and the voltage across the inductors L_{in1} and L_{in2} was clamped at $(|v_g|-V_B)/2$. At t_0, the current on the DC link capacitor reaches zero blocking D_4 and starts the charging process of C_{in}. Considering the voltage across C_{f1} constant over a switching period a resonant stage occurs between L_{in1} and C_{in}. This stage ends at the moment that T_1 is turned off and T_2 is triggered. Fig. 04 shows this operating stage.

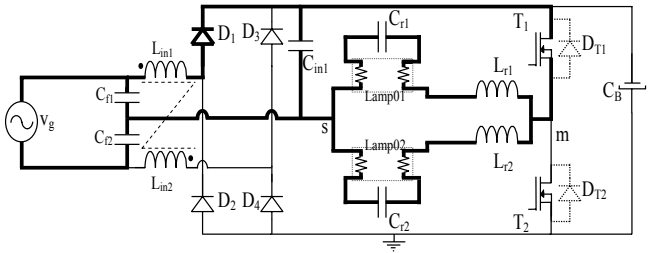


Fig. 04 – First operating stage.

Second stage – (t_1, t_2): At t_1, T_1 is turned off and D_{T2} starts conducting the sum of the current trough L_{r1} and L_{r2}. At this moment, the voltage at C_{in} reaches its lowest level ($|v_g|/2$)-V_{Lin1}. This stage is finished at t_2 when the voltage at C_{in} reaches $V_B/2$ and D_4 starts to conduct. Fig. 05 shows the circuit configuration during this stage.

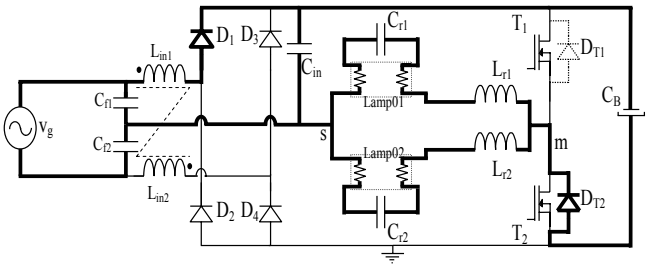


Fig. 05 - Second operating stage.

Third stage – (t_2, t_3): At t_2, D_4 starts to conduct and the voltage across C_{in} is clamped at $V_B/2$. During this time interval the current trough L_{r1} and L_{r2} reaches zero and consequently T_2 is turned on. This stage ends at t_2 when the current at L_{in1} reaches zero and D_1 is naturally blocked. The circuit for this time interval is shown at Fig.06.

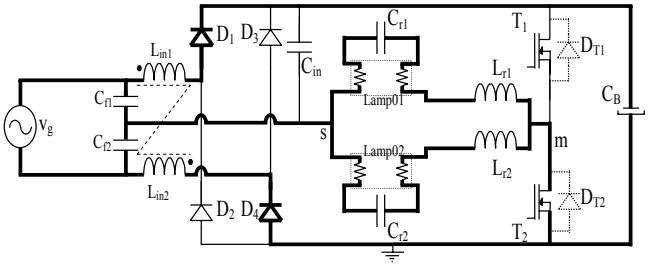


Fig. 06 - Third operating stage.

Fourth Stage – (t_3, t_4): At t_3, the current at L_{in1} is null blocking D_1 and starts the process of charging on the capacitor C_{in}. Like in the first stage, a resonant stage occurs between L_{in2} and C_{in}. This stage finishes when T_1 is triggered on and T_2 is triggered off. Fig. 07 shows this operating stage.

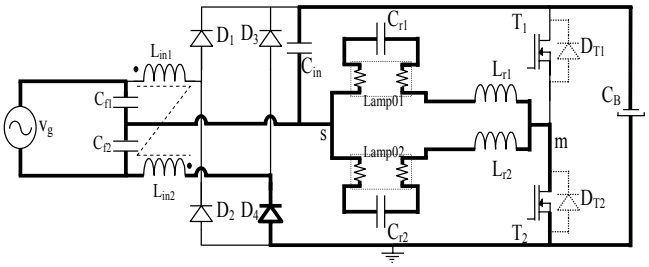


Fig. 07 - Fourth operating stage.

Fifth stage - (t_4, t_5): At t_4, T_1 is turned on and T_2 is blocked and D_{T1} starts conducting the sum of the current trough L_{r1} and L_{r2}. At this moment, the voltage at C_{in} reaches its highest level V_B+V_{Lin1}-$|v_g|/2$. This stage is finished at t_2 when the voltage at C_{in} reaches $V_B/2$ and D_1 starts to conduct. Fig. 08 shows the circuit configuration during this stage.

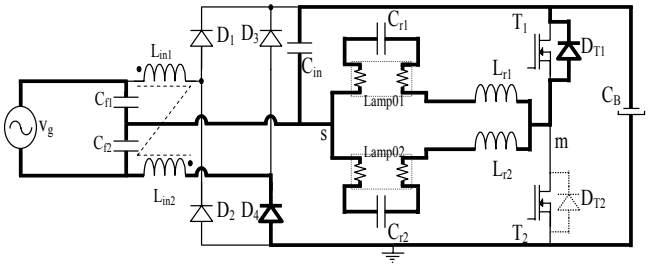


Fig. 08 - Fifth operating stage.

Sixth stage – (t_5, t_6):. At t_5, D_1 starts to conduct and the voltage across C_{in} is clamped at $V_B/2$. During this time interval the current trough L_{r1} and L_{r2} reaches zero and consequently T_1 conducts the current. This stage ends at t_2 when the current at L_{in2} reaches zero and D_4 is naturally blocked. The circuit for this time interval is shown at Fig. 09.

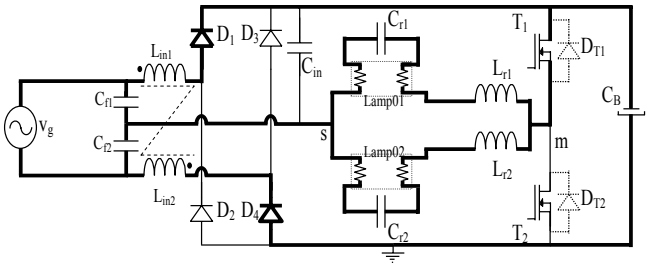


Fig. 09 - Sixth operating stage.

The time behavior of the main quantities on this analysis is presented at Fig. 10.

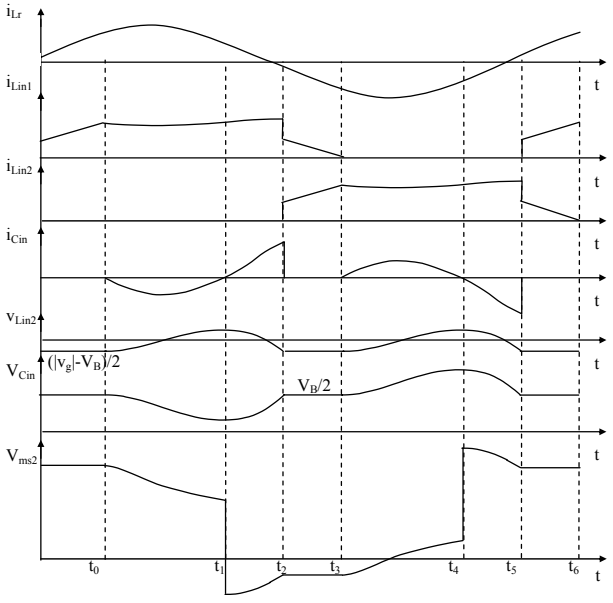


Fig. 10 – Switching waveforms.

B. Design consideration

For the mathematical modeling of the circuit proposed only the time interval t_2 - t_6 that means the period during which D_4 is conducting and there is current flow trough L_{in2}. Since the current trough L_{in2} has the same behavior the analysis developed to L_{in1} can be applied to determine the value of L_{in2}.

The following assumptions are made for the analysis:

$$v_g(t) = V_P \cdot \sin(\omega \cdot t) \quad (1)$$

$$i_{Lr}(t) = I_{Lr} \cdot \sin(\omega_r \cdot t + \theta) \quad (2)$$

$$v_{Lin1}(t) = L_{in1} \cdot \frac{di_{Lin1}(t)}{dt} \quad (3)$$

$$v_{Lin2}(t) = L_{in2} \cdot \frac{di_{Lin2}(t)}{dt} \quad (4)$$

$$i_{Cin} = C_{in} \cdot \frac{dv_{Cin}}{dt} \quad (5)$$

$$v_{Lin1}(t) = v_{Lin2}(t) \quad (6)$$

During the time interval t_2 - t_3 the following equations are valid:

The voltage across C_{in} is defined by Eq. (7).

$$v_{Cin} = -\left|v_g(t)\right| + v_{Lin2} + V_B \quad (7)$$

and

$$-\left|v_g(t)\right| + v_{Lin1} + v_{Lin2} + V_B = 0 \quad (8)$$

Applying Eq. (6) on Eq. (8) leads to:

$$-\left|v_g(t)\right| + 2 \cdot v_{Lin2} + V_B = 0 \quad (9)$$

Substituting Eq. (4) on Eq. (9) :

$$-\left|v_g(t)\right| + 2 \cdot L_{in2} \cdot \frac{di_{Lin2}(t)}{dt} + V_B = 0 \quad (10)$$

Integrating over the period:

$$\int_{i_{Lin2}(t_2)}^{i_{Lin2}(t)} di_{Lin2}(t) = \frac{\left|v_g(t)\right| - V_B}{2 \cdot L_{in2}} \cdot \int_{t_2}^{t} dt \quad (11)$$

Solving Eq. (11) gives Eq. (12) that represents the current on L_{in} within the time interval t_2 - t_3.

$$i_{Lin2}(t) = \frac{\left|v_g(t)\right| - V_B}{2 \cdot L_{in2}} \cdot \left(t - t_2\right) + i_{Lin2}(t_2) \quad (12)$$

During the time interval t_3 – t_5 the following equations are valid:

The voltage across C_{in} is defined by Eq. (13).

$$v_{Cin}(t) = v_{Lin2}(t) + V_B - v_{Cf1}(t) \quad (13)$$

Applying Eq. (4) on Eq. (13) leads to:

$$v_{Cin}(t) = L_{in2} \frac{di_{Lin2}(t)}{dt} + V_B - v_{Cf1}(t) \quad (14)$$

Derivating Eq. (14) related to time:

$$\frac{dv_{Cin}(t)}{dt} = L_{in2} \cdot \frac{d^2 i_{Lin2}(t)}{dt^2} - \frac{dv_{Cf1}(t)}{dt} \quad (15)$$

Considering the switching interval related to the mains period it correct to affirm that:

$$v_{Cf1}(t) + v_{Cf2}(t) = \left|v_g(t)\right| \quad (16)$$

That leads to:

$$\frac{dv_{Cf1}(t)}{dt} = -\frac{dv_{Cf2}(t)}{dt} \quad (17)$$

and:

$$i_{Cf1}(t) - i_{Cf2}(t) = i_{Lin2}(t) \quad (18)$$

$$i_{Lin2}(t) = C_{f1} \frac{dv_{Cf1}(t)}{dt} - C_{f2} \frac{dv_{Cf2}(t)}{dt} \quad (19)$$

It is assumed that $C_{f1} = C_{f2}$:

$$i_{Lin2}(t) = 2 \cdot C_{f1} \frac{dv_{Cf1}(t)}{dt} \quad (20)$$

or:

$$\frac{dv_{Cf1}(t)}{dt} = \frac{i_{Lin2}(t)}{2 \cdot C_{f1}} \quad (21)$$

$$i_{Cf1}(t) - i_{Cf2}(t) + i_{Cin}(t) + i_{Lr}(t) = 0 \quad (22)$$

Taking Eq. (2), Eq. (4) and Eq. (18) and applying on Eq. (22):

$$-i_{Lin2}(t) + C_{in} \cdot \frac{dv_{Cin}}{dt} = -I_{Lr} \cdot \sin(\omega_r \cdot t + \theta) \quad (23)$$

Substituting Eq. (15) on Eq. (23):

$$-i_{Lin2}(t) + C_{in} \cdot \left(L_{in2} \cdot \frac{d^2 i_{Lin2}(t)}{dt^2} - \frac{dv_{Cf1}(t)}{dt} \right) = \quad (24)$$
$$= -I_{Lr} \cdot \sin(\omega_r \cdot t + \theta)$$

Substituting Eq. (21) on Eq. (24):

$$-i_{Lin2}(t) + C_{in} \cdot \left(\frac{i_{Lin2}(t)}{2 \cdot C_{f1}} - L_{in2} \cdot \frac{d^2 i_{Lin2}(t)}{dt^2} \right) =$$
$$= -I_{Lr} \cdot \sin(\omega_r \cdot t + \theta) \quad (25)$$

Rearranging Eq. (25):

$$i_{Lin2}(t) \left(\frac{2 \cdot C_{f1} - C_{in}}{2 \cdot C_{f1}} \right) + C_{in} \cdot L_{in2} \cdot \frac{d^2 i_{Lin2}(t)}{dt^2} = \quad (26)$$
$$= I_{Lr} \cdot \sin(\omega_r \cdot t + \theta)$$

Considering $C_{f1} >> C_{in}$:

$$i_{Lin2}(t) + C_{in} \cdot L_{in2} \cdot \frac{d^2 i_{Lin1}(t)}{dt^2} = \quad (27)$$
$$= I_{Lr} \cdot \sin(\omega_r \cdot t + \theta)$$

Sonving Eq. (27) for $i_{Lin2}(t)$:

$$i_{Lin2}(t) = I_{Lr} \cdot \sin(\theta) \cdot \cos(\omega_0 \cdot t) + \left(\frac{\left|v_g(t)\right| - V_B}{2 \cdot Z_0} \right) \cdot \sin(\omega_0 \cdot t) + K \quad (28)$$

Where:

$$\omega_0 = \frac{1}{\sqrt{C_{in} \cdot L_{in2}}}, \quad C_{in} = \frac{1}{Z_0 \cdot \omega_0} \quad e \quad Z_0 = \sqrt{\frac{L_{in2}}{C_{in}}}$$

For the time interval t_5 - t_6 the same analysis can be applied resulting in:

$$i_{Lin2}(t) = \frac{\left|v_g(t)\right| - V_B}{2 \cdot L_{in2}} \cdot \left(t - t_5\right) + i_{Lin2}(t_5) \tag{29}$$

Considering the power balance between input and output the values of L_{in1} and L_{in2} can be calculated as well for the input capacitor C_{in}. To calculate the average input current, is taken the sum of the average current trough L_{in} over each time interval considered. Performing on this way the average input current, during a switching period, is expressed by:

$$I_{Lavg} = \frac{1}{T_r} \cdot \int_{t_2}^{t_3} i_L(t) \cdot dt + \frac{1}{T_r} \cdot \int_{t_3}^{t_5} i_L(t) \cdot dt + \\ + \frac{1}{T_r} \cdot \int_{t_5}^{t_6} i_L(t) \cdot dt \tag{30}$$

Considering θ = 0:

$$I_{Lavg} = \left|v_g(t)\right| \cdot \left[\frac{1 - \cos(\alpha \cdot \frac{3\pi}{4})}{4 \cdot \pi \cdot \alpha \cdot Z_0} + \frac{37 \cdot}{256 \cdot L_{in1} \cdot f_r} \right] + K \tag{31}$$

Where: $\alpha = \frac{\omega_0}{\omega_r}$ and

$$K = -V_B \cdot \left[\frac{1 - \cos(\alpha \cdot \frac{3\pi}{4})}{4 \cdot \pi \cdot \alpha \cdot Z_0} - \frac{37}{256 \cdot L_{in1} \cdot f_r} \right] + \\ + \frac{0.85}{\pi} \cdot \frac{\alpha}{\alpha + 1} \cdot I_{Lr} + \frac{7 \cdot P_0}{4 \cdot V_P} \tag{32}$$

Unity power factor can be obtained when K=0, resulting in:

$$V_B = \frac{\left[I_{Lr} \cdot \frac{2 \cdot \alpha}{0.85 \cdot (\alpha + 1)} + \frac{7 \cdot P_0}{4 \cdot V_P} \right]}{\left[\frac{1 - \cos(\alpha \cdot \frac{3\pi}{4})}{4 \cdot \pi \cdot \alpha \cdot Z_0} - \frac{37 \cdot}{256 \cdot L_{in2} \cdot f_r} \right]} \tag{33}$$

$$L_{in2} = \frac{\eta \cdot {V_P}^2}{16 \cdot P_0 \cdot \pi^2 \cdot \alpha^2 \cdot f_r} \cdot \\ \cdot \left(1 - \cos(\alpha \cdot \frac{3 \cdot \pi}{4}) + \frac{37 \cdot \pi^2 \cdot \alpha^2}{64} \right) \tag{34}$$

$$C_{in} = \frac{2 \cdot P_0}{\eta \cdot {V_P}^2 \cdot f_r} \cdot \left(\frac{1}{\left(1 - \cos(\alpha \cdot \frac{3 \cdot \pi}{4}) \right) + \frac{37 \cdot \pi^2 \cdot \alpha^2}{64}} \right) \tag{35}$$

Where: $\eta = \frac{P_0}{P_{in}}$

IV. EXPERIMENTAL RESULTS

To prove the results of the mathematical analysis of the electronic ballast, the power factor correction technique is applied to a prototype for two 40W lamps using a fixed frequency drive, as shown in Fig. 11, and to a commercial electronic ballast for two 40W lamps too using a self-oscillating drive.

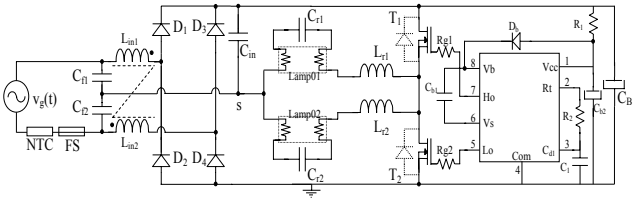


Fig. 11 - Diagram of the implemented prototype for 2x40W lamps.

A. Fixed frequency drive

From Fig. 11, it can be observed that, in the absence of the lamp, voltage surges do not occur because the inverter does not have a load, therefore, no energy is accumulated to supply bus capacitor C_B. On the other hand, if the lamp doesn't start-up or if it breaks, load will exist and the dc bus voltage will increase a lot. Therefore, it is necessary to design a circuit against voltage surges and to remove the pulses of one of the switches to avoid damage. That circuit is not presented in the paper.

The proposed methodology with a η of 85%, f_r of 28kHz, considering the design methodology of the resonant tank presented in [8] and operating with 220V rms line input the circuit result in the following circuit parameter values for a 2x40W prototype:

C_{f1}=C_{f2}=220nF C_{r1}=C_{r2}=12nF L_{r1}=L_{r2}=2.9mH
C_{in}=22nF L_{in1}=L_{in2}=2.8mH

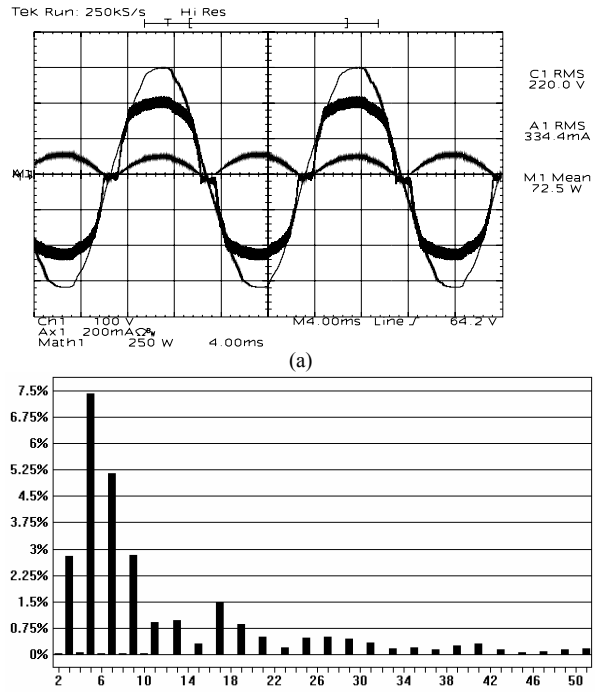
The experimental results are:

P_{in}=72.5W FP=0.985 DHT=10.1%
CF=1.47 η=91%

The measured ac input current and its harmonic spectrum are shown in Fig. 12. The line harmonic components, with a THD (Total Harmonic Distortion) of 10.1% and a 0.985 PF (Power Factor), satisfy IEC 61000-3-2 for Class C lighting applications. Fig. 13(a) shows the measured current in one of the lamps and the measured crest factor (CF) is 1.47. Fig. 13(a) present the voltage, current and power waveforms in one of the lamps. It can be observed that these currents present a rounder shape than that of a perfect sinusoid. This increases their rms value, reducing their crest factor.

Fig. 14 presents the voltage and current waveforms of one of the switches. Fig. 15 presents the voltage across one of the lamps during the start-up process.

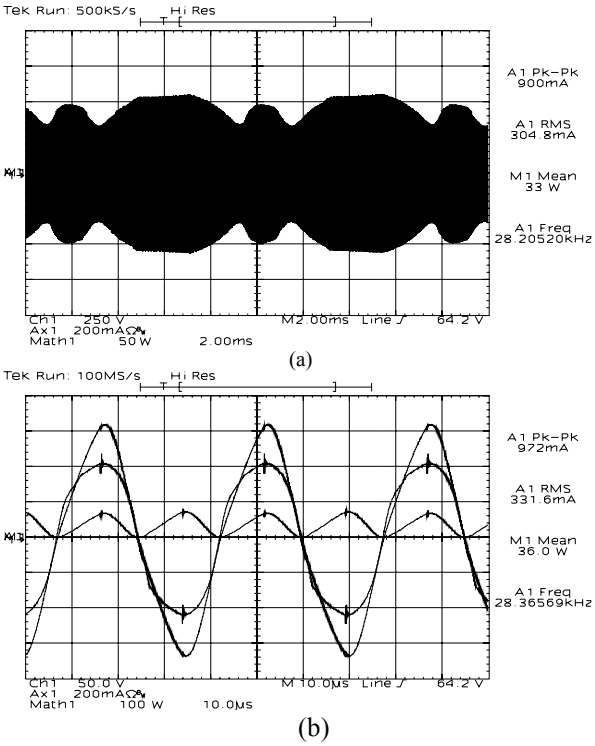
Fig. 16(a) shows the bus voltage during the start-up process and Fig. 16(b) its ripple in steady-state. Note that, after the start-up, the dc bus voltage stabilized around 430 Volts with a peak-to-peak ripple of 15 Volts. These data are very close to those obtained during the design methodology, proving the effectiveness of the presented methodology.



(a)

(b)

Fig. 12 – (a) Measured ac input current and (b) its harmonic spectrum for 2x40W lamps (c:200mA/div; v:100V/div; p:250w/div; t:4ms/div).



(a)

(b)

Fig.13 - (a) Lamp's current, CF=1.47. (i: 200ma/div; t: 2ms/div); (b) voltage and current in one of the lamps. (v: 50v/div; i: 200ma/div; p: 100w/div; t: 10µs/div).

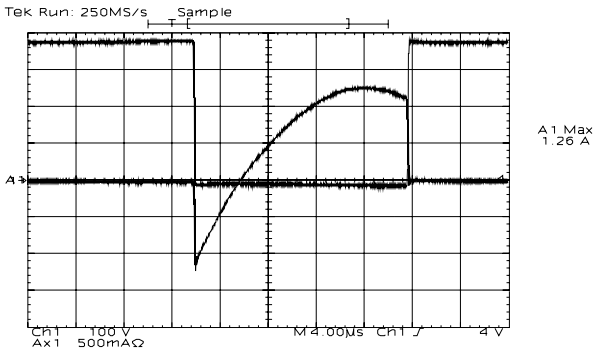


Fig. 14 – Switching voltage and current (v:100V/div; c:1A/div; t:4µs/div).

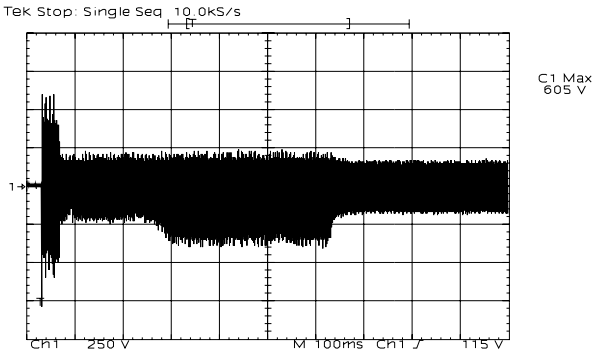
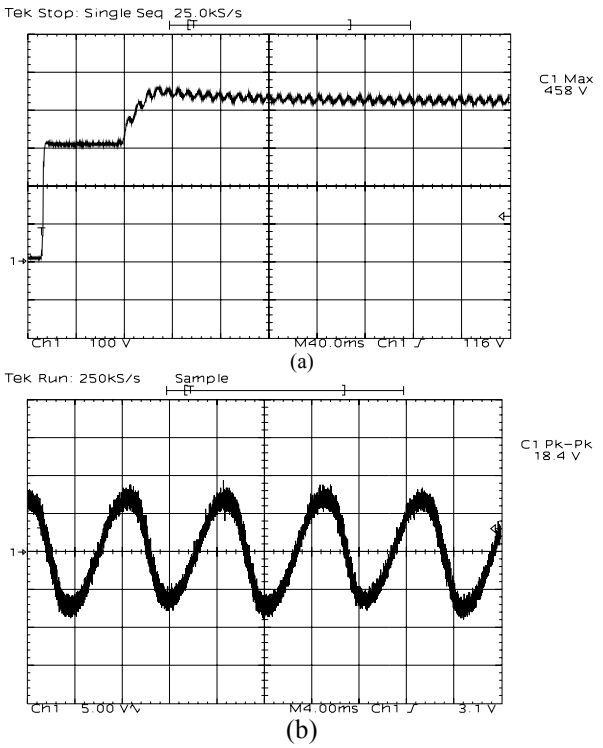


Fig. 15 – Voltage across one of the lamps during the start-up process. (v:250V/div; t:100ms/div).



(a)

(b)

Fig. 16 – (a) Dc bus voltage during the start-up process (v:100V/div; t:40ms/div) and (b) bus ripple with the PFC strategy proposed for the 2x40W (v:5V/div; t:4ms/div).

B. Self-oscillating drive

Aiming to verify the applicability of the power factor correction technique in commercial electronic ballasts, a few tests were performed on commercial ballast for two 40W lamps using a self-oscillating drive. Some bench

adjustments, such as the redefinition of the resonant tank and the substitution of the bridge rectifier's diodes, were necessary due to the operational characteristics of the proposed topology. Changing the parameters of the tank was achieved by using the methodology presented in [8]. The bridge rectifier's diodes operate at the switching frequency, so they were substituted for fast diodes.

The results showed that there isn't any restriction in applying the self-oscillating drive using the proposed technique. The measured efficiency is about 93% with an ac input current THD of 10.2%.

The measured ac input current is shown in Fig. 17. The harmonic components satisfy IEC 61000-3-2 for Class C applications. Fig. 18 presents the measured lamp current. The measured crest factor is about 1.63.

Fig. 19 shows the bus voltage during the start-up process and Fig. 13 presents the voltage across one of the lamps during the same process.

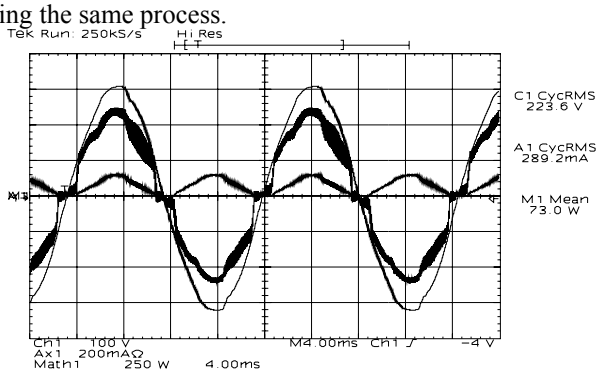


Fig. 17 – Input waveforms for the 2x40W commercial ballast with the proposed PFC circuit (c:100mA/div; v:100V/div; t:5ms/div).

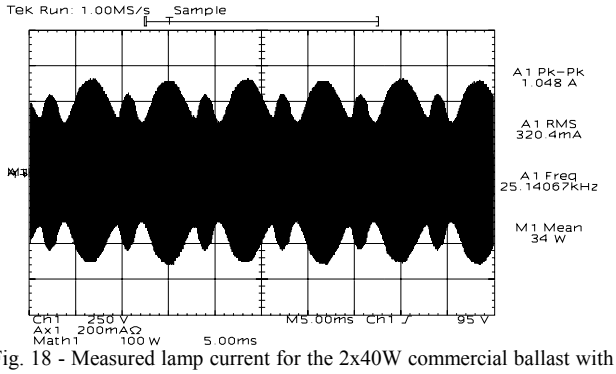


Fig. 18 - Measured lamp current for the 2x40W commercial ballast with crest factor of 1.63 (c:200mA/div; t:5ms/div)

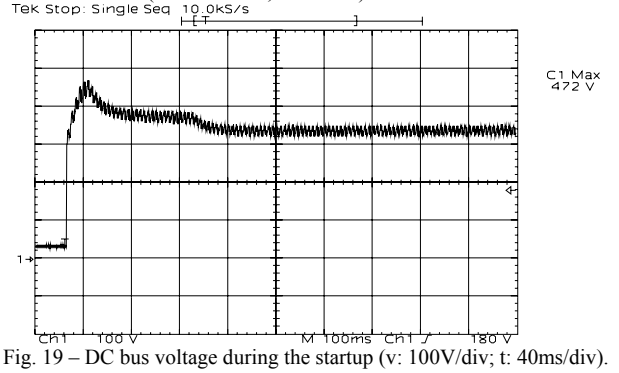


Fig. 19 – DC bus voltage during the startup (v: 100V/div; t: 40ms/div).

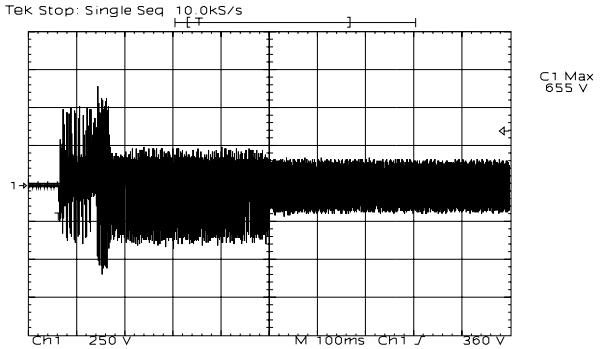


Fig.20 – Lamp voltage during the startup. (v:250V/div; t:100ms/div).

V. CONCLUSION

The experimental results obtained could validate the mathematical analysis and the design methodology.

The proposed topology has basically the same features of the CS-CPPFC structure but the absence of the input filter and the reduction on the volume of the input inductors L_{in1} and L_{in2} reduces the component count. Since the self-oscillating drive technique can be applied without any restriction in the proposed topology, this ballast became attractive for a possible commercial application due to its simplicity and low cost.

REFERENCES

[1] Hammer, E. E., "High Frequency Characteristics of Fluorescent Lamps up to 500 kHz", *Journal of the Illuminating Engineering Society*, 1987, pp. 52 - 61.

[2] Hammer, E. E., McGowan, T. K., "Characteristics of Various F40 Fluorescent Systems at 60 Hz and High Frequency", IEEE Transactions on Industry Applications, Vol. 21, No. 1, 1985, pp. 11 - 16.

[3] Alves, J. A., Perin, A. J., Barbi, I., "An Electronic Ballast with High Power Factor for Compact Fluorescent Lamp", *IEEE Industry Application Society – Annual Meeting*, 1996, pp. 2129 – 2135.

[4] Blanco, C., Alonso, M., Lopez, e., Calleja, A., Rico, M., "A single stage fluorescent lamp ballast with high power factor", *IEEE Applied Power Electronics Conf.*,1996, pp. 616 - 621

[5] Pereira, E. I., Perin, A. J., Nascimento, C. B., "Electronic ballast for fluorescent lamps with the PFC stage integrated with the resonant inverter", *Annual IEEE Power Electronics Specialists Conference*,2004, p.4050 – 4056.

[6] Pereira, E. I., Perin, A. J.," Electronic Ballast for Fluorescent lamps with the PFC Stage Integrated to the Resonant Inverter", *The 7th Brazilian Power Electronics Conference*, 2003, pp. 392 - 397.

[7] Qian, J., Lee, F. C. (1997), "A new continuous input current charge pump power f*actor correction (CIC-CPPFC) electronic ballast", IEEE Industry Application Society – Annual Meeting*, 1997, pp. 2299 – 2306.

[8] Qian, J., Lee, F. C., "Charge Pump Power - Factor - Correction Technologies Part II: Ballast Applications", *IEEE Transactions on Power Electronics*, vo. 15, no. 1, 2000, pp. 130 - 139.