# A SiC JFET Driver for a 5 kW, 150 kHz Three-Phase Sinusoidal-Input, Sinusoidal-Output PWM Converter

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***Abstract*— Silicon carbide (SiC) power semiconductor devices are capable of being operated at higher voltages, frequencies and temperatures than silicon power devices. These SiC device capabilities will provide the power electronics designer with new possibilities to produce compact designs. Presently the JFET is the only controlled turn off/on SiC device that is close to commercialization and available as restricted samples. However the JFET is a normally-on device that requires a negative gate voltage to turn off. In order to correctly design a gate driver one must understand the characteristics of the JFET. This paper presents a description of the JFET semiconductor structure, and the SiC JFET's static and dynamic characteristics from room temperature to 200°C. A SiC JFET gate driver circuit is presented and its performance described. The proposed gate driver improves the switching performance of the JFET by operating the gate in avalanche during the off time.**

***Keywords- Silicon carbide; JFET; gate driver, high-temperature operation, static characteristic, dynamic characteristic***

## I. INTRODUCTION

To design converters with ever increasing power densities, the converters should be operated at higher switching frequencies and/or temperatures. At higher frequencies the volume of the magnetic components reduces, however, in order to maintain a high efficiency particular attention must be paid to the switching losses of the semiconductor devices. For high frequency operation above 100 kHz, the silicon (Si) MOSFET has been the device of choice but they are limited in voltage rating (above 600V) and operating temperature range. For higher voltage and temperature applications, research indicates that power electronic components constructed from silicon carbide (SiC) have great potential [1][2]. The SiC power semiconductors are characterized by outstanding performance concerning their voltage blocking capability, on-state voltage drop, switching speed, and thermal resistance [3]. The conduction and switching losses could be reduced by a factor of 10 compared to Si devices and the device operating temperature could be significantly increased. Accordingly, future SiC devices should allow the realization of highly compact converter systems with lower switching and conduction losses. Furthermore, due to the wide band gap the SiC devices are suitable for high voltage applications. SiC Schottky-diodes are already commercially available [2][4] and SiC turn-off power semiconductors are currently under development [1]. The SiC JFET (Junction Field Effect Transistor) is the only controlled turn off/on SiC device that is close to commercialization and is available as restricted samples, which are packaged either as an individual device or as a cascode device.

The cascode device comprises of a SiC JFET and a series connected low voltage Si MOSFET as shown in Fig. 1 [5]. The SiC JFET can be turned on and off by using the gate of the Si MOSFET [1]. The main reason for the cascode arrangement is that the normally-on JFET, which requires a negative gate-source voltage for turn off, now becomes a normally-off device that has a behavior that is very similar conventional MOSFET [1]. The forward characteristic is determined by the level of applied gate-source voltage and is very similar to that of a comparable MOSFET. In the off-state the cascode exhibits a rugged avalanche behavior. In the on-state there are good short circuit properties because the JFET on-resistance increases with temperature and protects the device from overload. Since SiC has a higher operating temperature capability the SiC the device can dissipate more power and therefore the time to turn-off the device under these conditions is in the order of milliseconds and not microseconds as is with Si power devices [1].

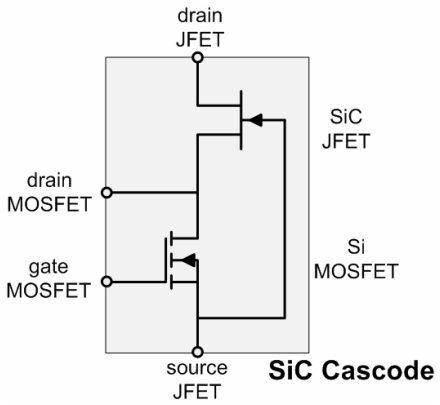



Figure 1. SiC JFET/Si low voltage MOSFET cascode

However, there are several limitations with the cascode device, such as the maximum operating temperature of the cascode is limited by the Si-MOSFET, and the conduction losses increase as two devices are connected in series. Therefore to fully utilize the potential of the SiC JFET it is desirable to use the JFET as a separate device rather than in the cascode configuration. A specialized gate driver is required to match the SiC JFET's gate to source characteristic, to be able to provide the required current drive capability and achieve high speed switching. For standard Si MOSFETs and IGBTs a commercial gate driver can be used as these devices'

characteristics are well known. However for the SiC JFET a modified driver must be used since it is a normally-on device that typically requires a large negative bias to turn off. SiC JFET gate drivers have been previously presented [5]-[7], although in [5] this gate driver was not designed for production purposes and could not easily cope with the variable device-to-device JFET characteristics. An improved gate driver was reported in [7] that could cope with the varying JFET characteristics but reported only a 9% reduction in switching loss compared to using a SiC cascode with a standard gate driver. In order to design the gate driver and a converter bridge leg the SiC JFET characteristics need to be fully determined. An optimized gate driver for SiC JFETs is presented in this paper that provides superior performance and is constructed using a minimal number of components.

In Section II, the semiconductor structure of the SiC JFET and the temperature dependent static and dynamic characteristics are presented. Section III presents the gate driver design, operation and switching performance of a SiC JFET from room temperature to 200°C.

## II. SiC JFET

SiC device technology is maturing, and SiC Schottky diodes are commercially available with a relatively low current rating, although the devices are easily paralleled. As is presented in the literature the SiC diode, both the Schottky and PiN, have significant less reverse current than that of a conventional fast or ultra-fast Si diode [8]. This is attractive for high speed operation. SiC Schottky diodes have been compared in an application such as a three-phase motor drive and found to have significantly less energy loss, especially at higher temperatures [9].

The more interesting devices are the controlled turn on and off devices. There is much research effort going into SiC MOSFET and BJT devices however there are technical difficulties that must be overcome. One controlled device that can be manufactured today in small quantities is the SiC JFET. The JFET is a majority carrier device that has a normally on characteristic. Experimental n-type JFETs with a high voltage rating of 3.5kV have been constructed [10] and they require a negative bias applied to the gate to pinch off the channel. The pinch off voltage level is determined from the design of the channel [11].

As of May 2005 information on commercially developed SiC JFETs is available from only two companies. SemiSouth Laboratories [12] have a 600V, 2A SiC JFET that has enhancement mode functionality [13]. A positive gate-to-source voltage of 3V is required to fully turn the device on and a reverse voltage of -5V is required to fully block the rated reverse voltage of 600V. SemiSouth presently has no SiC JFETs available for external evaluation. The other company, SiCED [4], is producing SiC JFETs and these are available as restricted samples. Therefore the SiCED SiC JFETs are characterized and used in the testing of the gate driver circuit.

### A. JFET structure

Two JFET structures (Fig. 2) have been proposed by SiCED [10]; structure (a) has a lower on-resistance but slower switching, while structure (b) has fasting switching but a higher on-resistance. Both structures are fabricated on a 4H-SiC substrate, are doped as n-type JFETs and have a buried p-layer. Structure (a) has a buried gate that acts as the controlling electrode while structure (b) has an upper p-layer that acts as a gate. Structure (a) has a lower on-resistance since the current flows directly from the source through the channel to the drift region. However for structure (a) the surface area of the gate above the drain is large and this results in a large gate-to-drain (Miller) capacitance. With this structure the gate resistance is dependent on the conductivity of the p-type material, which is low for SiC. This means the gate resistance is high and this reduces the switching speed of the JFET. In contrast structure (b) allows ohmic contacts to all the p-regions and this results in a lower gate resistance connection. For structure (b) the direct gate to drain area is smaller and therefore the Miller capacitance is smaller, and as a result structure (b) has a faster switching speed. However the disadvantage with this structure is that a pre-channel region between the source and channel is required to block the gate-source pinch off voltage. This results in a channel that has a higher on-resistance. For example, an 1800V JFET of structure (a) has an on-resistance of $14m\Omega cm^2$ compared to $24m\Omega cm^2$ for a structure (b) device [10]. The choice between the two structures is a trade-off between switching speed and on-resistance, and since for high frequency converters the switching loss is a dominant loss, structure (b) is used to fabricate the JFET used in the cascode device [11].

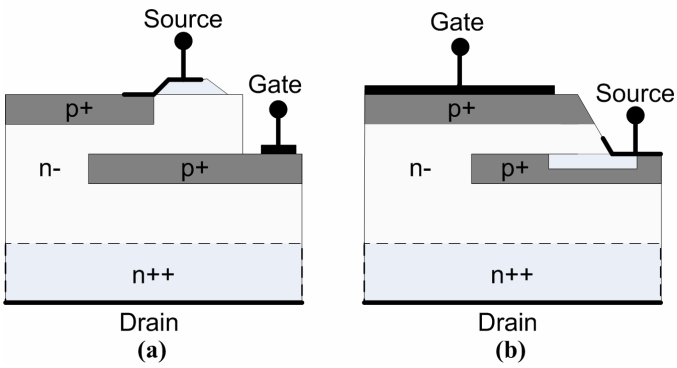



Figure 2. Two different structures of the 4H-SiC vertical JFET [7] (a) low on-resistance structure (b) fast switching structure.

### B. JFET characteristic

The SiC JFET is available as a cascode sample with a rating of 1300V and 4A [11] although individual JFETs in a TO-220 package have recently become available. The measured results presented in this paper are for the 1300V, 4A TO-220 packaged device unless otherwise stated.

The typical characteristics of the gate current, $I_g$, versus the gate voltage referenced to the source, $V_{gs}$, of a SiC-JFET for temperatures of 25°C, 125°C and 200°C are shown in Fig. 3. Measurements for 10 JFETs were taken and the characteristics of the two devices presented in Fig. 3 represent the minimum and maximum characteristics of the devices measured. Since the SiC-JFET is normally-on device, a negative gate voltage is required to turn the device off. As can be seen in Fig. 3 the pinch-off voltage, $V_p$, is device and temperature dependent. For

one device (labeled as #5) the $V_p$ is -22V at 200°C and for another device (#9) as high as −31V at 25°C. Considering the variation of the pinch-off voltage with junction temperature and the influence of highly dynamic changes of the drain-source voltage on the gate voltage by the Miller capacitance, a larger negative voltage should be applied to guarantee the JFET is in an off-state. This is complicated by the fact that the breakdown voltage of the gate-source junction also varies with each device. From the JFET measurements in Fig. 3 the gate breakdown (avalanche) voltage varies from -25V to -35V. The breakdown voltage of device #5 is more positive than the pinch off voltage of device #9. Therefore the gate driver must be designed to operate the JFET gate in avalanche without damage, while coping with the large variability in the gate characteristic.

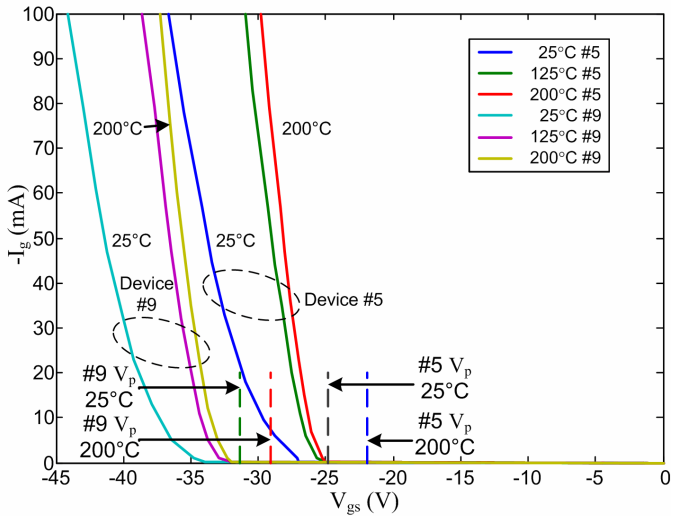



Figure 3. Reverse gate breakdown and pinch-off voltages of two JFET samples (#5 and #9) at *Tcase=25°C, 125°C* and *200°C*

The gate of the JFET is connected to a p-type region that forms a p-n diode to the channel. The forward gate characteristic for the SiC JFET has been experimentally measured for three different case temperatures and is presented in Fig. 4. As the case temperature increases the threshold voltage decreases and at 125°C the threshold voltage is 2.4V. Therefore the gate driver should not apply more than 2V to the gate without some form of gate current limiting.

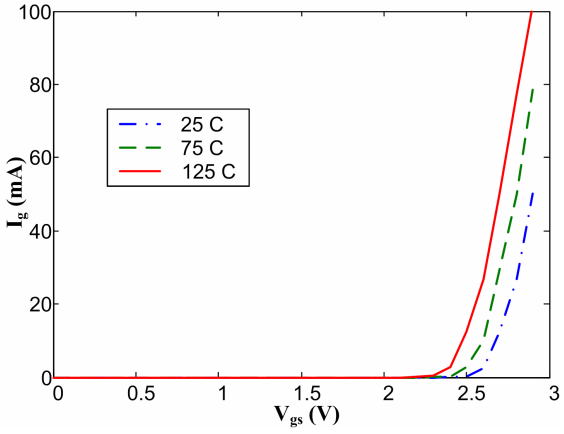



Figure 4. Forward gate characteristic at *Tcase=25°C, 75°C* and *125°C*

To determine the amount of gate charge required to switch off the JFET a special gate circuit that sets the gate current to a constant 1mA is used and the gate voltage is driven to just before breakdown. This circuit results in a slow switching transition of about 6-10µs. Fig. 5 shows that approximately 12nC of charge is required to be supplied by the gate in order to turn-off the SiC JFET at 450V. Therefore the SiC JFET has low gate capacitance compared with a high voltage MOSFET, thus the current drive requirement of the gate driver is reduced and faster switching times should result.

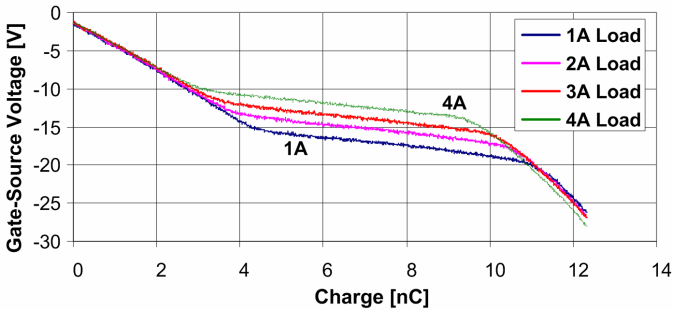



Figure 5. Gate charge requirement for turn-off of a SiC JFET at $V_{ds}$=450V and for $I_d$=2A.

For a JFET it is assumed that full conduction occurs with a zero gate to source voltage. Since the SiC JFET gate has a higher forward threshold than Si devices a positive bias, less than the threshold voltage, can be applied. A positive voltage reduces the width of depletion region at the gate p-n junction and this results in a slightly wider channel for the current to flow, which decreases the on-state resistance. It is important that the positive gate is kept below the threshold voltage for all operating conditions in order not to forward bias and destroy the gate junction. The reduction in on-state resistance for positive gate voltages has been experimentally measured for three case temperatures. The maximum applied gate-to-source voltage is +2V to ensure it is below the threshold voltage for all operating temperatures. By applying 2V to the gate the on-resistance is reduced by approximately 4% at all temperatures, which would result in a 4% reduction in the device's conduction losses. The disadvantage of a positive gate voltage is that the gate drive power supply now must produce both a positive and negative supply and therefore a compromise has to be made between additional gate drive complexity against lower losses.

Fig 6 shows the variation in the on-resistance, $R_{ds}$, for varying gate voltage, $V_{gs}$. At 25°C the measured cascode JFET resistance is 0.47Ω with $V_{gs}$ = 0V and increases to 1.47Ω at 200°C. The on-resistance of the device at 25°C increases by 24% over the gate voltage range of 0V to -10V compared with 30% for 200°C operation. The resistance increases dramatically for 25°C operation as the channel is blocked near the pinch off voltage. At an elevated temperature of 200°C the change in on-resistance is not as sudden.

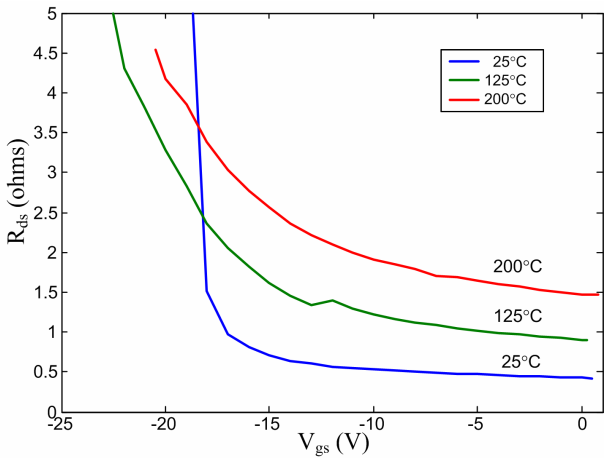



Figure 6. SiC JFET cascode device on-resistance from pinch off to 0.5V and case temperatures of *25°C,125°C* and *200°C*.

The output transfer characteristic of a SiC JFET is shown in Fig. 7 for gate-to-source voltages of 0V and 2V. The JFET exhibits ohmic behavior up until 2 to 3 times its nominal current rating. Above that current level the channel between the drain and source begins to narrow because of the increased voltage drop in the channel causes the depletion region to enlarge. Therefore the JFET has a self-limiting maximum current level that is dependent on the gate voltage and junction temperature. It can be seen that the channel resistance is higher for higher operating temperatures and this characteristic allows parallel connected JFETs to automatically share current. For a positive gate voltage of 2V the saturation current at 25°C is increased by 30% compared to the case of $V_{gs}$ = 0V.

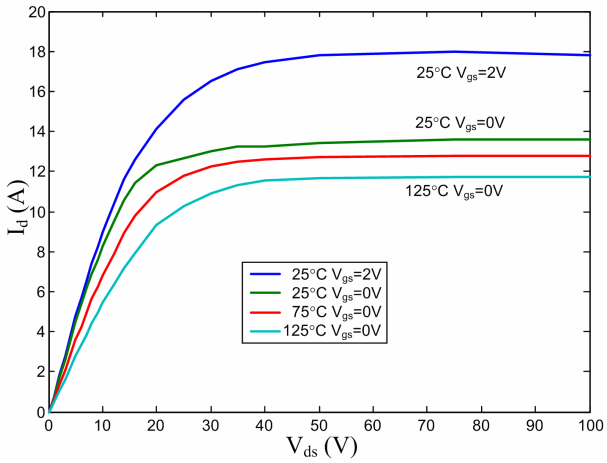



Figure 7. Output transfer characteristic of SiC JFET (TO-220) for various tempatures and gate voltages

## III. SiC JFET Gate Driver

From the JFET measurements the pinch-off voltage is in the range of -22V to -32 V and in order to avoid a turn on due to dv/dt, temperature drift, or different sample characteristics an even lower voltage should be applied. The limiting factor for this voltage level is the gate-source avalanche voltage, which is approximately -35 V for this technology but varies between samples. Thus for the turn-off of the JFET, the gate driver circuit has to apply a gate source voltage lower than the pinch-off voltage within very short time and it should also be capable of limiting the gate rms current in case a gate junction avalanche does occur.

A gate driver based on a commercial gate driver IC has been proposed in [6] to switch SiC JFETs at 250 kHz. The off voltage was set at -30V since it was found that the pinch-off voltage for most samples tested was -20V. This gate driver design will not limit the gate current to a low level under a gate avalanche condition and would likely destroy the device. Another gate driver incorporating avalanche current limiting is proposed in [7] and the authors compare the resulting JFET switching losses to the cascode driven by a MOSFET driver circuit. It was found that for the JFET only device the switching losses were reduced by 9% compared to the cascode. Another gate driver concept is proposed in [14] where the authors use a conventional opto-gate driver IC (HCNW3120) together with a DC offset for the gate driver. During turn-on the gate driver forces the gate voltage to be -9V, which is the offset voltage. The authors claim that the increase in the on-resistance and conduction losses at a -9V gate voltage is not significant. For turn off the driver produces -22V, resulting in a differential voltage of 13V that is well inside the gate driver ratings. This gate driver design will also not limit the gate current to a low level under a gate avalanche condition and would also likely destroy the device. The gate driver presented in this paper is designed to limit the gate current under avalanche conditions and to drive the JFET to achieve reduced switching losses.

### *A. Gate driver operation*

The basic idea of the proposed driver is to create a circuit that adapts to the different JFET gate characteristics. The simplified circuit (Fig. 7) is composed a commercial opto-gate driver (HCNW3120, the same device as used in [14] although any suitable isolated buffer can be used), a series gate resistance, $R_s$, and a parallel connection of a capacitor C, diode D and resistance $R_p$. The output of the parallel combination is directly connected to the gate of the JFET and the source of the JFET is connected directly to the positive supply pin of the gate driver IC. The negative supply, $V_s$, of the gate driver is -35V, which is the absolute maximum specified operating voltage of the device. Therefore the commercial use of this gate driver would not be satisfactory and a custom designed version would have to be produced. The output voltage, $v_g$, of the gate driver therefore swings between 0V and -35V. This voltage level is less than the maximum pinch-off voltage of any device to be driven. However this means that this voltage level could cause a gate avalanche condition for a JFET with a more positive avalanche (breakdown) voltage. In order to limit an uncontrolled avalanche current the parallel circuit $R_S$, $C_G$ and $D_{on}$ is placed in series with the JFET gate. This parallel combination creates an impedance that is capable of limiting the avalanche current and at the same time capable of supplying the high gate current peaks necessary for fast turn-on and turn-off. The resistor, $R_p$, is of a high value (12kΩ) and ensures that a small current flows during the JFET's off interval. The capacitor, C, is dimensioned to be large enough in order to provide the desired transient current peaks.

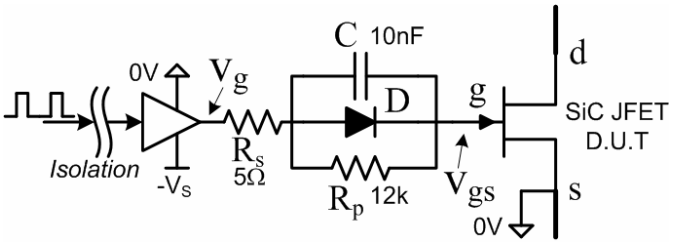



Figure 8. Proposed SiC J-FET gate drive circuit.

The simplified operating behavior of the gate drive circuit is described using the waveforms depicted in Fig. 9. These waveforms are derived using the assumption that the JFET gate-to-source junction is modeled as two anti-parallel diodes, one with a forward threshold of 2.5V and the other a forward threshold of 30V for current flow in the opposite direction.

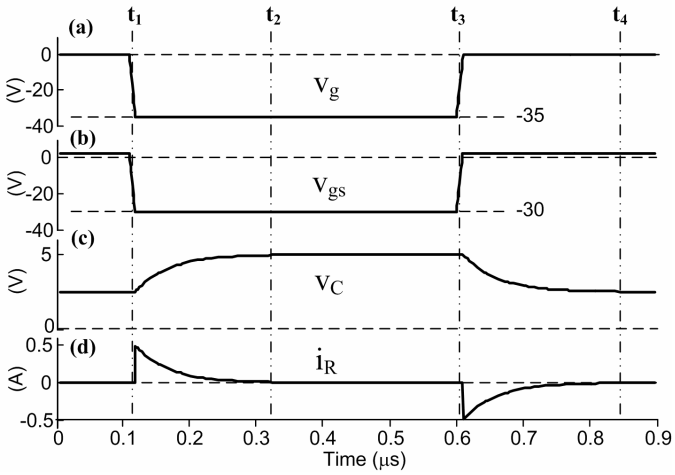



Figure 9. Time behavior of characteristic quantities of the proposed driver circuit.

**Time $t_1$:** For the time before $t_1$ it is assumed that the isolation buffer voltage $v_g$ is 0V and the JFET is conducting current. At $t_1$ the isolation buffer now outputs -35V and this causes the gate-to-source junction of the JFET to become reverse biased at -30V as set by the gate junction avalanche voltage. The series capacitor, C, is now charged to the voltage difference between the breakdown voltage and the gate driver voltage, in this case 5V. The time constant for charging the capacitor is given by $R_sC$. At time $t_2$ the capacitor is fully charged to 5V and the current flowing through the gate is limited by $R_p$ to less than 0.5mA.

**Time $t_3$:** Prior to $t_3$ the JFET has been off. At $t_3$ the voltage $v_g$ changes from -35V to 0V. At that instant the gate voltage $v_{gs}$ is increased to 5V since the voltage on the capacitor does not instantaneously change. However above 2.5V the JFET gate becomes forward biased and $v_{gs}$ is then clamped to 2.5V. The peak current into the gate is limited by the series resistor $R_s$, the initial capacitor voltage, and forward gate voltage. In this case the current is limited to 0.5A. The forward biasing of the gate junction helps improve the turn on time of the JFET due to the lower channel resistance. The capacitor voltage now discharges with a time constant of $R_sC$. At time $t_4$ the capacitor current has decreased to near zero. The switching cycle can now be repeated.

*B. SiC JFET Switching Performance*

The switching action of the SiC JFET (1300V, 4A, TO-220 package) and proposed gate driver is tested in a single switch inductive test circuit as shown in Fig. 10. A $600V_{DC}$ voltage is supplied to an inductor of 700μH and a freewheeling SiC Schottky (CREE CSD05120 5A, 1200V) diode. The SiC JFET is switched for a short time such that a continuous current is flowing in the inductive load. The turn on and off switching performance is measured using a custom designed AC current sensor placed on the drain leg of the JFET and from the JFET drain-to-source voltage. The temperature of the JFET and diode case is increased from 25°C to 200°C for the measurements. The JFET used in the tests has a gate breakdown voltage of -29V and a pinch off voltage of -20V. For each operating temperature two switching tests are performed, one with a gate driver voltage of -25V, which means the gate-to-source junction is not operating under avalanche; and secondly with a voltage of -35V that causes the gate junction to operate under the avalanche and forward bias.

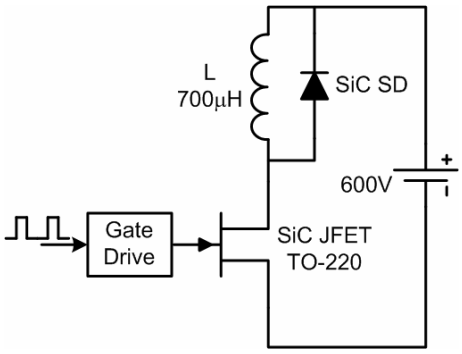
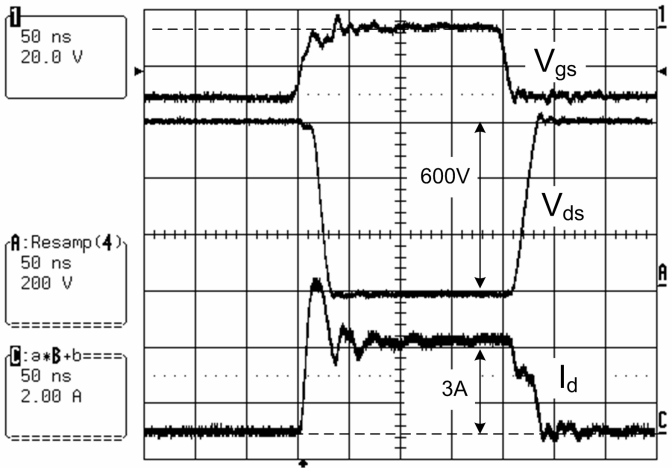


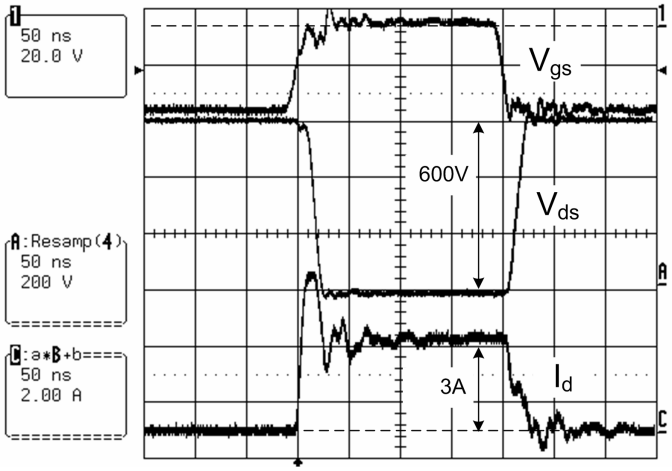

Figure 10. Single switch SiC JFET inductive switching test circuit

Fig. 11(a) and (b) shows the turn on and off behavior for the SiC JFET operating with a case temperature of 25°C for both non-avalanche and avalanche gate modes respectively. Figure 11(a) shows the turn–on and off behavior of the JFET when a load current of 3A is switched. The delay time is very small (6ns) and the drain current rises quickly to the load current value in 6ns. It can be seen that there is an additional current peak in the JFET caused by a reverse SiC diode current that is necessary to re-establish the space-charge region in the diode. The time taken for the drain-to-source voltage to decrease to near zero is 25ns. This time accounts for most of the turn-on losses generated in the JFET. For the JFET turn-off the delay is slightly longer at 9ns and the current in the drain takes longer to decrease, with a time of 30ns. Again the turn-off losses are associated with this current fall time. It can be seen that there is virtually no overshoot in the drain-to-source voltage.

In Fig. 11(b) the switching waveforms are for the same device and operating temperature, but in this case the gate driver voltage has been increased to -35V and the gate now operates in avalanche during the off period and in forward conduction during the device's on-time. The turn-on and off delay times are now increased and are 8ns and 11ns respectively. This delay is caused by the extra time needed to reach the pinch off voltage level from the new on and off gate voltage levels. Since the operation in avalanche charges the

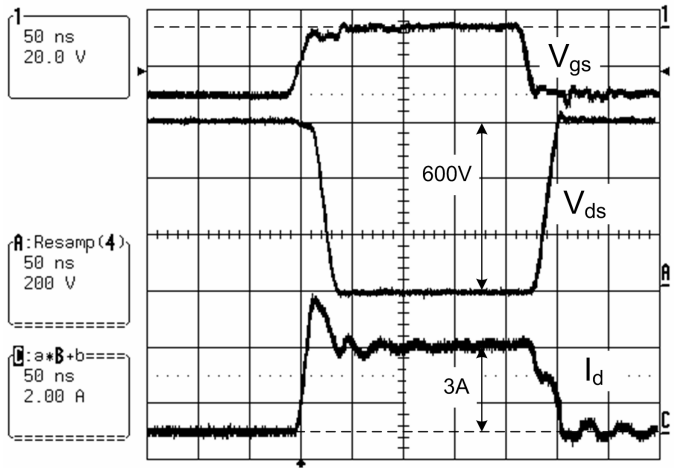



(a) Time 50ns/div, $I_d$ 2A/div, $V_{ds}$ 200V/div, $V_{as}$ 20V/div

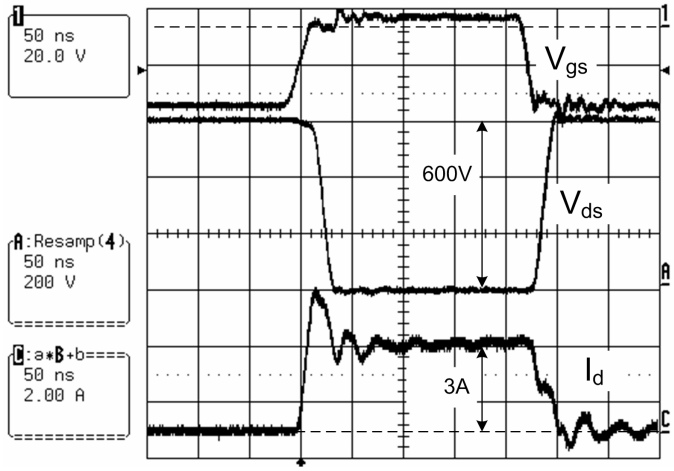



(b) Time 50ns/div, $I_d$ 2A/div, $V_{ds}$ 200V/div, $V_{gs}$ 20V/div

Figure 11. Switching waveforms of the SiC JFET at 25°C for
(a) no gate avalanche and no forward bias
(b) gate avalanche and forward bias.




(a) Time 50ns/div, $I_d$ 2A/div, $V_{ds}$ 200V/div, $V_{as}$ 20V/div




(b) Time 50ns/div, $I_d$ 2A/div, $V_{ds}$ 200V/div, $V_{gs}$ 20V/div

Figure 12. Switching waveforms of the SiC JFET at 200°C for
(a) no gate avalanche and no forward bias
(b) gate avalanche and forward bias.

capacitor there is additional current to help improve the switching speed of the JFET. From the switching waveforms the current rise time is reduced from 6ns to 5ns and the current fall time is reduced from 30ns to 23ns.

The case temperature of the test SiC JFET and SiC diode is increased to 200°C and the same switching measurements recorded and are given in Fig. 12. Fig. 12(a) shows the turn–on and off behavior of the JFET when a load current of 3A is switched. It can be seen that the peak current flowing in the JFET during turn-on is less than for the case at 25°C. This is because the maximum current (saturation current of the JFET) is less and the on resistance is greater at higher temperatures. Overall the turn-on and off waveform shapes are very similar. The turn on and off times for both 25°C and 200°C have been measured, with better resolution than from Figs. 11 and 12, are given in Table I. It can be seen that the delay time does not change, within measurement accuracy, with temperature although the pinch off voltage does change by 1 to 2V. This is because the time difference to change the gate voltage several volts is less than 0.5ns. Both the current rise and fall times for the JFET have increased, resulting in a slower switching performance and increased losses at 200°C.

TABLE I. SiC JFET SWITCHING TIMES

| Condition | Turn on (ns) | | | Turn off (ns) | |
|---|---|---|---|---|---|
| | *delay* $t_d$ | *I rise* $t_{r\,i}$ | *V fall* $t_{f\,v}$ | *delay* $t_d$ | *V fall* $t_{f\,i}$ |
| 25°C Non-avalanche | 6 | 6 | 25 | 9 | 30 |
| 25°C Avalanche | 8 | 5 | 22 | 11 | 23 |
| 200°C Non-avalanche | 6 | 10 | 32 | 10 | 28 |
| 200°C Avalanche | 8 | 10 | 26 | 11 | 27 |

Switching the SiC JFET quickly in circuits with high DC voltage levels results in very high dv/dt levels that are much greater than for IGBTs, which are today's device of choice for high voltage operation. From the switching waveforms in Figs. 11 and 12 the dv/dt and di/dt magnitudes are measured and given in Table II. The highest dv/dt and di/dt levels both occur during the turn-on of the SiC JFET using the avalanche mode gate driver. At room temperature the dv/dt level exceeds 40kV/µs with the highest value being 50kV/µs. This is much higher than is the rating of commonly used isolated gate driver

devices based on opto-couplers. For example, the opto-gate driver used in the test circuit has a minimum dv/dt rating of 15kV/µs, and a typical rating of 30kV/µs. Therefore additional considerations must be taken into account for the design of the gate drive to ensure that the switching signal isolation method has an appropriate common mode rating or additional components added to reduce the dv/dt seen by the isolation device. In addition to the signal isolation device, the gate driver power supply must also be rated for the required dv/dt level. The power supply must have sufficient isolation and a low primary to secondary capacitance to ensure the common mode currents to the control side are kept to a minimum.

TABLE II. SIC JFET SWITCHING VOLTAGE AND CURRENT RATES

| Condition | Turn on | | Turn off | |
|---|---|---|---|---|
| | *dv/dt (kV/µs)* | *di/dt (A/µs)* | *dv/dt (kV/µs)* | *di/dt (A/µs)* |
| 25°C Non-avalanche | 41 | 575 | 25 | 80 |
| 25°C Avalanche | 50 | 606 | 34 | 107 |
| 200°C Non-avalanche | 27 | 333 | 32 | 86 |
| 200°C Avalanche | 33 | 333 | 32 | 89 |

Over the measured temperature range the turn-on and off times are of the order of 40ns each, therefore it is feasible to uses these SiC JFET devices in a circuit operating at high switching frequencies greater than 500 kHz. For these frequencies the signal isolation device is required to have short propagation delays

Further work needs to be carried out on the switching performance of the JFETs including repeating the measurements with a bridge leg of JFETs. The operation of the bridge leg with and without SiC diodes will be investigated. In addition, methods for providing signal isolation techniques with low delay times, and high dv/dt capabilities will be investigated. A converter bridge leg that can be used in a fully SiC back-to-back converter application is be constructed and tested.

## IV. CONCLUSIONS

This paper has presented the static and dynamic characteristics of a SiCED 1300V, 4A SiC JFET that includes a description of the device's semiconductor structure. The pinch off voltage and gate avalanche voltage vary with each device and with operating temperature. To ensure the JFET is turned off a suitably large negative gate voltage needs to be applied; however this large gate voltage may breakdown the gate p-n junction. Therefore the gate and on-state characteristics are used to design a suitable JFET gate driver that allows the gate to be operated in avalanche and limits the average gate current to a low level.

A small positive gate voltage is applied during the initial turn-on to reduce the on-state resistance and improve the switching speed of the SiC JFET. With the use of the proposed gate driver the turn-on and off times are less than 35ns at room temperature when switching 3A at 600V. The maximum dv/dt measured is 50kV/µs and therefore special care has to be applied to the design of the signal isolation method and gate driver power supply. Overall the proposed gate driver circuit ensures fast and reliable switching for all SiC JFETs.

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