Comparison of Performance and Realization Effort of a Very Sparse Matrix Converter to a Voltage DC Link PWM Inverter with Active Front End

Simon Round, Frank Schafmeister, Marcelo Heldwein, Eduardo Pereira, Leonardo Serpa, Johann Kolar*

This paper undertakes an unbiased comparison of the very sparse matrix converter (VSMC) and the back-to-back voltage DC-link converter (BBC) for a permanent magnetic synchronous motor drive application. The VSMC has the same functionality as the conventional matrix converter but a reduced number of switches and lower control complexity. The two converters are designed with a thermal rating of 6.8kW for an ambient temperature of 45°C. From the design, the volume of the VSMC is 2.3 liters and is half that of the BBC. The efficiency for the VSMC at full load is 94.5% compared to 92% for the BBC. At very low output frequencies the output current of the VSMC can be increased by 25% above nominal compared to a 54% decrease for the BBC. Overall the VSMC offers significant advantages in volume and efficiency for motor drive applications compared to the BBC.

Keywords : matrix converter, back-to-back converter, efficiency comparison, volume comparison, converter design

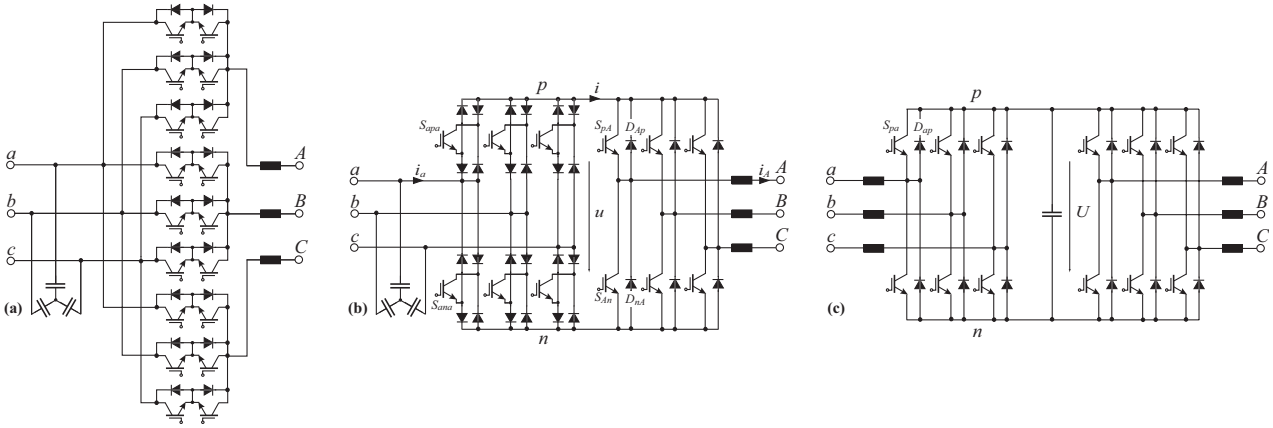


Fig.1 Topologies of Bi-directional AC-AC converters (a) Conventional Matrix Converter, (b) Very Sparse Matrix Converter[4] and (c) PWM inverter with active front end or Back-to-Back Converter, which requires an additional 3 boost inductors and a DC link capacitor.

1. Introduction

Traditional three-phase AC motor drive systems are constructed using a six-switch inverter, an uncontrolled rectifier mains connection and large electrolytic DC-link capacitors. Although the drive system is able to provide variable frequency and voltage to motor at a high efficiency, the mains input currents are non-sinusoidal and the power flow is unidirectional. The matrix converter is an alternative topology that directly produces a variable amplitude and frequency three-phase output from a three-phase input source without any energy storage in a DC-link. In addition to a unity power factor mains current and bi-directional power flow, the only passive components the matrix converter has are small AC filtering capacitors, therefore the matrix converter is sometimes referred to as an "all silicon converter"[1]~[3]. To achieve an equivalent functionality to the matrix converter, using more traditional converter topologies, requires a two-stage AC/DC/AC conversion process, where two voltage DC-link PWM converters are connected in a back-to-back configuration (BBC) as shown in Fig.1(c). In the literature it is often claimed that the matrix converter is more compact and efficient than an equivalent BBC system. Therefore one has to undertake an unbiased comparison of the matrix converter and BBC in terms of compactness, which includes the EMI filtering requirements, efficiency and torque rating for a typical AC motor drive application.

The conventional matrix converter (CMC) employs nine bi-directional switches (Fig.1(a)), presently constructed from two IGBTs and two diodes, to selective connect the input phases to the output phases[1]. The use of the 18 IGBTs and 18 diodes allows the selective turn-on of the switch for each current direction using a safe modulation strategy. The sparse matrix converter (SMC), implemented with 15 switches and not considered further, and very sparse matrix converter (VSMC), shown in Fig.1(b), have been proposed[4]. In the case of the VSMC the number of controlled switches reduces to 12 and results in an output inverter stage that is the equivalent to the conventional BBC implementation. The (V)SMC are functional equivalent to the CMC but the (V)SMC offers a lower realization effort and less control complexity. In this paper the BBC will be compared against the VSMC.

* Swiss Federal Institute of Technology,
Power Electronic Systems Laboratory,
Physikstrasse 3, 8092 Zurich, SWITZERLAND
http://www.pes.ee.ethz.ch
round@lem.ee.ethz.ch, schafmeister@lem.ee.ethz.ch,
pereira@lem.ee.ethz.ch, serpa@lem.ee.ethz.ch,
heldwein@lem.ee.ethz.ch, kolar@lem.ee.ethz.ch

In order to perform an unbiased comparison for a motor drive application, the same motor specification can not be used for both converter systems as this would disadvantage either of the converter types, depending on the motor specification.

This can be explained by considering that in the case of the BBC, the active front end boosts the DC link voltage above the peak of the maximum operating voltage in order to ensure controllability. Therefore the motor's nominal operating voltage can be specified as the highest input voltage minus a control margin. For a constant output power this results in a reduced output current and an increased BBC efficiency compared to the case if a motor with a low voltage mains rating is used.

In the case of the matrix converter the maximum output voltage available is always lower than the input voltage. Therefore the motor specification should have a nominal voltage that is highest achievable output voltage when the matrix converter is operated from the lowest input voltage minus a control margin. This nominal output voltage level is much lower than the output voltage for the case of the BBC. Therefore for the same output power rating the matrix converter's output current rating is higher and its losses are increased. By selecting a motor with a voltage rating that is suitable for the matrix converter, this would result in a BBC with higher output currents than for the case of a motor with a higher nominal voltage rating. Therefore to make a direct comparison, each converter type requires a special motor design to ensure the efficiency of each converter is maximized.

From Fig.1(b) it can be seen that the VSMC has a DC link between the input and output stages, although it does not use any energy storage capacitors. To better compare the physical size of the BBC and VSMC, the BBC is considered using the minimum DC-link capacitance possible for normal operation[5].

In this paper the claims that the matrix converter has a higher power density, including EMI filter, and efficiency than the BBC are determined for an AC motor drive application. In Section 2 the basic operation of the VSMC and the BBC, including modulation strategies, typical voltage and current waveforms are presented. Section 3 presents the analytical calculation of stresses on the converters' components. The design of each converter, including thermal and EMI requirements, is presented in Section 4. The VSMC and the BBC are then evaluated in terms of efficiency and operating requirements in Section 5.

2. Basic Principle of Operation

2.1 Matrix Converter For the conventional matrix converter the bi-directional switches must be operated so that any time two phases of the input are not shorted together and that the output current is not open-circuited. To provide reliable current commutation between the switches a multi-step commutation strategy is employed that measures the direction of the current. In contrast the VSMC configuration provides an additional degree of freedom in that the output stage can be switched into free-wheeling operation and this allows the input stage to commutate with zero DC link current. This allows zero switching losses for the input stage.

The matrix converters are limited to producing an output voltage that is 0.866 of the input voltage. Although the matrix converter does allow over-modulation operation, the penalty is an increase in the input current distortion[1].

For the VSMC, two modulation schemes have been previously presented[6]. In both modulation schemes the commutation of the input stage at zero current can be seen in Fig.2. The first modulation scheme (*MS1*) switches the input stage so that the voltage across the DC link goes from the highest and second highest positive line-line voltage, and this produces the maximum output voltage range (Fig.2(a)). However relatively large switching losses occur, especially for generating low output voltages which are required for low output voltage/speed motor operation. The second modulation scheme (*MS2*) proposed reduces the switching losses significantly for the case where the desired output voltage amplitude is less than half of the input voltage amplitude. In this modulation scheme the input stage switches the lowest positive and second highest input voltage into the DC link (Fig.2(b)) and this reduces the switching losses.

Fig.3 shows simulated results for the input and output waveforms of the VSMC when operated with the two modulation methods. The output frequency is 100Hz, the input frequency is 50Hz and the switching frequency is 25kHz. From Fig.3(a) it can be seen that the average DC link voltage is much higher than for the low voltage modulation scheme in Fig.3(c).

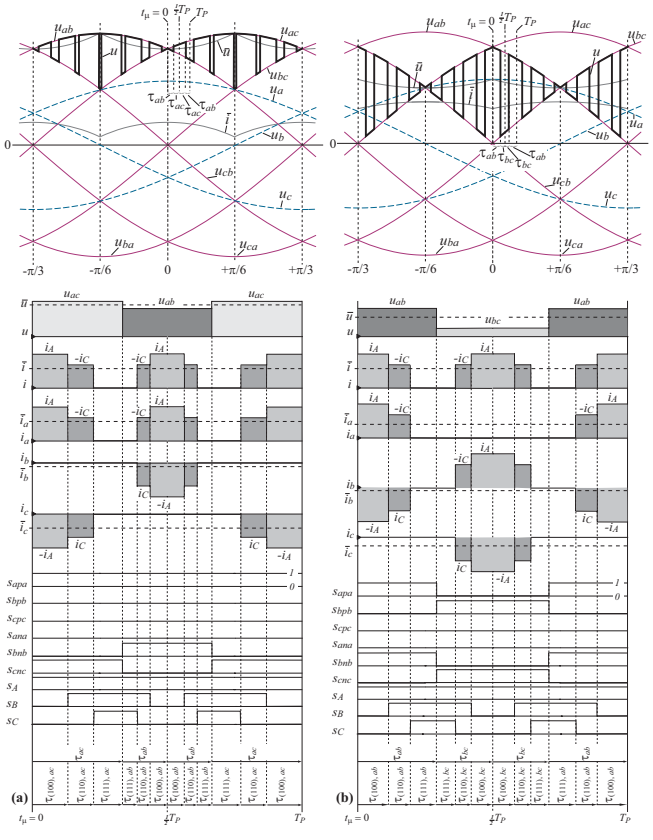


Fig.2 VSMC Modulation Schemes (a) Conventional Modulation Scheme[4]; (b) Low Output Voltage Modulation Scheme[6]. Both (a) and (b) shows the time behavior of u, i, mains phase current i_i within a pulse period t_μ=0…T_P for φ_1 in 0…+π/6 and φ_2 in 0…+π/3 (φ_1 & φ_2 denote the phase of the reference values of the input and output voltage space vector respectively).

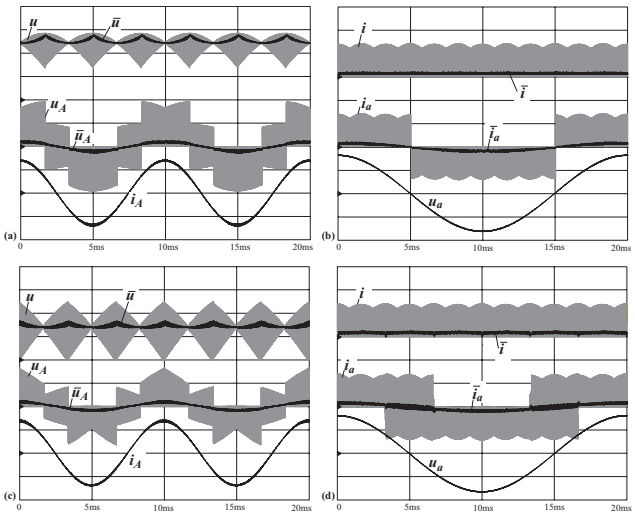


Fig.3 Simulation of the VSMC operating behavior for *MS1* (a)&(b) and *MS2* (c)&(d)); (a)&(c) DC link voltage u, local average $\bar{u}$, output phase voltage u_A (w.r.t load star point), local average $\bar{u}_A$, output phase current i_A; (b)&(d) DC-link current i, local average $\bar{\imath}$, input phase current i_a, local average $\bar{\imath}_a$, input phase voltage u_a; scales: 200V/div, 15A/div; M_{12}=0.1, Φ_2=0.

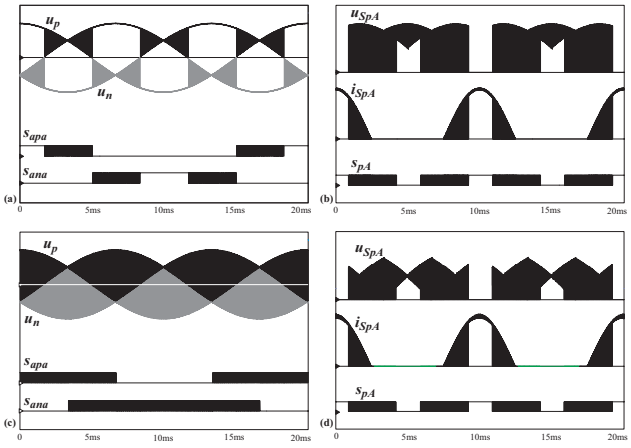


Fig.4 Modulation of the VSMC input and output stage for *MS1* (a)&(b) and *MS2* (c)&(d) for output current phase displacement Φ_2=0. Representation of positive and negative DC link bus, u_p and u_n, w.r.t the mains star point ((a)&(c)) and switching functions s_{apa} and s_{ana} of input stage bridge leg *a*; also shown: voltage, current and switching function of transistor S_{pA} on VSMC output stage.

The output stage switching losses are not only dependent on the DC-link voltage but also on the current that is switched. Therefore the switching losses can be reduced if an output stage bridge is not switched in the vicinity of the phase current maxima, but rather the output phase is clamped to the positive or negative DC bus for an interval of $\pi/3$ [6]. As is shown in Fig.4 there is no switching around the maximum of the phase current and this will result in a reduction of the switching loss.

2.1.1 Unbalanced Mains Under normal operation of the matrix converter it is likely that the input supply voltage would contain a degree of unbalance and/or voltage distortion. If no compensation is applied then this unbalance and distortion would directly appear in the output voltages. In [7] it is presented, for the case of unbalanced input voltages, that the output has no distortion if the input current command in the stationary reference frame is set such that the instantaneous effective power command is constant and the instantaneous reactive power is varied to compensate for the negative sequence component. This implementation is relatively simple and reduces the output voltage distortion. Another method has been proposed in [8] where a direct feed-forward unbalance control scheme reduces the influence of input voltage distortion. The line side source voltage vector is measured and its fundamental component determined using a Fourier transform. This information is then used to generate the appropriate distorted switching functions of the line side converter that are then able to reduce the distortion in the output waveforms.

2.2 Back-to-Back Converter

The BBC is constructed using a six-switch active rectifier and six-switch inverter connected together with a common DC-link. The rectifier is operated to draw unity power factor sinusoidal currents from the input mains, while the inverter provides the variable frequency and output voltage to the motor. Fig.5 shows a comparison between the input and output waveforms generated by the BBC compared to the VSMC for nominal operation. In the case of the BBC it can be seen that the converter is operating from a higher DC bus by the level of the output voltage waveforms. The output motor current is lower than the motor current for the VSMC since the motors for each converter have different specifications. The input current waveforms for both converter systems have a very similar shape.

The BBC input and output waveforms have been generated using space vector modulation. The advantage of the BBC over the VSMC is that the output voltage can reach higher levels before going into the over-modulation region due to the higher DC-link voltage produced by the boosting action of the rectifier.

The BBC can also operate with unbalanced mains voltage conditions, but the degree of unbalance that allows normal operation is dependent on the sizing of the DC-link capacitor. For low values of DC-link capacitance there will be an increased level of low-frequency voltage ripple on the DC-link, which can impact operation at high modulation indexes.

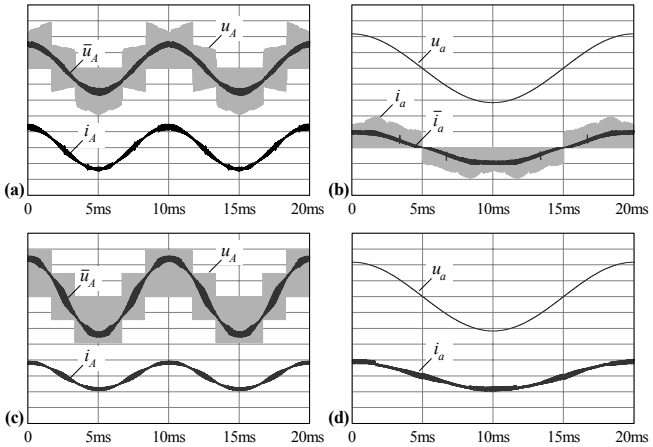


Fig.5 Comparison of the VMSC (a) output and (b) input waveforms and the BBC (c) output and (d) input waveforms operating at the nominal output power of 6.8kW. Output voltages shown include the instantaneous output voltage and averaged output voltage. Scales: 150V/div, 15A/div.

The input and output switching frequencies can be independently selected to optimize the input inductances, and switching losses. Although having non-synchronized switching frequencies increases the ripple current of the DC-link capacitor. In this comparison the switching frequency for both converters is fixed at 20kHz.

2.3 DC/DC Equivalent The advantages of a VSMC as compared to a BBC are obvious from Fig.6 where both converters are represented by their DC-DC equivalent circuits. For the case of the BBC the DC-DC equivalent is a boost converter followed by a buck converter if energy conversion from the mains to the load is considered. In this case the DC link voltage is impressed by a DC link capacitor C_1 and switching losses occur in the rectifier as well as for the inverter stage. In contrast, for the VSMC where the equivalent circuit is two buck converters, the switching losses only occur for the input or for the output stage. Therefore, the main advantage of a VSMC as compared to a BBC is not just a lower volume of the passive power components but a potentially higher efficiency of the energy conversion at high switching frequency. However the disadvantage of the VSMC (and of the CMC), due to its buck-buck equivalent, is the relatively low maximum amplitude of the output voltage.

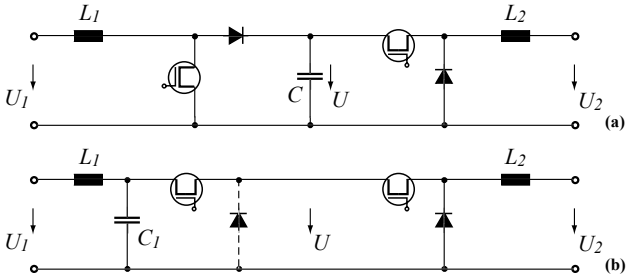


Fig.6 DC-DC equivalent circuits of the three-phase AC-AC converters (a) Back-to-Back with DC voltage link (Boost-Buck) and (b) Matrix (Buck-Buck).

3. Component Stresses

The stresses on the passive and switching components can be determined using analytical equations. In this section the analytical calculations for conduction and switching losses and passive component stress are given for the VSMC and BBC.

3.1 Very Sparse Matrix Converter[4]

For the VSMC it is important to accurately model the conduction losses of the switches and diodes since there are no rectifier switching losses.

3.1.1 Conduction Losses The mathematical representation of the IGBT (and/or diode) conduction losses for both topologies is based on a model comprising a series voltage source $U_{F,i}$ and a differential resistor r_i . These two on-state parameters have been experimentally measured (Table 1) for the IGBTs and diodes used to construct the two converters[9]. Accordingly, the local average value of the conduction power loss can then be expressed.

Table. 1. On-state parameters of the IGBT and diode module (part IXYS FII50-12E) for a junction temperature of T_j=120°C.

On-State Parameters		
	U_F (mV)	r (mΩ)
S	768	78.7
D	732	38.0

3.1.2 Conduction Losses - Rectifier Stage The worst operating case for conduction losses is when both the modulation index and output power factor are one[10]. The average and rms worst case currents are

$$\bar{I}_{Sapa,WC} = \frac{\sqrt{3}\hat{I}_2}{2\pi}; \quad I^2_{Sapa,rms,WC} = \frac{5\hat{I}_2{}^2}{2\pi^2}. \tag{1}$$

Using these currents and the two on-state parameters leads to the specific conduction losses of the three input stage components:

$$P_{C,\mathrm{Rect},Sapa} = u_{F,S} \cdot \bar{I}_{Sapa} + r_S \cdot I^2_{Sapa,rms} \tag{2}$$

$$P_{C,\mathrm{Rect},Dpa} = 0 \tag{3}$$

$$P_{C,\mathrm{Rect},Dap} = u_{F,D} \cdot \bar{I}_{Sapa} + r_D \cdot I^2_{Sapa,rms} \tag{4}$$

The total VSMC rectifier conduction losses are calculated using

$$P_{C,\mathrm{Rect},VSMC} = 6 \cdot (P_{C,\mathrm{Rect},Sapa} + 2P_{C,\mathrm{Rect},Dap} + 2P_{C,\mathrm{Rect},Dpa}). \tag{5}$$

3.1.3 Conduction Losses - Inverter Stage For the inverter stage the transistor losses are given as

$$P_{C,Inv,S} = u_{F,S} \cdot \hat{I}_2 \frac{2+\sqrt{3}M_{12}\cos\Phi_2}{4\pi} + r_S \cdot I^2_{Inv,S,rms} \tag{6}$$

where the squared rms-value of transistor current is

$$I^2_{Inv,S,rms} = \hat{I}_2{}^2 \frac{2\pi + 6\Phi_2 + (8M_{12}-6)\sin(2\Phi_2 - \frac{\pi}{3}) - 16M_{12}\sin(\Phi_2 - \frac{\pi}{3})}{24\pi}. \tag{7}$$

For the diode losses a similar formulation is used

$$P_{C,Inv,D} = u_{F,D} \cdot \hat{I}_2 \frac{2-\sqrt{3}M_{12}\cos\Phi_2}{4\pi} + r_D \cdot I^2_{Inv,D,rms} \tag{8}$$

where

$$I^2_{Inv,D,rms} = \hat{I}_2{}^2 \frac{4\pi - 6\Phi_2 - (8M_{12}-6)\sin(2\Phi_2 - \frac{\pi}{3}) + 16M_{12}\sin(\Phi_2 - \frac{\pi}{3})}{24\pi}. \tag{9}$$

The conduction losses of the entire inverter stage can be directly calculated by

$$P_{C,Inv,VSMC} = 6 \cdot (P_{C,Inv,T} + P_{C,Inv,D}). \tag{10}$$

3.1.4 Switching Losses To determine the switching losses the switching behavior of the IGBTs and diodes have been measured[9] for a junction temperature of T_j=120°C. Using a quadratic least-square approximation of the measured data for voltage and current, where only physically sensible terms are considered, it is possible to determine a switching loss equation that has 5 coefficients (K_1...K_5) given in Table 2 for a junction temperature of 120°C.

Table 2 Coefficients $K_1 \ldots K_5$ derived by least-square approximations of measured IGBT/ diode (part IXYS FII50-12E) switching losses for a junction temperature of 120°C [9].

IGBT-Switching Loss Parameter					
	K_1	K_2	K_3	K_4	K_5
$S_{on\rightarrow off}$	179	-1.31	$650\ 10^{-3}$	$-116\ 10^{-3}$	$3.48\ 10^{-3}$
$S_{off\rightarrow on}$	70.0	2.94	$518\ 10^{-3}$	$102\ 10^{-3}$	$-1.55\ 10^{-3}$
$D_{on\rightarrow off}$	97.9	-3.73	$488\ 10^{-3}$	$140\ 10^{-3}$	$4.27\ 10^{-3}$
Units	$nWs(VA)^{-1}$	$nWs(VA^2)^{-1}$	$nWs(V^2)^{-1}$	$nWs(V^2A)^{-1}$	$nWs(V^3A^2)^{-1}$

3.1.5 Switching Losses - Rectifier Stage Since the rectifier stage switches with zero link current there are no switching losses.

$$P_{Sw,\mathrm{Rect},S/D} = 0. \tag{11}$$

3.1.6 Switching Losses - Inverter Stage The switching losses in the inverter stage for the IGBTs and diodes can be determined from

$$P_{Sw,S/D} = \frac{f_p \hat{U}_1}{32\pi^2} \begin{pmatrix} 48\hat{I}_2\left(6K_1 + K_2\hat{I}_2\pi\right) \\ +4\hat{U}_1(3\sqrt{3}+4\pi)\left(6K_4\hat{I}_2 + 2\pi K_3 + \pi K_5\hat{I}_2^2\right) \\ -12\hat{I}_2\left(12K_1 + K_4(3\sqrt{3}+4\pi)\hat{U}_1\right)\cos\Phi_2 \\ -3\hat{I}_2^2\left(12\sqrt{3}K_2 + \hat{U}_1K_5(9+4\sqrt{3}\pi)\right)\cos(2\Phi_2)d \end{pmatrix} \tag{12}$$

where the substitution of

$$K_i \rightarrow K_{i,Son} + K_{i,Soff} \tag{13}$$

is used for the transistors and

$$K_i \rightarrow K_{i,Doff} \tag{14}$$

for the diodes.

Since this polynomial approach[9] depends linearly on the coefficients K_i, the switching losses of the complete VSMC can be calculated by the substitution

$$K_i \rightarrow 6(K_{i,Son} + K_{i,Soff} + K_{i,Doff}). \tag{15}$$

3.1.7 AC Filter Capacitor Stresses The stresses on the filter capacitors, in general, are dependent on the rms of the current since this current is responsible for losses in the capacitor's ESR. For the conventional modulation strategy (*MS1*) the global rms value of capacitor current is [10]

$$I^2_{CFilt,MS1,rms} = \hat{I}_2{}^2 M_{12}\frac{24 - 3\pi^2 M_{12}\cos^2(\Phi_2) + 16\cos(2\Phi_2)}{8\pi^2} \tag{16}$$

For low output voltage modulation (*MS2*) the capacitor current stress is increased

$$I^2_{CFilt,MS2,rms} = \hat{I}_2{}^2\sqrt{3}M_{12}\frac{24 - \sqrt{3}\pi^2 M_{12}\cos^2(\Phi_2) + 16\cos(2\Phi_2)}{8\pi^2}. \tag{17}$$

3.2 Back-to-Back Converter The same mathematical model for the IGBT and diode conduction and switching losses as for the VSMC is used for the BBC.

3.2.1 Conduction Losses - Rectifier Stage To calculate the IGBT losses requires the average and rms current as given by

$$\bar{I}_{S,\mathrm{Rect}} = \frac{\hat{I}_1}{2}\cdot\left(\frac{1}{\pi} - \frac{m_{\mathrm{Rect}}}{4}\right) \tag{18}$$

$$I_{S,\mathrm{Rect},rms} = \hat{I}_1\cdot\sqrt{\frac{1}{4} - \frac{m_{\mathrm{Rect}}}{3\pi}}. \tag{19}$$

The switch conduction losses are

$$P_{C,\mathrm{Rect},S} = u_{F,S}\cdot\bar{I}_{S,\mathrm{Rect}} + r_S\cdot I^2{}_{S,\mathrm{Rect},rms}. \tag{20}$$

For the diode the average and rms current are

$$\bar{I}_{D,\mathrm{Rect}} = \frac{\hat{I}_1}{2}\cdot\left(\frac{1}{\pi} + \frac{m_{\mathrm{Rect}}}{4}\right) \tag{21}$$

$$I_{D,\mathrm{Rect},rms} = \hat{I}_1\cdot\sqrt{\frac{1}{4} + \frac{m_{\mathrm{Rect}}}{3\pi}}. \tag{22}$$

The diode conduction loss is calculated using

$$P_{C,\mathrm{Rect},D} = u_{F,D}\cdot\bar{I}_{D,\mathrm{Rect}} + r_D\cdot I^2{}_{D,\mathrm{Rect},rms}. \tag{23}$$

The total conduction losses are

$$P_{C,\mathrm{Rect},B2B} = 6\cdot(P_{C,\mathrm{Rect},S} + P_{C,\mathrm{Rect},D}). \tag{24}$$

3.2.2 Conduction Losses - Inverter Stage For the inverter stage the IGBT average and rms currents are

$$\bar{I}_{S,Inv} = \frac{\hat{I}_2}{2}\cdot\left(\frac{1}{\pi} - \frac{m_{Inv}}{4}\right) \tag{25}$$

$$I_{S,Inv,rms} = \hat{I}_2\cdot\sqrt{\frac{1}{4} - \frac{m_{Inv}}{3\pi}}. \tag{26}$$

The switch conduction losses are calculated using

$$P_{C,Inv,S} = u_{F,S}\cdot\bar{I}_{S,Inv} + r_S\cdot I^2{}_{S,Inv,rms}. \tag{27}$$

The diode average and rms currents are

$$\bar{I}_{D,Inv} = \frac{\hat{I}_2}{2}\cdot\left(\frac{1}{\pi} + \frac{m_{Inv}}{4}\right) \tag{28}$$

$$I_{D,Inv,rms} = \hat{I}_2\cdot\sqrt{\frac{1}{4} + \frac{m_{Inv}}{3\pi}}. \tag{29}$$

The diode conduction loss is calculated from

$$P_{C,Inv,D} = u_{F,D}\cdot\bar{I}_{D,Inv} + r_D\cdot I^2{}_{D,Inv,rms} \tag{30}$$

For the inverter stage the total conduction losses are

$$P_{C,Inv,B2B} = 6\cdot(P_{C,Inv,S} + P_{C,Inv,D}). \tag{31}$$

3.2.3 Switching Losses To calculate the switching losses the general formulation given in (32) is used for both rectifier and inverter stages.

$$P_{sw,S/D} = 2Uf_p\cdot\left(K_1\bar{I}_A + K_2I^2_{A,rms} + \frac{1}{3}K_3U + K_4U\bar{I}_A + K_5UI^2_{A,rms}\right) \tag{32}$$

where

$$K_i \rightarrow K_{i,Son} + K_{i,Soff} \tag{33}$$

is used for the transistors and

$$K_i \rightarrow K_{i,Doff} \tag{34}$$

for the diodes.

For the rectifier stage the average and rms currents are calculated using

$$\bar{I}_{A,\mathrm{Rect}} = \frac{\hat{I}_1}{2\pi} \tag{35}$$

$$\bar{I}^2_{A,rms,\mathrm{Rect}} = \frac{1}{4}\hat{I}_1^2\left(\frac{2}{3} - \frac{\sqrt{3}}{2\pi}\right) \tag{36}$$

and for the inverter stage they are

$$\bar{I}_{A,Inv} = \frac{\hat{I}_2}{2\pi} \tag{37}$$

$$\bar{I}^2_{A,rms,Inv} = \frac{1}{4}\hat{I}_2^2\left(\frac{2}{3} - \frac{\sqrt{3}}{2\pi}\right). \tag{38}$$

3.2.4 DC-Link Capacitor Sizing and Stresses To determine the minimum DC-link capacitor value a formulation, based on a DC/DC equivalent model, from pg. 56 of [11] is used. This formulation, given by (39), sizes the capacitor to ensure that the capacitor voltage does not fall below a defined minimum value during the transient from full regeneration to full motoring mode.

$$C_{DC-link,\min} = \frac{L \cdot P_2^2 \left[(E_{dc} - U_{dc})^2 - (E_{dc} + U_{dc})^2 \right]}{E_{dc}^2 \cdot U_{dc}^2 \left((\min(u_{dc}) + E_{dc})^2 - (U_{dc} + E_{dc})^2 \right)} \quad (39)$$

where L is dc equivalent inductance (2 times input inductance, Table 2.2. in [11]), P_2 is the nominal output power, E_{dc} is the peak input line voltage, and U_{dc} is the DC-link voltage.

To select a suitable capacitor for the link the ripple current the capacitor has to handle must be calculated. Using the method presented in [12] the ripple current can be determined from the difference between the rectifier's ripple current and the inverter's ripple current.

The rms input (output) current value of the inverter (rectifier) over an interval of 60° is given by (40) where i stands for either the rectifier or inverter:

$$I_{d,i,rms}^2 = \frac{3 \cdot \sqrt{3}}{2 \cdot \pi} \cdot m \cdot I_{i,rms}^2 \left(1 + \frac{2}{3} \cos 2\Phi_i \right) \quad (40)$$

Neglecting the power loss in the inverter (rectifier), the dc component of the input (output) current can be obtained based on the power balance such as:

$$\bar{I}_i = \frac{3}{2 \cdot \sqrt{2}} \cdot m \cdot I_{i,rms} \cdot \cos \Phi_i \quad (41)$$

Finally, the rms value of the inverter (rectifier) input (output) current ripple can be calculated as

$$\tilde{I}_{i,rms} = \sqrt{I_{d,i,rms}^2 - \bar{I}_i^2} \quad (42)$$

In order to obtain the DC-Link capacitor rms current, it is assumed that the switching of the rectifier and the inverter stages are synchronized. By summing the square of the rectifier and inverter rms ripple currents, a sensible estimate of the capacitor rms ripple current can be obtained from

$$\tilde{I}_{C,rms} = \sqrt{\tilde{I}_{\mathrm{Rect},rms}^2 + \tilde{I}_{Inv,rms}^2} \; . \quad (43)$$

4. Converter Design

In this comparison it is assumed that each converter is operating from 50 Hz, 400 V, +10%, -15%, 3-phase mains voltage supply. Each converter will be supplying a variable frequency, output voltage to a 6.8kW permanent magnetic synchronous machine. Both the VSMC and BBC are thermally rated for 6.8kW operation. The switching frequency for both stages of each converter is selected to be 20kHz since it is beyond the audible range. For both converters the minimal dynamic modulation margin is $\Delta M_{\min} = 5\%$.

For the VSMC operating at minimum voltage $U_{1,min}$ the modulation margin ΔM_{min} should be kept. Considering the maximal voltage transfer ratio of the matrix converter, the nominal output voltage (line-to-line) is

$$U_{2N} = \frac{\sqrt{3}}{2}(1 - \Delta M_{\min}) \cdot U_{1,\min} = 280V \quad (44)$$

The nominal output current is then defined by

$$I_{2N} = \frac{P_{2N}}{\sqrt{3} \cdot U_{2N}} = 14A \quad (45)$$

The ideal motor therefore has to be designed in order to reach its nominal operating point for U_{2N} and I_{2N} as specified.

For the case of the BBC, the DC link voltage U is determined, considering ΔM_{min} and $U_{1,max}$, from (46).

$$U = (1 + \Delta M_{\min}) \cdot \sqrt{2} \cdot U_{1,\max} \approx 655V \quad (46)$$

The nominal output voltage (line-to-line) then is given by U and ΔM_{min} and is

$$U_{2N} = (1 - \Delta M_{\min}) \cdot \frac{1}{\sqrt{2}} U = U_{1,\max} = 440V \quad (47)$$

With the specified power level it follows that the nominal output current I_{2N} is 8.9A.

Using the analytical equations presented in section 3 the current stresses for the rectifier and inverter stages of the VSMC and BBCs can be calculated and are presented in Fig.7. As can be seen the switch rms current for the VSMC is much higher than the BBC due the lower maximum output voltage for the same power rating. For the BBC the diode rms current in the rectifier stage is significantly higher than the IGBT rms current due to the boost action.

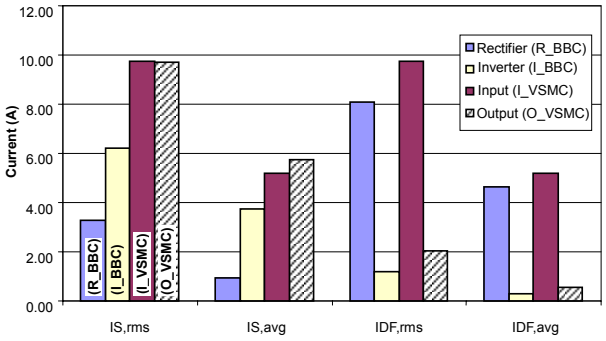


Fig.7 Current Stresses (switch rms and average, diode rms and average) for the rectifier and inverter stages of the VSMC and BBCs.

4.1 Design Procedure To produce a compact design it is desirable to use semiconductor modules that combine as many individual devices as possible into one package. For the BBC the IXYS phase leg modules (see Table 3), which contain 2 IGBTs and 2 fast diodes, have been selected. This IXYS module has a voltage rating of 1200V and a current rating of 32A at a case temperature of 90°C. The current rating is well within the rms and average currents as calculated and shown in Fig.7. For the VSMC the same IGBT module is used for the inverter stage but a bi-directional IGBT module, which includes a single IGBT and a bridge rectifier, is selected for the rectifier stage as it uses the same IGBT and ISOPLUS package as the BBC.

For BBC the other special components are the boost inductor and DC-link capacitors. Using (39) the minimum DC-link capacitance is calculated as 31µF and this is constructed from 4 parallel connected 8µF metal film capacitors. The total capacitor ripple current is 7.4A as calculated from (43) and each capacitor would then have 1.85A of ripple current. Each boost inductor has an inductance of 1mH and is constructed using two stacked Micrometals toroidal cores with 60 turns.

After the selection of the components the next step is to undertake a thermal analysis to determine the size of the heatsink, followed by the design of the EMI filters.

Table 3 Back-to-Back and Matrix Converter Components

Description	Back-to-Back	Very Sparse Matrix
Semiconductors		
Input	3 IXYS FII 50-12E	6 IXYS FIO 50-12BD
Output	3 IXYS FII 50-12E	3 IXYS FII 50-12E
Boost Inductor	3 1mH (toroidal)	- Not used
DC-Link Cap.	4 8µF, 400V_{AC}	- Not used

4.2 Thermal design Both the VSMC and BBCs have been thermally designed so that the maximum junction of any one semiconductor module is 150°C. The power dissipation of each switch module is calculated using the analytical equations of section 3 and is then used as the input to a 3-D thermal simulation. The length of the heatsink is adjusted to ensure that the maximum junction temperature is not exceeded. The results from the thermal analysis are shown in Fig.8 where the highest spot temperature on the VSMC heatsink is 122°C, whereas it is 104.5°C for the BBC.

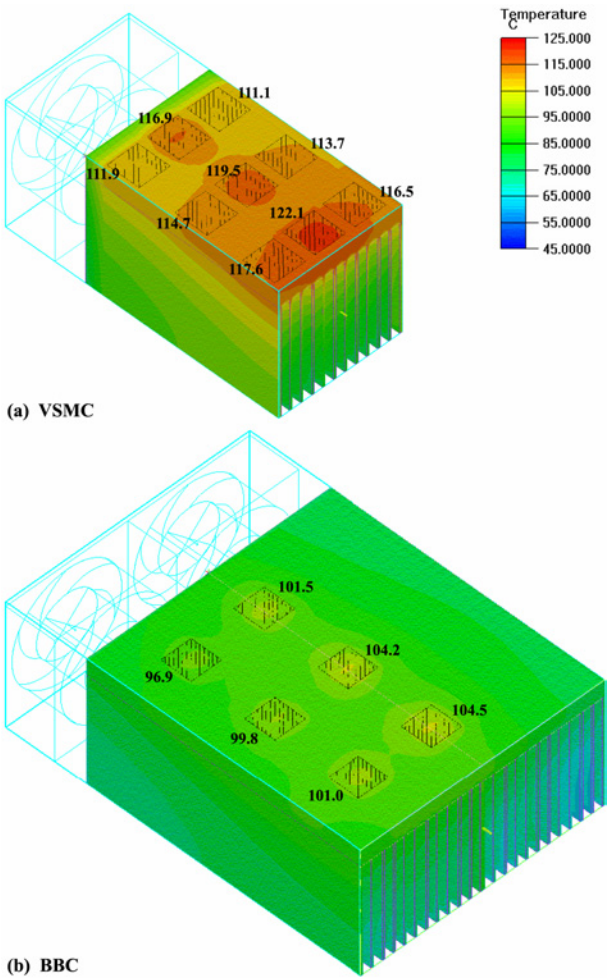


Fig.8 Thermal analysis of the (a) VSMC and (b) BBC's heatsink. Ambient temp. is 45°C and forced air cooling used. The fan type used is a Papst 80x80x32, 24VDC, 80m^3/h.

4.3 EMI Filter design In order to compare both drive systems regarding their EMC performance the standard CISPR 11:1997[13] is chosen for establishing the performance requirements where the frequency range of 0.15 to 30 MHz is considered for class B equipments. The largest emission condition is identified in both cases by analyzing the input current/voltage frequency spectrum of the converters and this is used as starting point for the design of the filters. The common mode (CM) sections of the VSMC and BBC filters employ the same topology and components and this is based on the fact that both systems are expected to present similar emission levels due to the same construction methods and operating behavior, although experimental verification is required to confirm this. The design procedure for the differential mode (DM) section of the filters is presented in [14] where the only difference is that in this paper a maximum value $QP_{max}(f)$, calculated approximately by linearly adding the RMS values $V_h(f)$ of the spectral components inside of the specified resolution bandwidth (RBW), is used instead of the non-linear calculations for a real Quasi-peak (QP) compliant measurement. By employing this procedure the computational effort is reduced and the final result will be a filter with an attenuation slightly higher than actually required. The input current spectra for both topologies and the expected DM conducted emission levels with the designed filters are shown in Fig.9 along with a simplified block diagram of the filter design procedure.

Having common EMC requirements and applying the presented design procedure to both designed drive systems make it possible to compare them (Table. 4) with regard to the physical dimensions and the total value of the components. In addition, the filter topology designed for the back-to-back system is shown in Fig.10 with the main components specified. For the VSMC system a filter with a similar structure, but different component values is designed. It is interesting to note that the volume of the EMI filter increases as the switching frequency is increased, since an increased level of switching harmonics now fall into the EMC frequency range of interest.

Table.4 EMC input filter components and physical dimensions.

Topology	Back-to-back	SMC
Total DM capacitance	15.54 μF	36 μF
Total DM inductance (10 kHz)	1.20 mH	1.29 mH
Total CM capacitance	28.2 nF	28.2 nF
Total CM inductance (10 kHz)	36 mH	36 mH
Total filter components volume	325 cm^3	360 cm^3

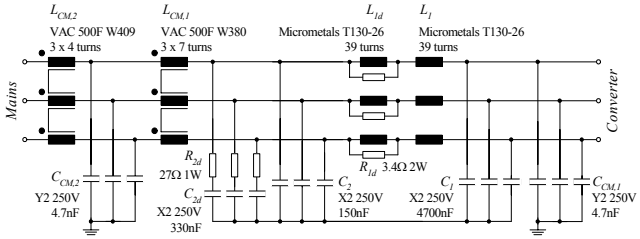


Fig.10 EMC input filter schematic for the BBC system and is designed to comply with CISPR 11 class B requirements.

4.4 Auxiliary power supply The auxiliary (house-keeping) power supply provides the power to the control electronics. This power supply must be designed to operate under all input voltage levels, including regeneration during mains loss up to 1100V. A two-switch, 30W flyback power supply is used for both the VSMC and BBC systems. The only difference is the placement of the reference potential for the control electronics. For the matrix converter the reference potential is placed at the star point of the AC capacitor filter, while for the back-to-back converter the reference potential is at the mid-point of DC bus. The auxiliary power supply design, in terms of input capacitance, does have an impact on ride through capability of the converter. This has not been considered in this implementation.

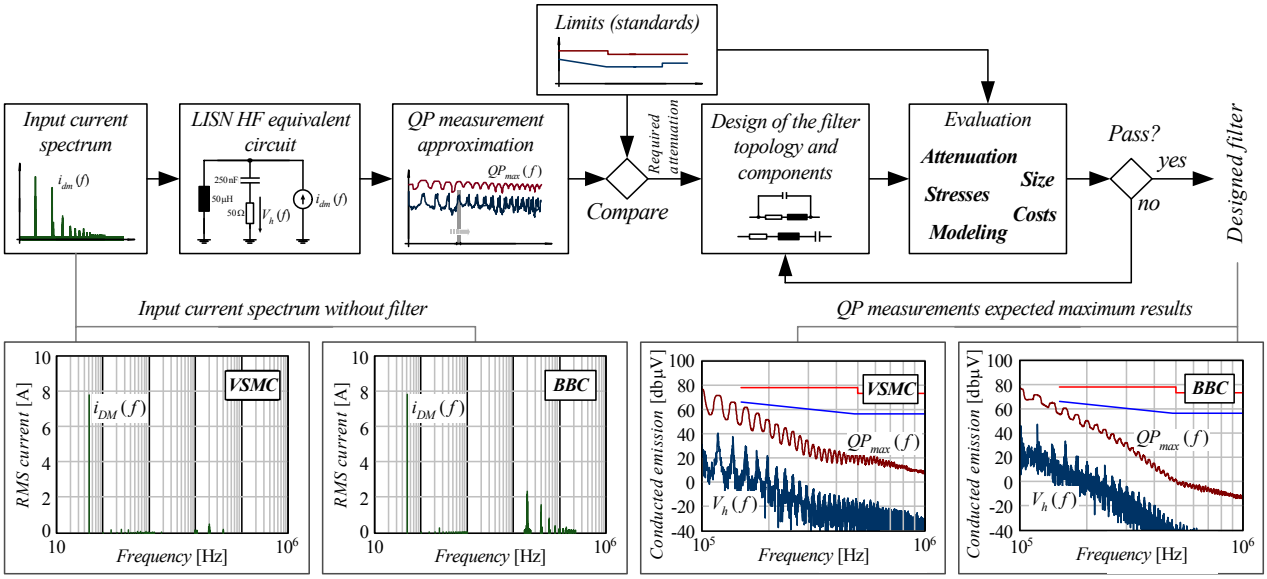


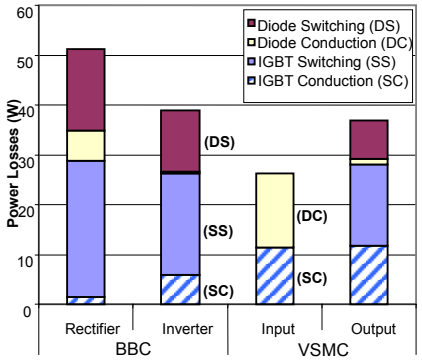
Fig.9 Filter design procedure and the input current spectra for the BBC and the VSMC, as well as the expected conducted quasi-peak emission levels measured for both systems.

4.5 Over-voltage Protection For the matrix converter, if an over-current fault occurs then the switching devices are typically turned off. This interrupts the load current and causes the load inductance to generate high over-voltages that must be prevented from damaging the converter. Over-voltages also occur when the mains voltage fails. Two methods have been proposed in the literature, firstly, a clamp circuit that is formed from two 3-phase diode-bridge rectifiers (one connected to the output and the other to the input terminals) and a capacitor and resistor on the dc side of the rectifier can be used[1]. If any over-voltage occurs on either the input or output terminals then this circuit will clamp the voltage and the energy is dissipated in the discharge resistor. The second method, presented in [15], replaces the clamp with varistors between each of the input phases and separate varistors connected between each of the output phases, together with a Zener diode added to each gate driver circuit to automatically to operate the IGBT in its linear region if the voltage across the device exceeds a maximum limit. With this method all of the switching devices are protected and the energy is quickly dissipated by the varistors and IGBTs.

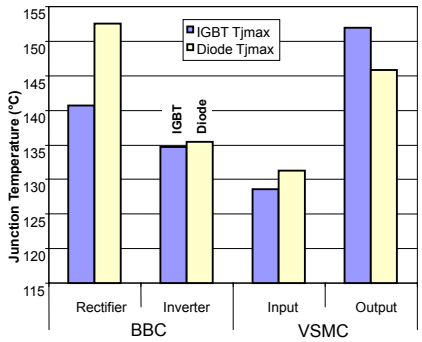
4.6 Physical Layout Fig.11 shows the physical layout arrangement of the VSMC and the BBC, where the layout includes all power devices, gate drives, passive components, EMI filter, fan, control and power supply. Both converters can be directly compared as they are drawn with the same scale. The overall volume of the VSMC is 2.3 liters compared to a volume of 4.6 liters for the BBC. The volumes of both these converters compare favorably to the volume of a standard diode-rectifier input, commercial 7.2kVA motor drive inverter that has a volume of 5.3 liters (including the enclosure and user interface). For the VSMC the output terminals and housekeeping power supply are placed over the heatsink fan. For the BBC the input boost inductors are placed in a space created by cutting out a section of the heatsink below the EMI input filter.

Fig.11 System layout and construction of (a) VSMC (24.4cm x 8.0cm x 11.8cm & volume is 2.3 liters) (b) BBC (22.7cm x 16.0cm x 13.4cm & volume is 4.6 liters).

4.7 Losses Fig.12(a) shows the power loss contributions for each switch and diode in the rectifier and inverter stages of the converters. It can be seen that the BBC has significantly higher losses than the VSMC. For the BBC the switching losses are the dominant factor for both stages. It can also be seen that there are no switching losses in the input stage of the VSMC. The thermally limiting device, as shown in Fig.12(b), for the converter design is the diode in the rectifier stage for the BBC and it is the output stage switch for the VSMC.



(a)



(b)

Fig.12 (a) Loss contributions and (b) junction temperatures of IGBTs and diodes at rated load for the BBC and VSMC.

5. System Evaluation

One key performance indicator is the system efficiency of the converters over the operating range. The efficiency is defined as

$$\eta = 1 - \frac{P_{Loss}(m, I_2)}{S_2(m, I_2)} \tag{48}$$

where $S_2(m, I_2) = \frac{3}{2} U_1 \cdot I_2 \cdot m$ and where m is the *modulation index* for either VSMC or BBC. (49)

Fig.13 presents the efficiency for the converters over varying modulation indexes and output current levels. It can be seen that the VSMC has an overall higher efficiency than the BBC, with the maximum efficiency at full load of the VSMC being 94.5% compared to 92% for the BBC.

To decrease the losses for the BBC it would be possible to decrease output switching frequency to 10kHz while retaining the input switching frequency at 20kHz in order to keep the boost inductor size small. This output switching frequency reduction would increase the efficiency by 1.5% but it would cause a higher DC link capacitor current stress. In performing this comparison it was decided to keep the switching frequency for both the input and output stages at 20kHz, which is outside the audible range.

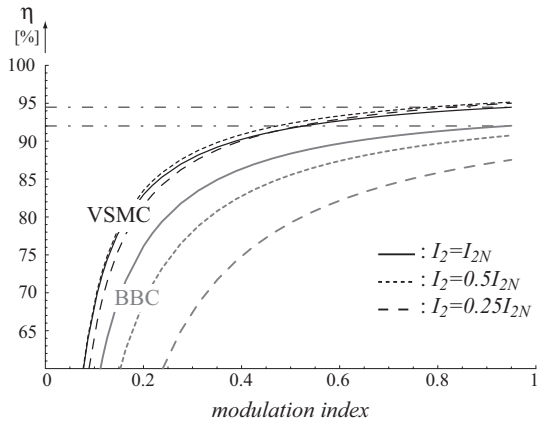


Fig.13 Efficiency comparison of the VSMC and BBCs for unity output power factor and varying output current.

An extreme operating point of the converters is for the case where the output frequency close to zero. This effectively causes "DC" to occur in the output phases, and in the worst case one transistor/diode pair has to switch the maximum peak output current for numerous mains cycles. Therefore the junction temperature of this highly stressed IGBT/diode pair will determine the maximum output current of the converter system. From Fig.14 it can be seen that for the BBC the output current has to be reduced to 46% of the nominal current for operation at zero output frequency.

For the VSMC, there is the possibility of applying the low dc-link voltage modulation strategy (*MS2*) and this results in a reduction of the output stage switching losses by more than 30%. In addition it is possible to force some output stage commutations by the appropriate switching actions of the input stage transistors[9]. This allows a certain amount of the switching losses to be shifted to the input stage and be equally distributed among all of the input stage transistors. These modulation options allow a significantly reduction of the output device losses and as a consequence the maximum output current amplitude can be increased by 25% (Fig.14) before the junction of the (clamping) transistor reaches 150°C.

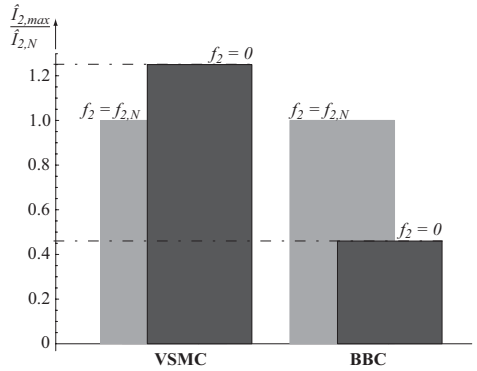


Fig.14 Calculated change in the maximum peak current for operation at nominal and zero output frequency for the VSMC and BBC. Due to various modulation strategies the VSMC can increase the output current by 25%, while for the BBC the output current must decrease by 54%.

5.1 Ride-Through In most modern drive systems it is desirable to implement a ride-through capability for brief input voltage dips. A common method is to de-accelerate the motor and extract the stored energy in the rotating machine to keep the auxiliary power supply and control electronics operational as well as maintaining the magnetization of the motor. For the BBC, it inherently has a DC link capacitor in which this energy can be stored but for the matrix converter there is no energy storage apart from the filter capacitors[16]. One approach is to use the over-voltage protection clamp circuit to store this energy. Another approach to extend the ride-through capability is presented in [17] where an additional capacitor and three switches are connected between the output and input of the matrix converter.

5.2 Control Both the VSMC and BBC systems require similar control hardware where a least 12 switches need to be controlled. The number of current sensors for the VSMC is less than the BBC where 2 are required for both the rectifier and inverter stages. The implementation of the control algorithms have similar complexity, although for the BBC system the switching of the input and output stages should be coordinated to minimize the DC link capacitor current stress. For any AC motor drive system it is desirable to have sensorless control implemented, depending on the final application requirements. Sensorless control[18] techniques can be equally applied to the matrix and BBCs and the final research aim of this research work is the implementation of a full sensorless control system for both the VSMC and BBC systems.

6. Conclusions

This paper has undertaken an unbiased comparison of the very sparse matrix and back-to-back converters. A VSMC has been used as the comparison as it is has the same functionality as the conventional matrix converter but a reduced number of switches and lower control complexity. Analytical equations detailing the conduction and switching losses of the both converter systems are presented. The VSMC and BBC design is undertaken assuming special purpose 6.8kW PMSM motors are applied to each converter. The converters have been designed for a thermal rating of 6.8kW, a mains voltage range of 340V to 440V, a 5% control margin and an ambient temperature of 45°C.

A limiting factor of the BBC is the diode in the IGBT module of the active rectifier. The volume of the VSMC (2.3 liters) is half that of the BBC (4.6 liters) and the efficiency for the VSMC is 94.5% compared to 92% for the BBC. The complexity of the two converters is very similar in terms of number of switches and control circuitry required. The volume of the EMI filter for the VSMC is only 10% larger than the BBC. A further advantage of the VSMC is that the continuous rated output current can be increased by 25% for standstill motor operation, while for the BBC it has to be decreased by 54%. Overall the very sparse matrix converter offers significant advantages over the back-to-back converter for motor drive applications.

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