Novel Phase Decoupling and Coordinating Tolerance Band Current Control for Three-Phase Three-Level PWM Rectifiers

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***Abstract*-A tolerance band (hysteresis) current controller is presented that provides phase decoupling control of a three-level, three-phase rectifier and allows the utilization of the full modulation range. The novel current control method provides coordinated switching between the phases and results in a near constant switching frequency and a current ripple performance that is similar to conventional carrier-based PWM controllers. Theoretical analysis of the control method is presented and the performance of the phase decoupling is experimental verified using a 5kW Vienna rectifier.**

I. INTRODUCTION

Three-phase PWM based rectifiers are desirable as the input phase currents can be controlled to have a sinusoidal shape. By using a three-level topology such as the Vienna rectifier in Fig. 1 the voltage stress on the switches is reduced to half that of a two-level topology. The control of the input current waveform shape for the three-level rectifiers can be divided into two categories, either the conventional carrier-based controller (CCC) or the conventional hysteresis (or tolerance band) controller (CHC) [1].

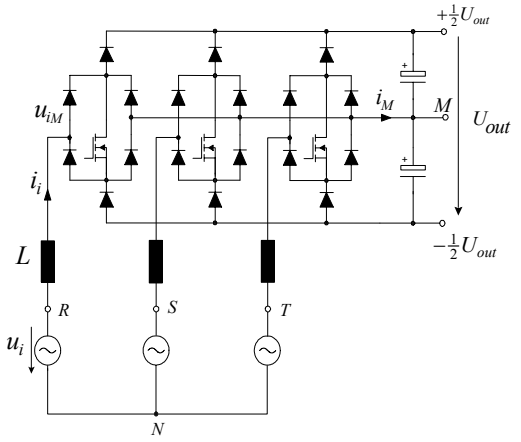

Fig. 1. Basic power circuit structure of a three-phase, three-level Vienna rectifier.

CCCs use a conventional PWM triangular carrier and linear compensator to help generate the switching signals [1]. The main advantages of CCCs are that the rectifier switches are operated at fixed frequency, which reduces the EMI filter design effort, and that the center point voltage is naturally stable. The disadvantages of CCCs are that control analysis is required to ensure system stability and a pre-control signal is required to ensure that the rectifier input current has a sinusoidal shape. In addition, the CCC has a low dynamic performance and requires additional control effort to compensate for non-idealities such as differences in the switch delay times.

In comparison, the CHC directly compares the line current with the reference current and controls the switches appropriately to force the line current to follow the reference. Hysteresis control is much easier to implement than a carrier-based controller and the transient response is extremely fast since the current instantaneously follows any change in the reference signal. However the main disadvantage is that the switching frequency is not regular as the actual switching frequency depends on the input inductor value, the hysteresis band amplitude and on the input and output voltage levels. For three-phase inverters and rectifier systems the CHC is implemented independently for each phase current. However it is well known that the switching of each phase is not independent as there is coupling or interaction between the phases [1]. This interaction can be seen in the phase current waveform (Fig. 2) where there are time intervals in which no switching action occurs, such as between 12 and 13ms in Fig. 2.

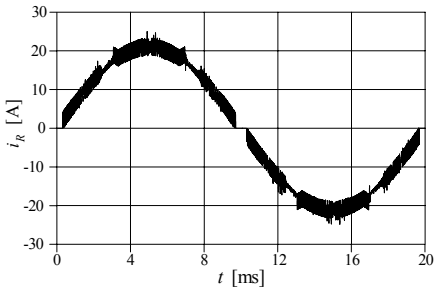

Fig. 2. Simulation of the input rectifier current for a conventional hysteresis current (CHC) controller. Simulation parameters are: $L = 450\ \mu H$, $U_{out} = 800\ V$, $\hat{U}_i = 327\ V$, $\hat{I}_i = 21\ A$.

A decoupling hysteresis controller (DHC) for three-level rectifiers has been published that removes the interaction between the phases by creating a virtual phase current [2]. The switching frequency of the DHC is now more uniform than CHC although the rms current ripple, for the same average switching frequency, is slightly higher than that produced by the CHC. This paper extends the DHC concept for three-level rectifiers so that the rectifier is operated with a constant switching frequency and that the switching of

each phase is synchronized/aligned to reduce the current ripple and achieve a phase current waveform similar to that of a CCC.

Section II of this paper presents the DHC and discusses separately the high frequency and low frequency control paths. In Section III the implementation of a variable hysteresis band to achieve a near constant switching frequency is presented. Experimental results from a Vienna rectifier operated using CHC and DHCs with and without a variable hysteresis bands are presented in Section IV. Finally in Section V a method to synchronize the switching of each of the decoupled phase controllers is presented and the input current waveform performance is shown with simulation results.

II. Decoupling Hysteresis Controller

The decoupling hysteresis controller (DHC) [2], as shown in Fig. 3, has the same basic outer structure as the standard CHC where the phase current is subtracted from a current reference and the hysteresis controller generates a switching signal from the current error. The DHC has an additional control loop that generates the current control signal, i_0. By summing the measured line current, i_i, with i_0 a virtual current i'_i is formed. With the correct formation of i_0 the switching of the hysteresis controller can occur without any interaction between each of the phase controllers. The operation of the DHC can be seen from the simulation results in Fig. 4(a) where the virtual phase current i'_R has a current ripple that is always being maintained within the hysteresis band. Fig. 4(c) shows the actual line current i_R and it can be seen that it is does not have the same current ripple as the virtual current. Compared to the phase current produced using the CHC (Fig. 2) the phase current is now being continuously switched over the complete mains period.

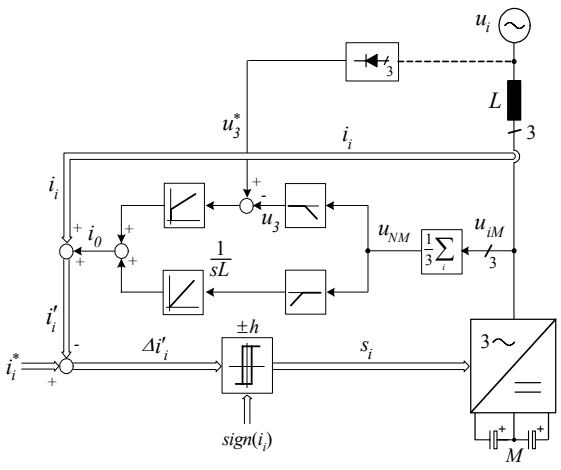

Fig 3. Decoupling hysteresis current control implementation.

The DHC has two branches to produce i_0, where the measured u_{NM} is used to produce part of i_0 through a high-pass filter and integrator and a low frequency shaping control. The high and low frequency branches are considered separately in the following sections, before being combined into a single controller.

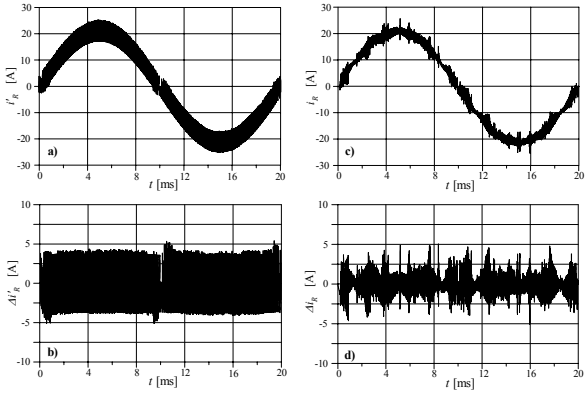

Fig. 4. Time behavior of the controlling signal i'_R **(a)** and of the mains current i_R **(c)** within one mains period in case of DHC. The respective current ripples are shown in **(b)** and **(d)**. Simulation parameters are: L = 450 µH, U_{out} = 800 V, $\hat{U}_i$ = 327 V, $\hat{I}_i$ = 21 A.

A. High Frequency Injection

The aim of the high frequency injection is to decouple the phases and avoid the interaction of the switching. The phase interaction is caused because the mid point to neutral voltage is not constant, as it is dependent on each of the rectifier input voltages as given by (1). The u_{NM} voltage is measured, either from direct measurement or by summing the input to midpoint voltages, and then high pass filtered to extract the high frequency or switching components of the voltage. From this voltage a current signal is generated by using an integrator with a gain of $1/L$, where L is the input phase inductance, as given by (2). This current signal is then summed with the actual current (as this is the controlled quantity). The high frequency components of the current i_0 now modify the measured phase current signal. This now virtually decouples each phase switching action, thus producing a regular switching that has no interference from the other phases.

$$u_{MN} = +\frac{1}{3}\left(u_{RM} + u_{SM} + u_{TM}\right) \tag{1}$$

$$i_0 = \frac{1}{L}\int_T u_{MN}\, dt \tag{2}$$

The operation of the DHC can also be explained using the equivalent circuits (Fig. 5). Fig. 5(a) shows the case where the mid-point of the two output capacitors is directly connected to the main neutral. In this case there is no mechanism for any coupling between the phases as the current, i_i, that flows in each phase is only dependent on the total voltage measured to the mid-point, u_{iM}. The fundamental current is produced by the voltage difference of the mains voltage, u_i, and the fundamental voltage at the input of the rectifier, $u_{iM,l}$. The current ripple is created from the high frequency switching voltage at the input of the rectifier.

In the case where the mid-point point is disconnected (Fig.5(b)), there is now coupling between the phases as each phase current must return via the other two phases. In terms of the equivalent circuit there are now two additional

voltage components formed because of the interaction (c.f. (1)). There is a low frequency voltage $\overline{u}_{MN}$ and a high frequency switching voltage, $u_{MN,r}$. For high frequency considerations the low frequency component is ignored. The addition of the decoupling controller now effectively shifts the switching component of u_{MN} into each of the phases (Fig.5(c)). This effectively makes the point *M''* look like it is connected to the mains neutral point and that is the reason why the high frequency switching does not have any interaction with the other phases.

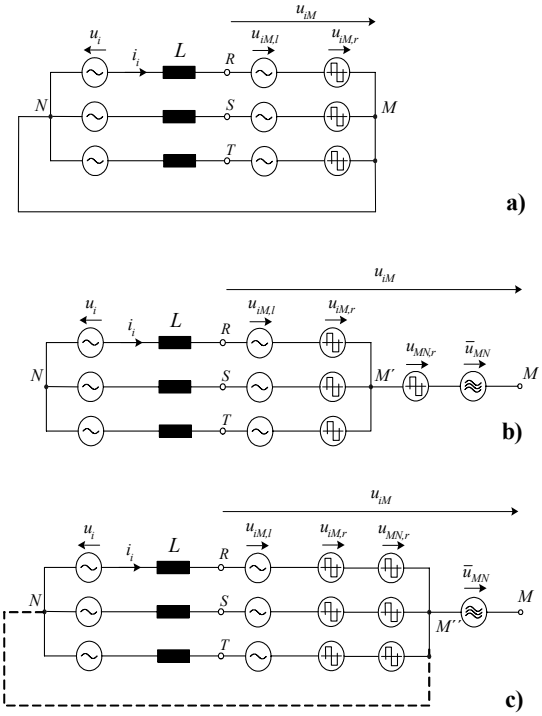

Fig 5. Equivalent circuits of DHC implementation (a) physical connection of M and N (b) DHC (c) virtual connection of M and N.

B. Low Frequency Control

From the equivalent circuit and (1) there is still a low frequency component, $\overline{u}_{MN}$, in the voltage u_{MN}. By applying a low frequency controller to the DHC system it is possible to properly shape this low frequency component. In conventional PWM systems it is desirable to add a third harmonic component to the reference so that the modulation range is extended [3]. It is also desirable to extend the modulation range for the three-level rectifier, therefore the low frequency controller is used to shape the low frequency component to be a third harmonic or zero sequence component. Fig. 3 shows the low frequency control path where the low pass filtered voltage u_{NM} is used as one input to the controller. This voltage is then compared against a reference third harmonic voltage. This reference voltage can be generated either from a 3-phase bridge rectifier connected to the mains voltage or through digital calculation [2]. The error between the reference and the measured voltage is processed by a PI controller to generate a low frequency component of current i_0 that is superimposed on to the phase currents. From [4] and [5] it is shown that i_0 at the control level causes a simultaneous change in the mid-point current and a zero sequence voltage in the input rectifier voltage. In this control case the controller produces a small change to i_0 . This control action can be represented as a feedback control diagram as shown in Fig. 6. In the case of the three-level rectifier the gain between i_0 and u_{MN} is very high. This can be seen from Fig 7(a) where the rectifier input voltage waveform now has a significant zero sequence component caused from the zero sequence voltage reference. Fig. 7(b) shows that the low frequency component of i_0 has a magnitude of 20mA while the low frequency component of $\overline{u}_{MN}$ is 80V, resulting in a gain of the order of 4000. This high gain can also be seen from the Fig.7(b) where the reference and the measured voltage are almost identical. It is interesting to note that the current i_0 has high peak values that are caused when the phase currents go through zero and that the controller is increasing its control value to maintain u_{MN} at the reference voltage level.

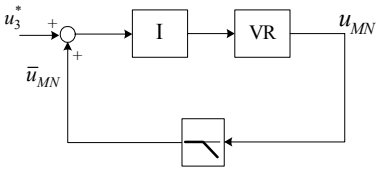

Fig. 6. Control block diagram for generation of u_{NM}.

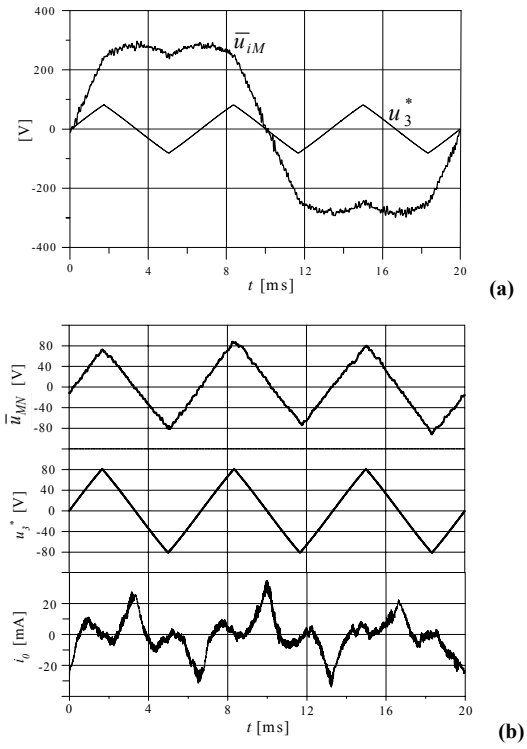

Fig. 7. Simulated time behaviour within one mains period of (a) the triangular signal u_3^* injected in the control loop to allow the extension of the rectifier modulation range and resulting low pass filtered rectifier input voltage, (b) low frequency components of u_{MN}, reference u_3^*, and i_0. Simulation parameters are: L=450µH, U_{out} = 800V, $\hat{U}_i$ = 327V, $\hat{I}_i$ = 21A.

Since the system has a very high gain between i_0 and u_{NM} it is not necessary to use the proportional part of the PI controller. Only integrator is necessary to take the error voltage and generate the controlling current. An integrator with a gain of $1/L$ is sufficient to act as a controller, therefore both the low and high frequency branches be combined together to produce a single control loop as is shown in Fig 8. This significantly reduces the complexity of the controller and does not change the performance of the system.

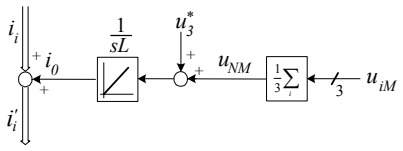

Fig 8. Combining high frequency and low frequency paths and using single integrator control.

C. Output Voltage Centre Point Control

A further advantage of the DHC compared to the CHC is that the mid-point voltage is naturally stable [2]. The bandwidth of this inherent mid-point control is determined by the system parameters and the operating point. To ensure that the control of the mid-point voltage has a defined bandwidth an additional output voltage center point controller can be added as shown in Fig. 9. The mid-point voltage is compared against a reference, which is normally half of the total output voltage, and a proportional controller produces a dc voltage, u_{dc}, from the error. This dc control voltage is added to the DHC. It has been shown in [5] that a current i_0 causes a mid-point current; therefore by adding the signal from the voltage controller to the input of the integrator it is possible to change the mid-point current. The mid-point current then causes the voltage on the capacitors to change and therefore reducing the error. The relationship between the voltage controller output u_{dc} and the average mid-point current is given in (3). Fig. 10 shows the characteristic of u_{dc} causing an average mid-point current I_M.

$$I_M = \frac{3}{\pi} \cdot \frac{2\hat{I}}{\frac{1}{2}U_{out}} \cdot u_{dc} \qquad (3)$$

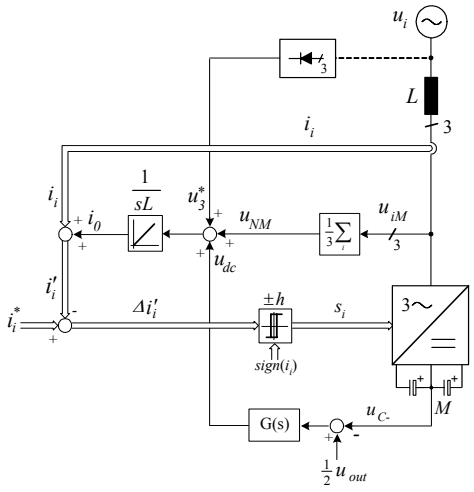

Fig 9. Output voltage center point control structure.

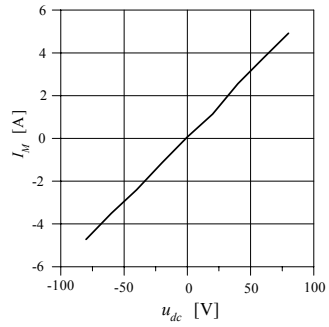

Fig. 10. Transfer characteristic from the controlling signal u_{dc} to the average mid-point current I_M.

The DHC has been shown to produce switching with no phase interactions and has inherent stability of the capacitor mid-point voltage [2]. Although DHC makes the switching frequency more regular than a CHC it is desirable to have the rectifier operating with a constant switching frequency as this makes EMI filtering task simpler. Implementing constant frequency switching in hysteresis control system, as has been shown in the literature for single and three-phase inverter systems, is achieved by varying the hysteresis band amplitude as the input voltage level changes [6,7].

III. Variable Hysteresis Band

Since the switching frequency or time the switch is on and off is dependent on hysteresis band level, voltage difference across the inductor and the inductor value the switching frequency can be kept constant by adjusting the size of the hysteresis band depending on the applied inductor voltage. Fig. 11 is used to help derive an expression for three-level systems to vary hysteresis band in order to keep the switching frequency constant. In order to derive a relatively simple expression for the hysteresis band it is assumed that during one switching period that the fundamental voltage is constant. During the positive half cycle of the mains voltage the turning on and off of the phase switch either impresses zero or half the output voltage at the input to the rectifier. When the switch is on the input rectifier voltage is zero and the current increases until the upper hysteresis band is reached. At that time the switch is turned off and the rectifier input voltage becomes ½U_{out} since the upper diode is conducting.

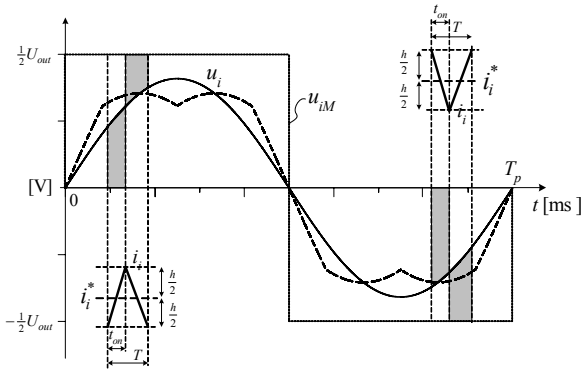

Fig. 11. Example of three-level switching waveforms

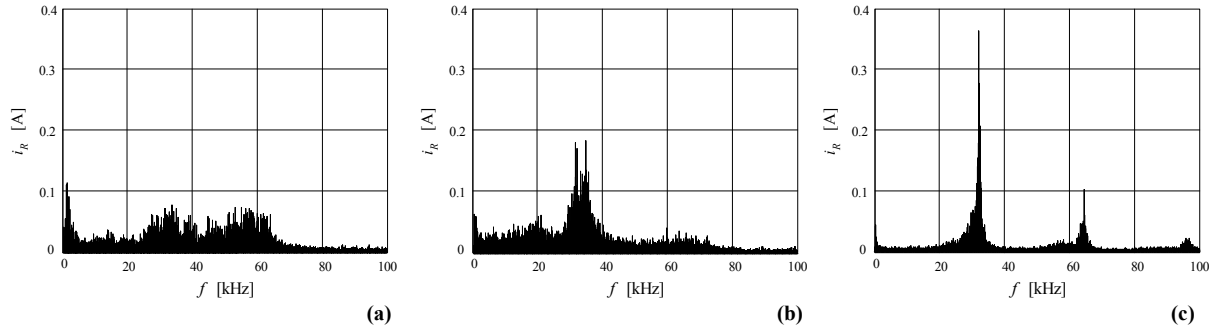

Fig. 13. Frequency spectrum of the input current, i_R, in case of (a) CHC, (b) DHC and (c) DHC with variable hysteresis band. The switching frequency is 32 kHz and the fundamental (50 Hz) is omitted.

This causes the current to decrease until the current reaches the lower hysteresis band. Together these two switching times represent one switching cycle.
By considering the positive half cycle the switching time, T, can be derived as

$$T = \frac{h \cdot L \cdot \frac{1}{2}U_{out}}{u_i\left(\frac{1}{2}U_{out} - u_i\right)} \qquad (4)$$

For the negative half cycle the switching time, T, is similarly determined. Combining the switching time equations and rearranging the hysteresis band, h, required to produce a constant frequency is expressed as

$$h = \frac{T \cdot |u_i|\left(\frac{1}{2}U_{out} - |u_i|\right)}{L \cdot \frac{1}{2}U_{out}} \qquad (5)$$

For sinusoidal input rectifier voltage, u_{iM}, the shape of the hysteresis band for one mains period is shown in Fig. 12, where the magnitude has been normalized by dividing by the peak value of the reference current. At the peak of the mains voltage the hysteresis band has to be decreased to maintain a constant frequency. The hysteresis band has to be also substantially decreased as the mains voltage approaches zero.

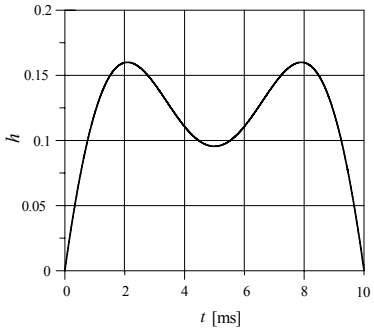

Fig. 12. Normalized hysteresis band shape for one half a mains period that allows keeping the switching frequency constant at 32 kHz. Normalized to a peak current of 1A.

Fig. 13 shows the frequency spectrum of input phase current ripple for the case of a CHC and a DHC with variable hysteresis band. In Fig. 13(a) it can be seen that the switching is occurring over a relatively wide frequency range for CHC compared to DHC with varying hysteresis band where the switching frequency is more centered around 32 kHz.

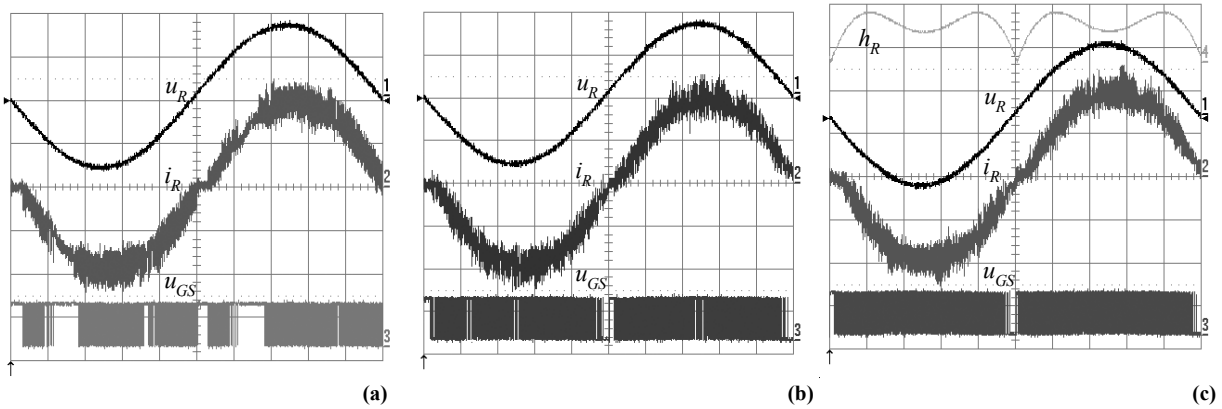

Fig. 14. (a) CHC (b) DHC with fixed hysteresis band (c) DHC with varying hysteresis band (u_R trace is 100V/div, i_R trace is 2A/div, u_{GS} is 5V/div, time base is 2ms/div). A high switching signal, u_{GS}, indicates that the switch is turned off.

IV. Experimental Analysis

The experimental evaluation of the DHC is achieved by using a Vienna Rectifier (VR) as the three-phase, three-level rectifier. The VR is connected to a three-phase 200 V rms line-to-line, 50 Hz voltage source and operated with an output voltage of 380 Vdc at an output power of approximately 1 kW. The current controller is implemented with analog circuitry to achieve accurate hysteresis current switching. The three reference currents and variable hysteresis bands are generated digitally using an Analog Devices ADSP21991 DSP, which is a 16-bit, 160MHz processor; although a standard control microprocessor could be used.

The experimental results for the CHC, DHC with a fixed hysteresis band and DHC with a varying hysteresis band are shown in Fig. 14. For CHC (Fig.14(a)) it can be seen for the R phase switching signal, u_{GS}, that there are periods where no switching occurs and the switch is turned off (a high u_{GS} indicates the switch is off). For the case of DHC with a fixed hysteresis band (Fig.14(b)) there is now more uniform switching occurring during the mains period although there is some variability in the switching frequency. For the case of DHC with a varying hysteresis band (Fig.14(c)), the shape of the hysteresis band can be seen and that the switching is more uniform.

V. Phase Switching Synchronization

The use of a variable hysteresis band produces nearly uniform switching frequency of each of the virtual phase currents. However the switching for each phase is still independent and is not coordinated in anyway. By synchronizing the switching actions of each phase to a common frequency reference an input current waveform shape similar to that produced by a CCC could be achieved. This waveform would have a reduce rms current ripple than produced by the CHC and DHC.

The synchronization and the achieving of constant switching frequency has been previously proposed [8]. In this paper the authors presented a method using a phase-locked-loop (PLL) that generated a varying hysteresis band to force the synchronization of phase switching. The switching signal was used as a one input into the Type II phase detector (PD), and a reference frequency was used as the other input. The use of the switching signal as an input to the PLL would make alignment of the switching difficult to achieve over the full range of duty cycles. This may explain why the alignment of the switching signals in Fig. 22 of [8] is not as good as that produced by CCC.

The method proposed in this paper (Fig. 15) uses a PLL and a pre-control signal for the hysteresis band, as presented in Section 3 and shown as the block that produces the signals $h_{R,S,T}$. The pre-control ensures that the switching frequency is already close to the required switching frequency. The synchronization circuit then adjusts the level of the hysteresis band to force the switching signals to become locked to a reference signal.

To reproduce a synchronized switching pattern as in CCC requires the switching signals to be centered about a common point. In this method the current error, $\Delta i'_i$ the difference between the current reference and the virtual current, is used to synchronize the switching action. Since the current error is an equally positive and negative signal, it can be compared with a zero reference to produce a 50% duty cycle logic signal. In CCC the current error signals are aligned therefore by aligning the current error logic signal with a reference signal the synchronization of the switching can be achieved. To adjust the switching of each phase a PLL is used to slightly modify the hysteresis band level. The PLL loop is implemented with a Type I (XOR) phase detector that when locked produces a 50% duty cycle output. The output of the phase detector is then low pass filtered and attenuated to produce the small change in the hysteresis band.

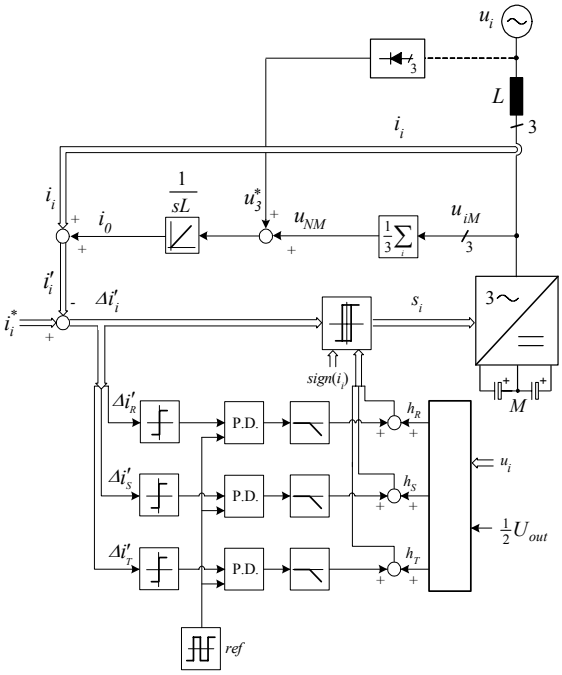

Fig. 15. Extension to DHC to synchronize the switching of each phase to produce input current waveforms similar to CCC [9].

Fig. 16 shows the waveforms generated by the synchronization control scheme. The reference signal is a 50% duty square wave. When each of the PLLs is locked, then the hysteresis bands have been modified such that the current error waveforms, $\Delta i_{R,S,T}$, are all in phase. The resulting output of the comparators, $t_{R,S,T}$, are in phase with the common reference signal. The switching signals, $s_{R,S,T}$, are also centered about the rising edge of the reference signal.

The use of a Type I XOR PD allows a simple and inexpensive implementation. The low pass filter that is designed to have a fast locking time as this should be able to track changes in less than 1 ms. The loop filter has been designed to have a cutoff frequency of 6 kHz.

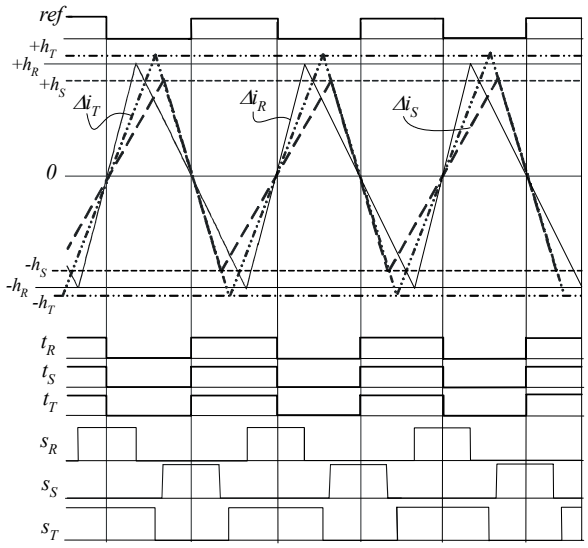

Fig. 16. Idealized waveforms produced by the DHC with synchronization.

The steady state performance of the synchronization can be seen in the phase current waveform of Fig. 17(a). The current waveform and frequency spectrum has a very similar characteristic to that produced by CCC. This shows that DHC with phase synchronization can have the advantages of both hysteresis and carrier-based current controllers. The performance of the synchronization will be experimentally verified in a future publication.

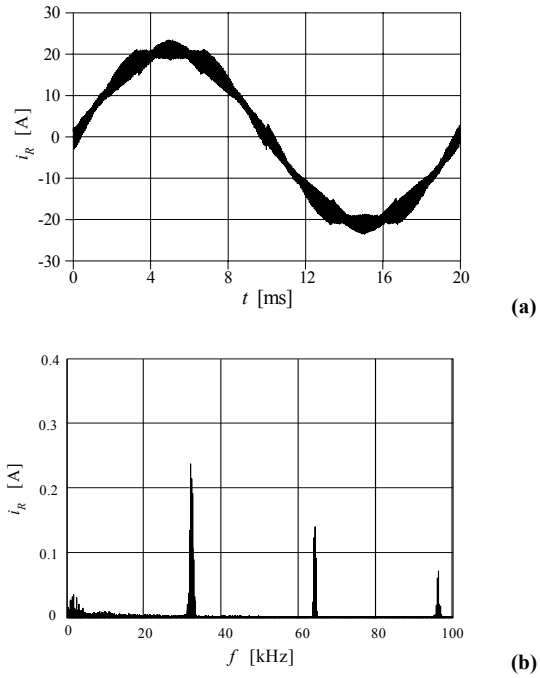

Fig. 17. Performance of DHC with synchronization. The resulting input current (a) and frequency spectrum of the ripple current (b).

VI. Conclusions

This paper has proposed an extension to the previously proposed decoupling hysteresis controller concept for three-level three-phase rectifiers takes produces a constant switching frequency and synchronized switching. The DHC takes advantage of the decoupling of the three phases by employing a virtual connection of the mains star point and the output center point in the control loop and removes the phase interaction at the control level. By using a varying hysteresis band, rather than a fixed band, the switching frequency of the rectifier can be made almost constant. The DHC control strategy with and without a varying hysteresis band has been verified through simulation and experimental implementation in a Vienna rectifier.

Through the use of a common fixed frequency reference signal and current error signal a PLL for each phase can slightly adjust the varying hysteresis band produced by the pre-controller to produce synchronized switching of all three phases. The synchronized switching produces a phase current waveform with reduced current ripple that has the same quality as achieved with conventional carrier-based controllers.

VII. References

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