Analytical Calculation of the Conduction and Switching Losses of the Conventional Matrix Converter and the (Very) Sparse Matrix Converter

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Abstract. To dimension the power semiconductors of a Conventional Matrix Converter (CMC) or a two-stage Sparse Matrix Converter (SMC and/or Very SMC) extensive simulations usually have to be performed as the losses of each device are dependent on several operating parameters, including the different ratios of input and output frequency. In this paper analytical expressions with high accuracy are derived for the switching and conduction losses of the CMC, SMC and VSMC's power semiconductors. These expressions directly show the parameter dependencies of the power semiconductor switching and conduction losses and therefore can be used to determine the maximal local or average thermal stress and for the thermal design of the power components. Furthermore, the total converter losses and conversion efficiency can be determined with minimal calculation effort.

I Introduction

Conventional Matrix Converters (CMC, cf. **Fig. 1a**) and two-stage Sparse- and/or Very Sparse Matrix Converters (SMC and/or VSMC, cf. **Fig. 1b**), which shows a reduced number of power semiconductors, are functionally equivalent [1].

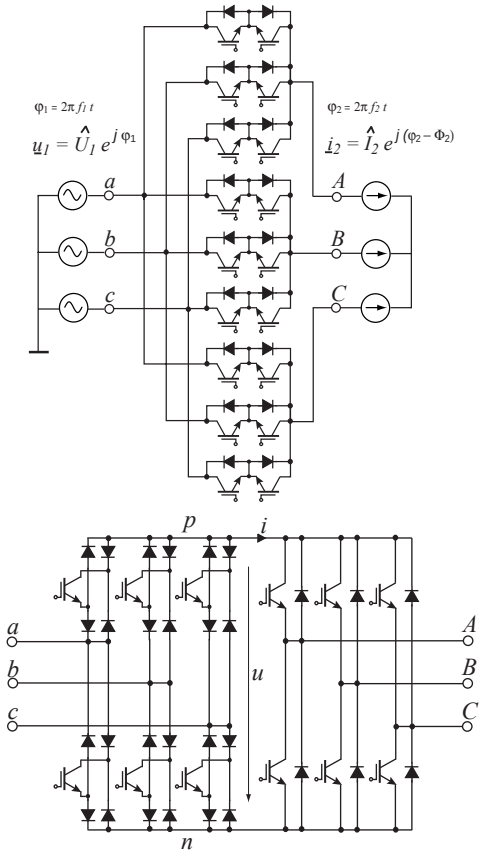


Fig. 1: Topology of the (a) Conventional Matrix Converter (CMC) and (b) Very Sparse Matrix Converter (VSMC)

The modulation method applied to the SMC and/or VSMC is illustrated in **Fig. 2**. Within each pulse half period two line-to-line voltages are switched into the DC link of the (V)SMC by proper control of the input stage. The adjustment of the output voltage amplitude is realized by the output stage only, which allows the input stage to operate without a free-wheeling interval. Moreover, the input stage commutation occurs at zero current (cf. *i* in **Fig. 2**) and this avoids the use of a multi-step commutation scheme that is dependent on the sign of the commutating voltage or current as is required for the CMC. However, the pulse pattern depicted in Fig. 2 can be directly transferred to the CMC resulting in the corresponding virtual DC link quantities u_{CMC} and i_{CMC} [6]. This allows a direct comparison of both topologies.

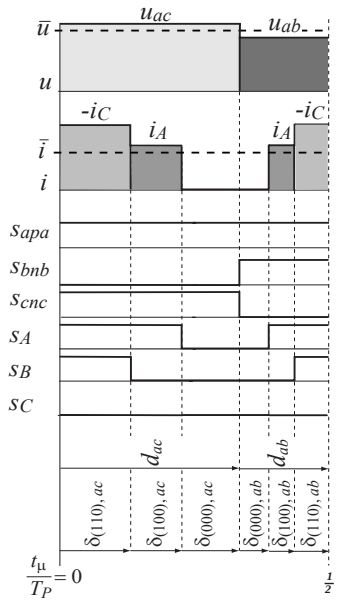


Fig. 2: Time behaviour of the DC link quantities u ,i and of the corresponding pulse pattern for the SMC and/or VSMC within $\varphi_1 \in [-\pi/6, \pi/6]$; $\varphi_2 \in [\pi/6, \pi/3]$ for a pulse half period. Switching state changes of the rectifier stage occur at zero DC link current. The pulse pattern can be directly transferred to the CMC resulting in an analogous virtual DC link voltage and current [6].

For conventional modulation of a SMC (being equivalent to indirect or virtual DC link modulation of a CMC), the relative turn-on times of the single switching states [1-3] e.g. for φ_1 in $-\pi/6$ …$+\pi/6$ and φ_2 in 0…$+\pi/3$ (as given in Fig.2) are

$$\begin{aligned} d_{ab} &= \cos(\varphi_1 + \pi/3) \\ d_{ac} &= \cos(\varphi_1 - \pi/3) \\ \delta_{(100)} &= M_{12} \cdot \cos(\varphi_2 + \pi/6) \\ \delta_{(110)} &= M_{12} \cdot \sin(\varphi_2) \end{aligned} \qquad (1)$$

$$\begin{aligned}\delta_{(100),ac} &= d_{ac}\cdot\delta_{(100)}\\ \delta_{(110),ac} &= d_{ac}\cdot\delta_{(110)}\\ \delta_{(110),ab} &= d_{ab}\cdot\delta_{(110)}\\ \delta_{(100),ab} &= d_{ab}\cdot\delta_{(100)}\end{aligned} \quad (2)$$

with

$$M_{12} := \frac{2}{\sqrt{3}}\frac{\hat{U}_2}{\hat{U}_1} \quad (3)$$

The switching state of the (V)SMC rectifier stage is determined by the two input phases, which are connected to the positive (p) and negative (n) DC link bus. For example,

$$s_{\mathrm{Re}ct} = (p;n) = (ac) \quad (4)$$

is valid for the first rectifier state of the pulse sequence shown in Fig. 2. Thereby, the actual rectifier switching state matrix

$$\underline{S}_{\mathrm{Re}ct} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix} \quad (5)$$

is represented by s_{Rect} in a very compact way. Analogously, the switching state of the (V)SMC inverter stage is described by the switching states of the three transistors being connected to the p-bus bar. For example, the first inverter switching state of the depicted pulse period can be represented by

$$s_{Inv} = \begin{pmatrix} s_A & s_B & s_C \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 \end{pmatrix}, \quad (6)$$

instead of the inverter switching state matrix

$$\underline{S}_{Inv} = \begin{pmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix}. \quad (7)$$

Considering (5) and (7) the output to input current transfer follows as

$$\underline{i}_{abc} = \underline{S}^T_{Rect}\,\underline{S}_{Inv}\cdot\underline{i}_{ABC}, \quad (8)$$

which has to be equal to the single-stage CMC switching state matrix for the same connections between the output (A,B,C) and input (a,b,c) terminals. This yields

$$\underline{S}_{CMC} = \underline{S}^T_{Rect}\,\underline{S}_{Inv}. \quad (9)$$

which directly provides the switching state correspondence of CMC and (V)SMC as shown in Fig. **4a.**

In this paper the basic considerations concerning the modeling of the time behavior of the switching and conduction loss components of the CMC and the (V)SMC are proposed. In a first step both loss components are calculated as an average over a single pulse period and will be denominated as local losses. Those local losses are again averaged over a whole mains fundamental period in a second step. Considering the converter system, as in a standard application feeding a synchronous or asynchronous motor, the maximum of the resulting loss term in φ_2 becomes relevant for operating points close to standstill. Finally, a last averaging over a entire load fundamental period yields the loss value that is relevant for the dimensioning of the semiconductors when operating at output frequencies larger than 5Hz and for the heat sink dimensioning in general. This last averaged value is the most significant and will be referred to as the global loss in the paper. This approach leads to formulas that accurately describe the global average losses and therefore provides a reliable basis for the thermal dimensioning of the power semiconductors and the heat sink.

In **Section II** the switching losses of CMC and (V)SMC are investigated. There the analytical considerations focus on the CMC and are proven by a digital simulation of a switched model. **Section III** is dedicated to the analytical description of the conduction losses. The main focus is on the CMC for which global average conduction loss formulas of general validity can be derived with low effort. In order to demonstrate the usage of the proposed equations in the design process a simple dimensioning example is given in **Section IV.**

II SWITCHING LOSSES

For calculating the energy loss of one single switching action that has dependency on the switched voltage and current a polynomial approach, using (10), is used.

$$w(u,i) = K_1 ui + K_2 ui^2 + K_3 u^2 + K_4 u^2 i + K_5 u^2 i^2 \quad (10)$$

The parameters K_i are derived from a least square approximation of measured data (cf. [9]) and are compiled in **Tab. 1** for a specific power transistor / power diode combination (IXYS FII50-12E).
It should be mentioned that (10) considers all physically reasonable terms of the switched voltage u and current i. It is also possible to neglect some of the terms while approximating the measured losses in order to simplify the mathematical expression. This would also simplify the expressions describing the global power semiconductors losses, which provide the dimensioning basis and will be given in the following section.

IGBT-Switching Loss Parameter					
	K_1	K_2	K_3	K_4	K_5
$T_{on\rightarrow off}$	179	-1.31	$650\ 10^{-3}$	$-116\ 10^{-3}$	$3.48\ 10^{-3}$
$T_{off\rightarrow on}$	70.0	2.94	$518\ 10^{-3}$	$102\ 10^{-3}$	$-1.55\ 10^{-3}$
$D_{on\rightarrow off}$	97.9	-3.73	$488\ 10^{-3}$	$140\ 10^{-3}$	$4.27\ 10^{-3}$
	$\mathrm{nWs(VA)^{-1}}$	$\mathrm{nWs(VA^2)^{-1}}$	$\mathrm{nWs(V^2)^{-1}}$	$\mathrm{nWs(V^2A)^{-1}}$	$\mathrm{nWs(V^2A^2)^{-1}}$

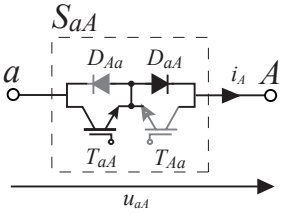
Tab. 1: Coefficients $K_1 \ldots K_5$ derived by least-square approximations of measured IGBT / free-wheeling diode (IXYS FII50-12) switching losses for a junction temperature of T_J=120°C (cf. [9]).

II.A CONVENTIONAL MATRIX CONVERTER (CMC)

For a switching action of the CMC, two bidirectional switches connected to the same output terminal are subject to losses. Considering a particular switching sequence of a full pulse period, each switching action of a switch in the first pulse half period is followed by an inverse switching action under same conditions within the second half of the pulse period (assuming $f_P \rightarrow \infty$, so that the ripple components of voltages and currents are neglected). Accordingly, the turn-on and turn-off energy of a certain switch can be added as given by

$$w_{onoff}(u,i) = w_{on}(u,i) + w_{off}(u,i). \quad (11)$$

As illustrated in **Fig. 3a,** the switching losses for the bidirectional switch S_{aA} are dependent on the output phase current i_A and the input line-to-line voltage determined from the two input phases involved in the switching actions ($u_{aA} = u_{ab}$ or $u_{aA} = u_{ac}$). The switching losses of switch cell S_{aA} only occur in one of the four semiconductors, which is dependent on the signs of u_{aA} and i_A (cf. **Fig. 3b**).



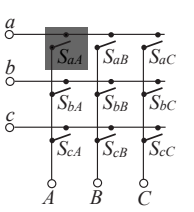
	$u_{aA} > 0$	$u_{aA} < 0$
$i_A > 0$	T_{aA}	D_{aA}
$i_A < 0$	D_{Aa}	T_{Aa}

(a) (b)

Fig. 3: (a) Schematic and notations of the bidirectional switch cell S_{aA}. The semiconductor being subject to switching losses is determined by the sign of the switched voltage u_{aA} and switched current i_A (cf. **(b)**).

For analyzing the switching actions of each bidirectional CMC switch within a certain pulse half period, a switching table (given in **Fig. 4)** is used that gives the CMC switching state matrix (9) for the different intervals of a pulse half period. This table corresponds to the pulse pattern shown in Fig. **2** and is valid for angles $\varphi_1 = \omega_1 t \in [-\pi/6, \pi/6]$ and $\varphi_2 = \omega_2 t \in [\pi/6, \pi/3]$. It visualizes how often a certain switch is changing its state within the pulse half period. Furthermore, it allows a direct determination of the switched

voltage u_{aA}. Analogous tables have to be created for three further combinations of angle intervals (φ_1 ,φ_2), which allows the behavior of each bidirectional switch within a full mains and load period (from symmetry considerations) to be determined.



$s_{SMC,Rect}$	(ac)			(ab)		
$s_{SMC,Inv}$	(110)	(100)	(000)	(000)	(100)	(110)
$\underline{S}_{CMC}$	1 1 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1 1	0 0 0 0 0 0 1 1 1	0 0 0 1 1 1 0 0 0	1 0 0 0 1 1 0 0 0	1 1 0 0 0 1 0 0 0
$\delta_{110}+\delta_{100}+$ $+\ \delta_{000}=1$	δ_{110}	δ_{100}	δ_{000}	δ_{000}	δ_{100}	δ_{110}
$d_{ac}+d_{ab}=1$	d_{ac}			d_{ab}		

(a) (b)

Fig. 4: (a) Schematic of the CMC with ideal switches. **(b)** Switching states of the CMC and (V)SMC for a pulse half period with the relative on-times (for $\varphi_1 \in [-\pi/6, \pi/6]$; $\varphi_2 \in [\pi/6, \pi/3]$).

The local switching losses are finally calculated by adding up all energy losses $w_{onoff}(u, i)$ for a pulse period and multiplying the sum with the switching frequency f_p .

$$p_{Sw} = f_P w_{\Sigma onoff} \tag{12}$$

This results, in combination with the aforementioned symmetry considerations, in the switching loss characteristic depicted in **Fig. 5** for the transistors T_{aA} and $T_{Aa.}$ (valid for $\Phi_2 = 0$). There, the φ_2 coordinate indicates a position within the output voltage fundamental period, while the φ_1 coordinate indicates a position within the input voltage period. The symmetry of the losses occurring in the forward (T_{aA})- and reverse transistor (T_{Aa}) caused by the sinusoidal load current i_A is obvious. It is important to note that the switching loss characteristic consists of several different segments, therefore it is not a trivial exercise to find a general analytic expression providing the global average of that characteristic for varying output current and voltage displacement angles Φ_2.

Unlike the (V)SMC where switching losses only occur in the inverter stage (the rectifier stage does not show switching losses, since it is switched at zero DC-link current), the CMC switching losses do occur during the switching of the virtual rectifier stage (e.g. all losses occurring for $\varphi_2 \in [-\pi/6, \pi/6]$; cf. Fig. **5**).

Depending on the ratio of output frequency f_2 and input frequency f_1 the (linear) trajectory of the operating point ($\varphi_2=2\pi f_2 t$, $\varphi_1=2\pi f_1 t$) in the φ_2 -φ_1 plane will show a characteristic slope and results in a corresponding variation of the local losses (cf. [9]).

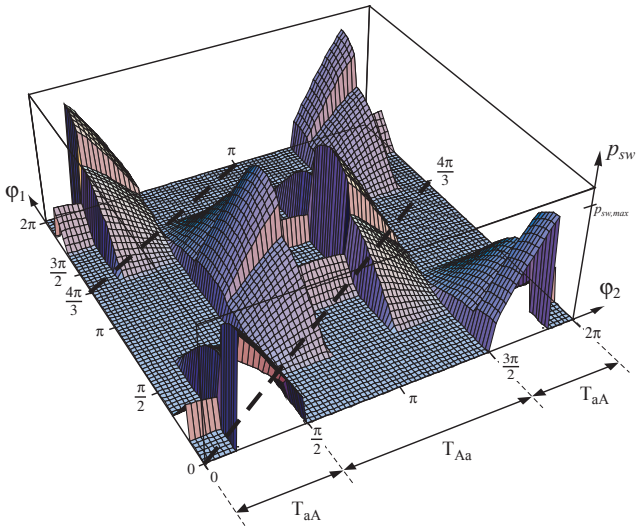


Fig. 5: Local switching losses of transistors T_{aA} and T_{Aa} forming switch S_{aA} of the CMC for $\Phi_2 = 0$. The diodes D_{aA} and D_{Aa} also show a qualitatively similar characteristic that is displaced by π rad in φ_1 or φ_2-direction.

Fig. 6 shows the switching losses resulting for such a characteristic slope for the operating point: $f_1 = 50$Hz; $f_2 = 75$Hz; $\Phi_2 = 0$ within a time interval of 20ms. The depicted graph could be seen as profile resulting from cutting the 3D characteristic given in Fig.5 along a (φ_1, φ_2) = (0, 0) → (4π/3, 2π) → (4π/3, 0) → (2π, π) axis. Also included in Fig. 6 are the results from a numerical simulation (SIMPLORER) using a switching CMC model and it provides an identical result and clearly verifies the analytical approach.

II.A.1 GLOBAL LOSSES

The global average switching loss for one semiconductor is most relevant for its dimensioning and can be derived by averaging over the whole φ_1 -φ_2 plane (13). Extensive simulations have proven that this value differs by less than 3% from the exact average values gained for an extremely wide variety of different operating points, each with a characteristic time behavior, such as the one in Fig. 6.

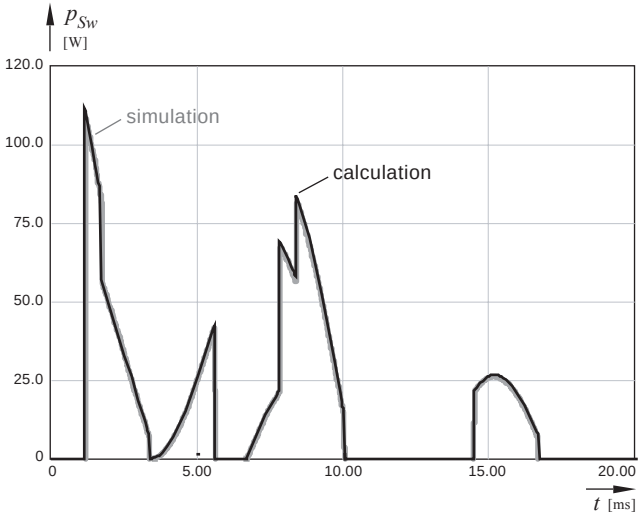


Fig. 6: Comparison of the analytically calculated and the simulated (switched CMC model) switching losses of the CMC transistors T_{aA}, T_{Aa} of $f_1 = 50$Hz; $f_2 = 75$Hz; $M = 1$; $\Phi_2 = 0$.

$$\begin{aligned} P_{Sw,T/D} = {} & \frac{f_P \hat{U}_1}{96\pi^2}\Big(22\Big(2K_3 + K_5\hat{I}_2^2\Big)\pi^2\hat{U}_1 + 12\hat{I}_2\Big(12K_1 + \sqrt{3}(8K_1 + 3K_4\hat{U}_1)\Big) + \\ & + 3\pi\Big(4\hat{I}_2(\hat{I}_2K_2 + 10K_4\hat{U}_1) + \sqrt{3}(2K_3\hat{U}_1 + \hat{I}_2^2(8K_2 + K_5\hat{U}_1))\Big) - \\ & - 12\hat{I}_2\Big(12K_1 + K_4(3\sqrt{3} + 4\pi)\hat{U}_1\Big)\cos\Phi_2 - \\ & - 3\hat{I}_2^2\Big(12\sqrt{3}K_2 + \hat{U}_1K_5(9 + 4\sqrt{3}\pi)\Big)\cos(2\Phi_2)\Big) \end{aligned} \tag{13}$$

This equation is valid for all semiconductors of the CMC (assuming $\Phi_2 \in [-\pi/3, \pi/3]$ or $\Phi_2 \in [2\pi/3, 4\pi/3]$), where the substitution

$$K_i \rightarrow K_{i,Ton} + K_{i,Toff} \tag{14}$$

can be used for the transistors and

$$K_i \rightarrow K_{i,Doff} \tag{15}$$

for the diodes. Since the polynomial (10) depends linearly on the coefficients K_i, the switching losses of the whole converter can be calculated by the substitution

$$K_i \rightarrow 18(K_{i,Ton} + K_{i,Toff} + K_{i,Doff}) \,. \tag{16}$$

As mentioned above, (13) could be simplified by considering a reduced number of polynomial coefficients of (10).

II.A.2 MAXIMUM IN φ_2

Besides the global average value of the switching losses, their local maxima are also relevant for the semiconductor dimensioning. Since there is a thermal transient impedance of the semiconductor device (which physically can be characterized by a thermal time

constant $\tau_{th}=R_{th}\,C_{th}$) the areas of maximum switching losses in Fig.5 should be averaged over τ_{th}. This yields relevant local loss values, being directly responsible for the temperature rise of the junction with reference to the heat sink ($\Delta T=p\,R_{th}$). As a consequence the converter has to be designed in order to keep the local junction temperature below the tolerable maximum value at any time (i.e. for any φ_1,φ_2) and for every operating point. Therefore, knowledge of the value τ_{th} is of special importance in order to determine physically reasonable averaging intervals. First results from extensive thermal simulations reveal an equivalent time constant of τ_{th} = 60…80ms for the IXYS FII50-12E / FIO50-12BD modules. When considering a mains frequency of f_1=50…60Hz, the relatively large value of τ_{th} clearly justifies averaging over a whole mains period. As a result the losses depend, mathematically, only on φ_2. This means for very low output frequencies, $f_2 \le 5$Hz, the maximum loss value in φ_2 becomes relevant. Graphically this operating point corresponds to a trajectory within the φ_1 -φ_2 plane of Fig.5 running approximately in parallel to the φ_1 axis.

The local loss maximum in φ_2 is relevant for dimensioning a converter system operating with very low output frequencies (and/or motor speed close to standstill) and is gained from

$$\hat{\tilde{P}}_{Sw,T/D}(\varphi_2) = \\ = \frac{f_P}{16\pi}\left(12\left(3+2\sqrt{3}\right)\left(K_1 i_{Sw}+K_2 i_{Sw}^2\right)\hat{U}_1+3\left(3\sqrt{3}+10\pi\right)\left(K_3+K_4 i_{Sw}+K_5 i_{Sw}^2\right)\hat{U}_1^2\right) \quad (17)$$

with

$i_{Sw} = \hat{I}_2\, cos(\Phi_2-\pi/6)$ for $\Phi_2 \in [0, \pi/6]$ [1]

$i_{Sw} = \hat{I}_2$ for $\Phi_2 \in [\pi/6, \pi/2]$.

II.B (VERY) SPARSE MATRIX CONVERTER (VSMC)

Due to the zero current switching of the (V)SMC input stage the relevant switching losses occur only in the output stage. **Fig. 7** shows the bridge leg A of the inverter stage.

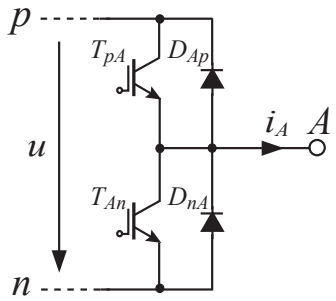


Fig. 8: Semiconductors in bridge leg A of VSMC Inverter-Stage.

Within the intervals $\varphi_2 \in [-\pi/6, \pi/6] \cup [5\pi/6, 7\pi/6]$ the bridge leg A is clamped either to the p-bus bar or to the n-bus bar and therefore is not producing any switching losses. For $\varphi_2 \in [\pi/6, 5\pi/6]$ the phase current i_A is positive ($i_A > 0$) and thus causes losses in transistor T_{pA} and the corresponding free-wheeling diode D_{nA}. For $\varphi_2 \in [7\pi/6, 11\pi/6]$ the negative phase current ($i_A < 0$) leads to switching losses in T_{An} and D_{Ap}. Both transistors T_{pA} and T_{An} are switched on and off twice during one pulse period. The two DC link voltages that are switched during one pulse period are given for the general case with u_μ and u_ν (and correspond to u_{ac} and u_{ab} in Fig.2). Summing the turn-on- and turn-off losses (11) results in the local losses which are given by

$$p_{Sw} = f_P\left(w_{onoff}(u_\mu, i_A) + w_{onoff}(u_\nu, i_A)\right) \quad (18)$$

with

$$u_\mu = \sqrt{3}\hat{U}_1 \cos(\theta_1 + \pi/6) \quad (19)$$

$$u_\nu = \sqrt{3}\hat{U}_1 \cos(\theta_1 - \pi/6) \quad (20)$$

$$\theta_1 = (\varphi_1 + \pi/6) \bmod \pi/3 - \pi/6\,. \quad (21)$$

The resulting switching loss characteristic of the (V)SMC inverter stage is shown in **Fig. 9**.

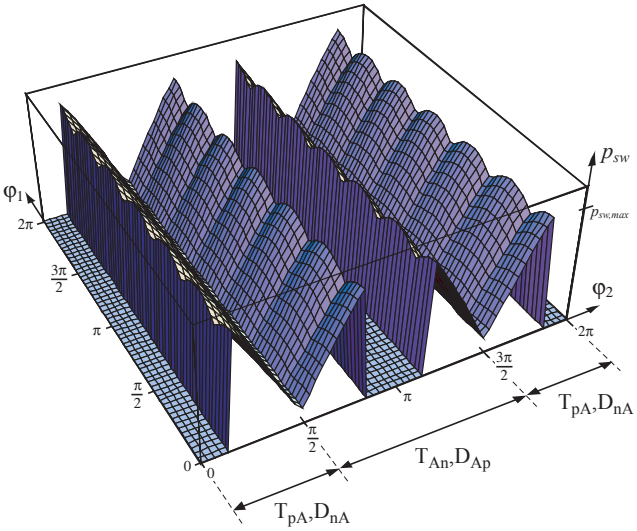


Fig. 10: Local switching losses of bridge leg A of the VSMC inverter stage for the four power semiconductors ($\Phi_2 = 0$).

II.B.1 GLOBAL LOSSES

Averaging over the whole φ_1 -φ_2 plane of Fig.8 leads to the global average value of the (V)SMC switching losses. For a single power semiconductor the global average value is

$$P_{Sw,T/D} = \frac{f_P\hat{U}_1}{32\pi^2}\left(48\hat{I}_2\left(6K_1+K_2\hat{I}_2\pi\right)+4\hat{U}_1(3\sqrt{3}+4\pi)\left(6K_4\hat{I}_2+2\pi K_3+\pi K_5\hat{I}_2^2\right)\right)- \\ -12\hat{I}_2\left(12K_1+K_4(3\sqrt{3}+4\pi)\hat{U}_1\right)\cos\Phi_2 - \\ -3\hat{I}_2^2\left(12\sqrt{3}K_2+\hat{U}_1K_5(9+4\sqrt{3}\pi)\right)\cos(2\Phi_2)\Big) \quad (22)$$

Again, the switching losses caused by the entire converter system are obtained with the following substitution

$$K_i \to 6(K_{i,Ton} + K_{i,Toff} + K_{i,Doff}) \quad (23)$$

II.B.2 MAXIMUM IN φ_2

Analogously to Section II.A.2 the local switching loss maximum in φ_2, which is relevant for very low output frequencies only, can be derived from the formula

$$\hat{\tilde{P}}_{Sw,T/D}(\varphi_2) = \\ = f_P\left(\left(K_1 i_{Sw}+K_2 i_{Sw}^2\right)\frac{9}{\pi}\hat{U}_1+\left(K_3+K_4 i_{Sw}+K_5 i_{Sw}^2\right)\left(\frac{9\sqrt{3}}{4\pi}+3\right)\hat{U}_1^2\right) \quad (24)$$

with

$i_{Sw} = \hat{I}_2\, cos(\Phi_2-\pi/6)$ for $\Phi_2 \in [0, \pi/6]$ [2]

$i_{Sw} = \hat{I}_2$ for $\Phi_2 \in [\pi/6, \pi/2]$.

[1] With a conventional output stage clamping strategy being applied. Applying an adapted strategy would lead to $i_{Sw} = \sqrt{3}/2\,\hat{I}_2$ for $\Phi_2 \in [0, \pi/6]$.

[2] With a conventional output stage clamping strategy being applied. Applying an adapted strategy would lead to $i_{Sw} = \sqrt{3}/2\,\hat{I}_2$ for $\Phi_2 \in [0, \pi/6]$.

III CONDUCTION LOSSES

III.A CONVENTIONAL MATRIX CONVERTER (CMC)

III.A.1 GLOBAL LOSSES

An analytical expression for the global conduction losses of the CMC semiconductors can also be derived with low calculation effort. According to the system symmetries, the current stresses on the three bidirectional switches S_{aA}, S_{bA} and S_{cA} connected to the output A are equal and determined by output phase current i_A. The sign of the phase current determines the current conducting transistor/diode pair of a switch. Therefore, the output phase current i_A has to be split into a positive and a negative component (cf. **Fig.7**), where, for example, the semiconductors T_{aA} and D_{aA}, are only stressed by the positive component i_A^+ (cf. Fig. 3).

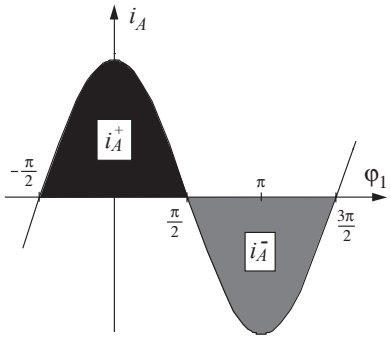


Fig. 11: Illustration of the positive and negative components i_A^+ and i_A^- of the output phase current i_A for an output displacement angle of $\Phi_2 = 0$.

Since all power semiconductors of the CMC show equal current stresses the global average current and the rms current of the semiconductors can be derived, as for the case of transistor T_{aA}

$$\bar{I}_A^+ = \frac{1}{2\pi}\int_0^{2\pi} i_A^+ d\varphi_2 = \frac{1}{2\pi}\int_{-\pi/2+\Phi_2}^{\pi/2+\Phi_2} \hat{I}_2 \cos(\varphi_2 - \Phi_2)\, d\varphi_2 = \frac{\hat{I}_2}{\pi} = \bar{I}_A^- \tag{25}$$

$$\bar{I}_{TaA} = \frac{1}{3}\bar{I}_A^+ = \frac{\hat{I}_2}{3\pi} \tag{26}$$

$$I_{TaA,rms}^2 = \frac{1}{3}\frac{1}{2\pi}\int_0^{2\pi} {i_A^+}^2 d\varphi_2 = \frac{\hat{I}_2^2}{12}. \tag{27}$$

Finally, the formula for the global conduction losses of one semiconductor results as

$$P_C = U_F \frac{\hat{I}_2}{3\pi} + r\frac{\hat{I}_2^2}{12} \tag{28}$$

Typical on-state parameters u_F and r are given in **Tab. 2**. Since the global conduction losses are only determined by the converter topology the result is independent of the modulation concept used, and is independent of the modulation index M and the output phase displacement angle Φ_2. With the substitutions

$$\begin{aligned} u_F &\rightarrow 18(U_{F,Transistor} + U_{F,Diode}) \\ r &\rightarrow 18(r_{Transistor} + r_{Diode}) \end{aligned} \tag{29}$$

the global conduction losses of the entire converter system can be calculated.

Digital simulations again verify (28) showing an excellent correspondence. Analytically obtained values differ less than 5% from the exact average values gained by a numerical simulation of a switched CMC model for a wide variety of different operating points.

On-State Parameters		
	U_F	r
Transistor	768	78.7
Diode	732	38.0
	mV	mVA^{-1}

Tab. 2: On-state parameters of the power transistor and diode of the power module IXYS FII50-12E for a junction temperature of T_j=120°C.

III.A.2 LOCAL LOSSES AND MAXIMUM IN φ_2

For the calculation of the local power losses, an exact analysis of the semiconductor currents is required. The current stresses are dependent on the position within the input and output voltage period (φ_1, φ_2). Therefore, in a first step the relative turn-on-time d_{aA} of a switch, e.g. S_{aA}, has to be determined.

If the angle values (φ_1, φ_2) are located in the interval $\varphi_1 \in [-\pi/6, \pi/6]$; $\varphi_2 \in [\pi/6, \pi/3]$ (cf. Fig. 4b), the rectifier states (ac), (ab) and the inverter states (110), (100), (000) are switched within a pulse period. Hence, the switch S_{aA} is only blocking while the zero state (000) is active. So, employing (1) the relative turn-on time can be calculated as follows

$$\begin{aligned} d_{aA} &= d_{ac}(\delta_{110} + \delta_{100}) + d_{ab}(\delta_{110} + \delta_{100}) \\ &= M_{12}\cos\varphi_1 \cos(\varphi_2 - \pi/6) \end{aligned} \tag{30}$$

By analogous calculations the relative turn-on time of the switch S_{aA} can be derived for the entire plane $\varphi_1 \in [0, 2\pi]$; $\varphi_2 \in [0, 2\pi]$. Due to the symmetry of the converter topology, the relative turn-on time for the other switches can be obtained directly by introducing displacements of $\pm 2\pi/3$ in φ_1 and/or φ_2 direction. The local conduction losses can be derived from the relative turn-on time

$$p_C = d_{aA}(u_F i_A + r\, i_A^2) \tag{31}$$

and are depicted in **Fig. 12** for the power semiconductors of switch S_{aA} with an operating point of $M = 1$, $\Phi_2 = 0$.

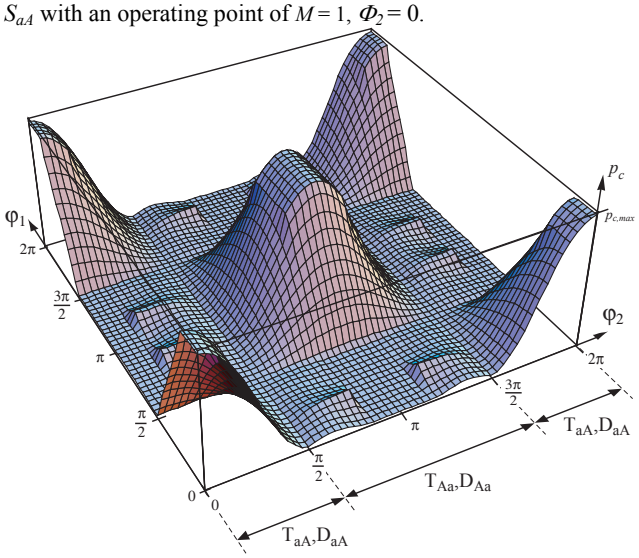


Fig. 12: Local conduction losses of switch S_{aA} (CMC) for the operating point $M = 1$, $\Phi_2 = 0$. Dependent on the sign of the phase current i_A, the losses occur in the transistor/diode-pair T_{aA}/D_{aA} or T_{Aa}/D_{Aa}.

After averaging p_C over the entire mains period ($\varphi_1 \in [0, 2\pi]$) the resulting conduction loss maximum in φ_2 is given by

$$\hat{\bar{p}}_{C,T/D} = \frac{1}{3}(u_F \cdot \hat{I}_2 + r \cdot \hat{I}_2^{\,2}) \tag{32}$$

for any power semiconductor (independent of modulation and phase displacement Φ_2). This result is also plausible with respect to Fig.4a. Assuming a very low output frequency the output phase current value will remain on an almost constant level. In the worst case one of the three output terminals is loaded with the maximum value (current amplitude $\hat{I}_2$). During one mains period this current is distributed equally to all three switches being connected to that output terminal. As a consequence the resulting conduction losses are also shared by the three transistors/diodes.

III.B (VERY) SPARSE MATRIX CONVERTER ((V)SMC)

III.B.1 INVERTER STAGE

Global Losses

An exact analytical calculation [4] yields the global conduction losses for the (V)SMC output stage transistors

$$P_{C,Inv,T} = u_{F,T} \cdot \hat{I}_2 \frac{2+\sqrt{3}M_{12}\cos\Phi_2}{4\pi} + r_T \cdot I^2{}_{Inv,T,rms}\,, \quad (33)$$

and for the diodes

$$P_{C,Inv,D} = u_{F,D} \cdot \hat{I}_2 \frac{2-\sqrt{3}M_{12}\cos\Phi_2}{4\pi} + r_D \cdot I^2{}_{Inv,D,rms} \quad (34)$$

with the squared rms values

$$I^2{}_{Inv,T,rms} = \hat{I}_2{}^2 \frac{2\pi + 6\Phi_2 + (8M_{12}-6)\sin(2\Phi_2 - \frac{\pi}{3}) - 16M_{12}\sin(\Phi_2 - \frac{\pi}{3})}{24\pi}$$

and

$$I^2{}_{Inv,D,rms} = \hat{I}_2{}^2 \frac{4\pi - 6\Phi_2 - (8M_{12}-6)\sin(2\Phi_2 - \frac{\pi}{3}) + 16M_{12}\sin(\Phi_2 - \frac{\pi}{3})}{24\pi}.$$

The conduction losses of the entire inverter stage can be directly calculated by

$$P_{C,Inv,(V)SMC} = 6 \cdot (P_{C,Inv,T} + P_{C,Inv,D})\,. \quad (35)$$

Local Losses and Maximum in φ_2

The procedure to determine the local conduction losses of the inverter stage is similar to that described in Section III.A.2 for the CMC. The relative turn-on time of the transistors can be derived and has to be weighted with the corresponding output phase current value in order to get a local current average and rms value. With the given on-state parameters those values lead to the local conduction losses. The results are visualized in **Fig. 13**.

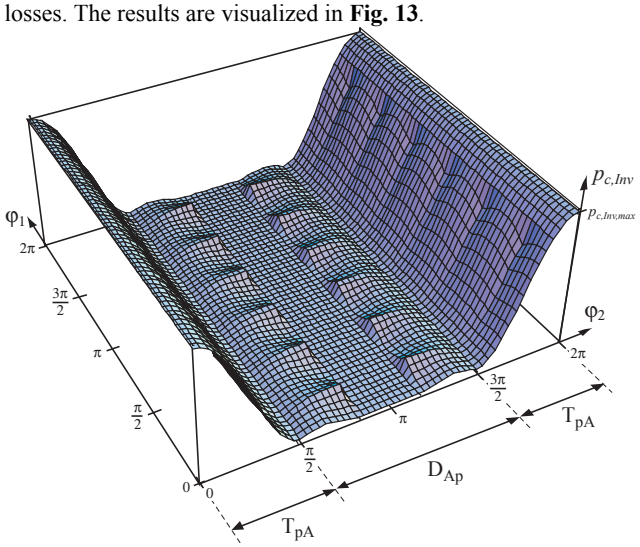


Fig. 13: Local conduction losses of the inverter stage transistor T_{pA} and diode D_{nA} ($M_{12} = 1$, $\Phi_2 = 0$).

The local conduction loss maximum in φ_2 that is relevant for operation at very low output frequencies can be given independently from M_{12} and Φ_2 as (cf. (32))

$$\hat{\bar{p}}_{C,Inv,T/D} = u_F \cdot \hat{I}_2 + r \cdot \hat{I}_2{}^2\,. \quad (36)$$

III.B.2 RECTIFIER STAGE

The denomination of the power semiconductors is given in **Fig. 14** for the rectifier stage topologies of VSMC and SMC.

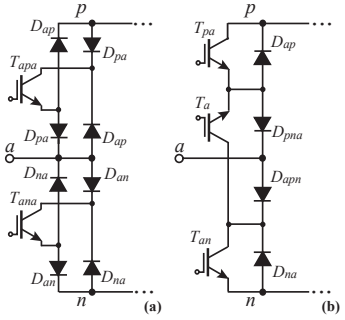


Fig. 12: Diode and power semiconductor structure of a rectifier bridge leg for a VSMC (a) and SMC (b).

Global Losses for $\Phi_2 \in [0, \pi/6]$

The global conduction losses of the rectifier stages can be calculated according to [4]. The results for the output phase displacement interval $\Phi_2 \in [0, \pi/6]$ (which is the relevant one for dimensioning issues) are given as

$$\bar{I}_{Tapa} = \frac{\sqrt{3}}{2\pi}\hat{I}_2 \cdot M_{12} \cdot \cos\Phi_2 \quad (37)$$

$$I^2{}_{Tapa,rms} = \frac{2}{\pi^2}\hat{I}_2{}^2 \cdot M_{12} \cdot (\tfrac{1}{4} + \cos^2\Phi_2)$$

With the defined current values (typical for transistor T_{apa}) the global conduction loss formulas can be written in a more compact way.
The generalized **worst case** to be considered for dimensioning the rectifier stage is given by

$$M_{12} = 1, \Phi_2 = 0$$

$$\rightarrow \bar{I}_{Tapa,WC} = \frac{\sqrt{3}\hat{I}_2}{2\pi}; \quad I^2{}_{Tapa,rms,WC} = \frac{5\hat{I}_2{}^2}{2\pi^2}$$

The losses of the Very Sparse Matrix Converter are

$$P_{C,Rect,Tapa} = u_{F,T} \cdot \bar{I}_{Tapa} + r_T \cdot I^2{}_{Tapa,rms} \quad (38)$$

$$P_{C,Rect,Dpa} = 0\,^3$$

$$P_{C,Rect,Dap} = u_{F,D} \cdot \bar{I}_{Tapa} + r_D \cdot I^2{}_{Tapa,rms}$$

This results in total VSMC rectifier losses of

$$P_{C,Rect,VSMC} = 6 \cdot (P_{C,Rect,Tapa} + 2P_{C,Rect,Dap} + 2P_{C,Rect,Dpa})\,.$$

The losses for the additional components of the Sparse Matrix Converter are given as

$$P_{C,Rect,Ta} = u_{F,T} \cdot 2\bar{I}_{Tapa} + r_T \cdot 2I^2{}_{Tapa,rms}$$

$$P_{C,Rect,Tpa} = 0\,^4$$

$$P_{C,Rect,Dpna} = u_{F,D} \cdot \bar{I}_{Tapa} + r_D \cdot I^2{}_{Tapa,rms} \quad (39)$$

The total SMC rectifier losses are:

$$P_{C,Rect,SMC} = 6 \cdot (\tfrac{1}{2}P_{C,Rect,Ta} + P_{C,Rect,Tpa} + P_{C,Rect,Dap} + P_{C,Rect,Dpna})\,.$$

Local Losses and Maximum in φ_2

The input stage conduction losses depend only on the DC link current, which comprises of positive and negative (if $\Phi_2 > \pi/6$) components. The DC link current components can be calculated from the actual output phase currents being weighted with the appropriate relative turn-on times of the output stage transistors. The results are graphically shown in **Fig.13** for transistor T_{apa}.

For very low output frequencies applied to a motor in steady state (which has to be considered assuming a thermal time constant of τ_{th} = 60…80ms) almost no back EMF does occur. Therefore the converter output voltage is also close to zero, which means the modulation index is about zero as well. Consequently this means that there will not be any rectifier stage losses at this operating point:

$$f_2 << f_1 \rightarrow M_{12} \approx 0$$

$$\hat{\bar{p}}_{C,Rect,T/D} = P_{C,Rect,T/D} = 0 \quad (40)$$

[3] When regenerating back energy from the motor to the mains ($\Phi_2 = \pi$) the worst case condition of D_{pa} is reached and corresponds to that one of D_{ap} (for Φ_2=0): $P_{C,Rect,Dpa,WC} = P_{C,Rect,Dap,WC}$

[4] Analogously: $P_{C,Rect,Tpa,WC} = P_{C,Rect,Tapa,WC}$

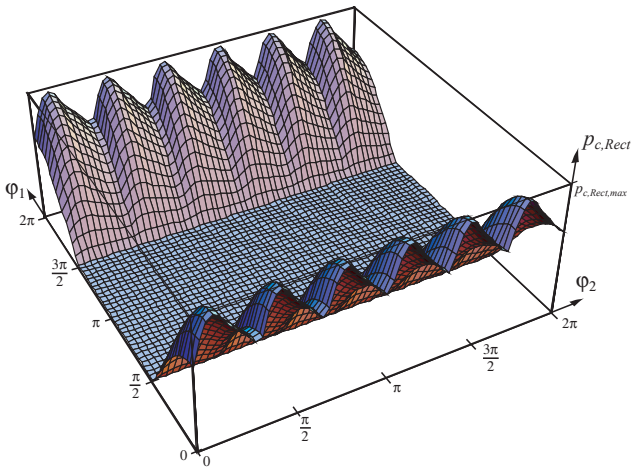


Fig. 15: Local conduction losses of VSMC rectifier stage transistor T_{apa} ($M = 1$, $\Phi_2 = \pi/3$). *Remark*: The characteristics of the other rectifier stage semiconductors look qualitatively different.

IV Dimensioning Example of a CMC

To show how the derived formulas are used for the dimensioning the power semiconductors of a CMC, the following specifications for the CMC are used.

Nominal output power:	$P_{2N} = 7.5\text{kW}$
Input voltage amplitude	$\hat{U}_1 = \sqrt{2}\ 230\text{V}$
Switching frequency	$f_P = 20\text{kHz}$

Therefore, the output current amplitude is

$$\hat{I}_2 = \frac{4}{3\sqrt{3}} \cdot \frac{P_{2N}}{\hat{U}_1} = 17.75A\,. \qquad (41)$$

IV.A Switching Loss Calculation

The average junction temperature of the power semiconductors are determined by the global losses (13). Operating the CMC with a nominal output current displacement angle of $\phi_2=0$ is considered in this example, which represents the operation of a synchronous machine in the motoring mode (steady state). From (13) using the coefficients from Tab.1 the switching losses are calculated as

Transistor	$P_{Sw,T} = 6.7\text{W}$
Diode	$P_{Sw,D} = 3.3\text{W}.$

IV.B Conduction Loss Calculation

The global conduction losses do not depend on ϕ_2. Applying (23) with the measured on-state parameters given in Tab.3 results in

Transistor	$P_{C,T} = 3.5\text{W}$
Diode	$P_{C,D} = 2.4\text{W}.$

IV.C Total Losses

The total losses of a single semiconductor are

$$P_{T/D} = P_{Sw,T/D} + P_{C,T/D} \qquad (42)$$

yielding

Transistor	$P_T = 10.2\text{W}$
Diode	$P_D = 5.7\text{W}$

The total losses of the entire converter system can now be derived directly using

$$P_{CMC} = 18 \cdot (P_T + P_D) \qquad (43)$$

Therefore the total loss of the CMC is $P_{CMC} = 286\text{W}$, or 3.8% of the output power.

In this context, it should be noted that the losses would rise to approximately 4.7% if an output current displacement angle of $\phi_2=\pi/3$ was considered. Assuming a rather conservative dimensioning this value could be taken to represent the systems worst case.

V Conclusions

In this paper the local switching and conduction losses of the different power semiconductors of a single stage (CMC) and a two stage (SMC and/or VSMC) matrix converter have been investigated in detail and visualized in 3D. The basic analytical approaches for deriving the local losses, which provide the foundation for the resulting dimensioning formulas, are given.

Mathematical equations describing the global average switching losses and the global average conduction losses are derived for both topologies. The global average values are accurate for all operating points (alternative equations are provided for operation close to standstill) of the converter systems and are of major relevance in the dimensioning of the semiconductor devices. Moreover, the global loss equations can be applied universally. For calculating the losses of different semiconductors of a given topology and even for obtaining the losses of the entire converter system the same equations can be used, only the semiconductor specific coefficients have to be substituted. Measured switching and conduction loss data of a typical IGBT/Diode pair, operated at a junction temperature of 120°C, are used as the basis for the presented numerical results. The derived loss formulations for the matrix converters are of high accuracy to enable the dimensioning of power semiconductors and heat sinks.

References

[1] **Kolar, J.W., Baumann, M., Schafmeister, F., and Ertl, H.:** *Novel Three-Phase AC-DC-AC Sparse Matrix Converter*. Proceedings of the 17th IEEE Applied Power Electronics Conference, March 10 - 14, Dallas, TX, Vol. 2, pp. 777 - 791 (2002).

[2] **Wei, L., and Lipo, T.A.:** *A Novel Matrix Converter Topology with Simple Commutation.* Record of the IEEE Industry Applications Society Annual Meeting, Chicago, Sept. 30 – Oct. 4, Vol. 3, pp. 1749-1754 (2001).

[3] **Schafmeister, F., and Kolar, J.W.:** *Novel Modulation Schemes for Conventional and Sparse Matrix Converters Facilitating Reactive Power Transfer Independent of Active Power Flow*. Proceedings of the 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, June 21-24, Vol. 4, pp. 2917-2923 (2004).

[4] **Schafmeister, F., Baumann, M., and Kolar, J.W.:** *Analytically Closed Calculation of the Conduction and Switching Losses of Three-Phase AC-AC Sparse Matrix Converters*. CD-ROM of the 10th International Power Electronics and Motion Control Conference, Sept. 9-11, Cavtat \& Dubrovnik, Croatia (2002).

[5] **Kolar, J.W., Ertl, H., and Zach, F.C.:** *Calculation of the Passive and Active Component Stresses of Three-Phase PWM Converter Systems with High Pulse Rate.* Proceedings of the 3rd European Conference on Power Electronics and Applications, Aachen, Germany, Oct. 9-12, Vol. 3, pp. 1303-1311 (1989).

[6] **Huber, L., and Borojevic, D.:** *Space Vector Modulated Three-Phase to Three-Phase Matrix Converter with Input Power Factor Correction*. IEEE Transactions on Industry Applications, Vol. 31, No. 6, pp. 1234-1246 (1995).

[7] **Wheeler, P., Clare, J., Empringham, L., and Bland, M.:** *Technology and Potential of Matrix Converters*. Power Electronics Europe, No. 3, pp. 25-28 (2001).

[8] **Holtz, J., and Boelkens, U.:** *Direct Frequency Converter with Sinusoidal Line Currents for Speed-Variable ac Motors.* IEEE Transactions on Industrial Electronics, Vol. 36, No. 4, pp. 475-478 (1989).

[9] **Schafmeister, F., Herold, S. and Kolar, J.W.:** *Evaluation of 1200V-Si-IGBTs and 1300V-SiC-JFETs for Application in Three-Phase Very Sparse Matrix AC-AC Converter Systems*. Proceedings of the 18th Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach (Florida), USA, February 9 - 13, Vol. 1, pp. 241 - 255 (2003).