Analytically Closed Calculation of the Conduction and Switching Losses of Three-Phase AC-AC Sparse Matrix Converters

F. Schafmeister, M. Baumann*, and J.W. Kolar

ETH Zurich
Power Electronic Systems Laboratory
ETH Zentrum / ETL H23
Physikstr. 3, CH-8092 Zurich/Switzerland
schafmeister@lem.ee.ethz.ch kolar@lem.ee.ethz.ch

*Vienna University of Technology
Dept. of Electrical Drives and Machines
Gusshausstr. 27/E 372
A-1040 Vienna/Austria
martina.baumann@tuwien.ac.at

Abstract – For three-phase AC-AC power conversion a conventional matrix converter (CMC) or a DC side connection of a current DC link rectifier and a voltage DC link inverter comprising no energy storage components in the DC link could be employed. The combination of DC converters does show a lower number of turn-off power semiconductors and, therefore, has been denoted as *Sparse Matrix Converter* (SMC) or *Very Sparse Matrix Converter* (VSMC). A limitation of the phase displacement of the current and voltage fundamentals at the input and at the output to $\pm\pi/6$ does allow a further reduction of the system complexity, the respective circuit topology has been introduced as *Ultra Sparse Matrix Converter* (USMC) in the literature.

In this paper a novel concept for the analytical calculation of the current stresses on the power semiconductors of the Sparse Matrix Converter Topologies (SMC, VSMC, and USMC) is proposed. Furthermore, the switching losses of the output stage which shows identical structure for the SMC, VSMC and USMC are calculated analytically based on an experimentally determined dependency of the switching loss energy on the switching voltage and current. As a comparison to a digital simulation shows, the analytical results do show a very good accuracy in a wide modulation range and for widely varying load current phase angle and widely varying ratio of output and mains frequency and therefore do provide an excellent basis for the dimensioning of the SMC, VSMC or USMC and/or for the determination of the rated output power and efficiency which could be achieved by employing given power transistors and diodes.

I. INTRODUCTION

In [1] novel topologies of three-phase AC-AC PWM converter systems have been proposed, which do show a reduced number of power transistors and a lower control complexity as compared to a conventional matrix converter (CMC). As **Fig.1** shows, the system topologies which have been denoted as *Sparse Matrix Converter* (SMC, cf. Fig.1(a),[2]), *Very Sparse Matrix Converter* (VSMC, cf. Fig.1(b),[3]), and *Ultra Sparse Matrix Converter* (USMC, cf. Fig.1(c)) are formed by DC side coupling of a current DC link rectifier and a voltage DC link inverter. There, the impression of the DC link voltage is by the AC side filtering capacitors via the rectifier stage, the DC link current formed by segments of the inductive load current and impressed via the inverter stage. Accordingly, no energy storage components have to be provided in the DC link.

As for the CMC the switching frequency harmonics of the SMC, VSMC, USMC input current and output voltage are suppressed by an input filter and by the inductive characteristic of the load. Therefore, for proper control mains and load current do show a sinusoidal shape. Via the DC link only active power is transferred, accordingly the input current displacement angle can be defined independently of the load current phase angle.

However, the formation of reactive power at the input is possible only in case a sufficiently large DC link current and/or active power flow to the output is present [1]. Additionally, for the USMC the admissible current displacement at the input and output is limited to $\Phi_1,\Phi_2 \in \pm\pi/6$ in order to ensure a DC link current $i > 0$, as a reversal of the sign of i is prevented by the rectifier stage diodes.

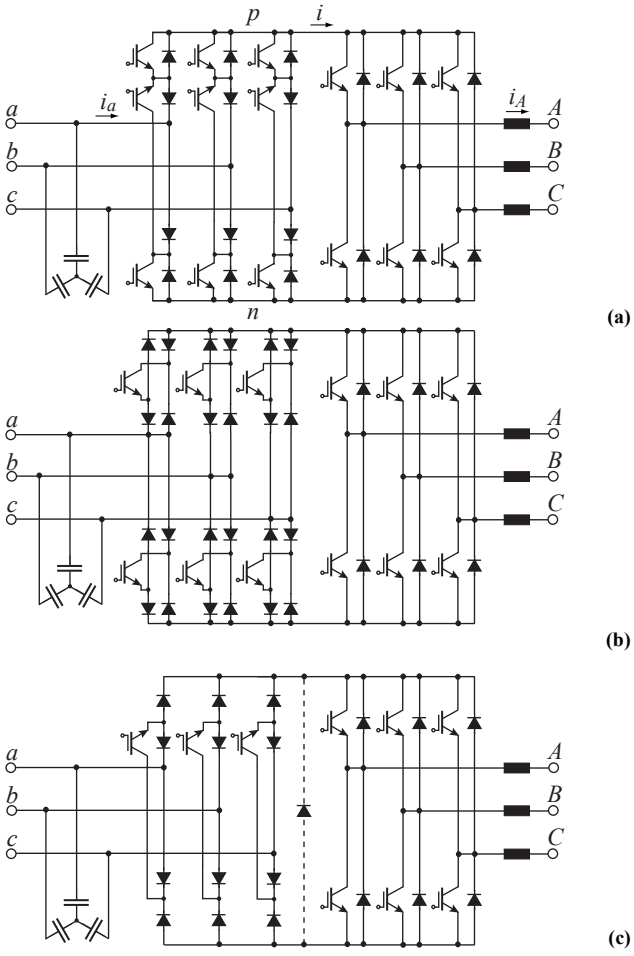

Fig.1: Basic structure of the power circuit of the *Sparse Matrix Converter* (SMC) **(a)**, *Very Sparse Matrix Converter* (VSMC) **(b)**, and of the *Ultra Sparse Matrix Converter* (USMC) **(c)** as proposed in [1].

As for the CMC, a phase displacement Φ_1 of input current and input voltage does reduce the amplitude of the fundamental which could

be formed at maximum at the output. A maximum output voltage range is given for ohmic input characteristic, i.e. $\Phi_1 = 0$. Accordingly, all further considerations will be limited to this case.

An essential advantage of the SMC, VSMC and USMC topologies does consist in the possibility of changing the switching state of the rectifier stage at zero current. If the inverter output stage is switched into the free-wheeling state in advance to commutating the rectifier stage the DC link current is reduced to zero and no continuous connection of the DC link to the mains has to be considered for changing the rectifier switching state. Therefore, the complex multi-step commutation in dependency on the sign of the DC link current or in dependency on the phase voltage difference of the commutating phases [1] being characteristic for the CMC can be omitted what does result in a higher system reliability. Furthermore, the switches of the input stage of the SMC which do provide an individual controllability of both current directions can be replaced by four-quadrant switches formed by a single transistor and a diode bridge resulting in the VSMC topology (cf. Fig.1(a) and (b)).

The aforementioned advantages do motivate a closer analysis of the novel circuit topologies. There, besides a comprehensive discussion of the system control as given in [1], for an industrial application the stresses on the power components and/or guidelines for the dimensioning of the components and a comparison of the conduction and switching losses and/or loss balances and estimated efficiencies of the individual systems are of special interest.

In this paper the calculation of analytical approximations of the current stresses on the power components which has been treated only briefly in [1] will be discussed in detail. As a comparison to the results of a digital simulation verifies, the analytical results do show a very good accuracy in a wide modulation range and for widely varying load current phase angle and widely varying ratio of output and mains frequency.

In **Section II** based on a brief discussion of the PWM scheme being employed in equal form for SMC, VSMC and USMC, the rms and average values of the power transistor and diode currents are calculated analytically. **Section III** shows the analytical calculation of the switching losses of the output stage, where extreme ratios of the mains and output frequency are considered and the dependency of the turn-on and turn-off switching energy loss energy on the switching current and voltage is approximated by a quadratic polynomial. All analytical approximations are verified by digital simulations and the relative errors are determined in dependency on the system operating parameters. Finally, in **Section IV** topics to be covered in the continuation of the research are discussed, where the transfer of the analytical calculation of the stresses on the components to the CMC, and the realization of a 10kW SMC using SiC/Si-cascode power switches and SiC-diodes should be pointed out.

II. CURRENT STRESSES ON THE POWER SEMICONDUCTORS

According to **Tab.1**, **Fig.2** and **Fig.3,** within a π/3–wide interval of the mains period always two line-to-line voltages are switched into the DC link and no free-wheeling interval of the rectifier stage is considered. Accordingly, the local average value of the DC link voltage does show a variation with six times the mains frequency f_1. In order to achieve sinusoidally varying local average values of the inverter output phase voltages this variation has to be compensated by an inverse variation of the inverter modulation index. Accordingly, the exact calculation of the average stresses on the components being determined by the varying modulation index and by the load current amplitude and phase angle is relatively involved. The averaging interval is directly defined only in case the ratio of the mains and output frequency does constitute a rational number and in general a wide averaging interval has to be considered if the output frequency is close to the mains frequency.

$\varphi_1=\omega_1 t$	u_p	u_n	u
0 ... $\pi/6$	u_a	u_b, u_c	u_{ab}, u_{ac}
$\pi/6$ ... $\pi/2$	u_a, u_b	u_c	u_{ac}, u_{bc}
$\pi/2$ ... $5\pi/6$	u_b	u_a, u_c	u_{ba}, u_{bc}
$5\pi/6$ ... $7\pi/6$	u_b, u_c	u_a	u_{ba}, u_{ca}
$7\pi/6$ ... $3\pi/2$	u_c	u_a, u_b	u_{ca}, u_{cb}
$3\pi/2$ ... $11\pi/6$	u_a, u_c	u_b	u_{ab}, u_{cb}
$11\pi/6$ ... 0	u_a	u_b, u_c	u_{ab}, u_{ac}

Tab.1: Intervals of a mains voltage period, and corresponding potentials of the positive and negative DC link bus u_p and u_n (given with reference to the mains star point) and DC link voltage u for the PWM scheme proposed in [1]. The clamping of a phase input to p or n is pointed out by a dotted area.

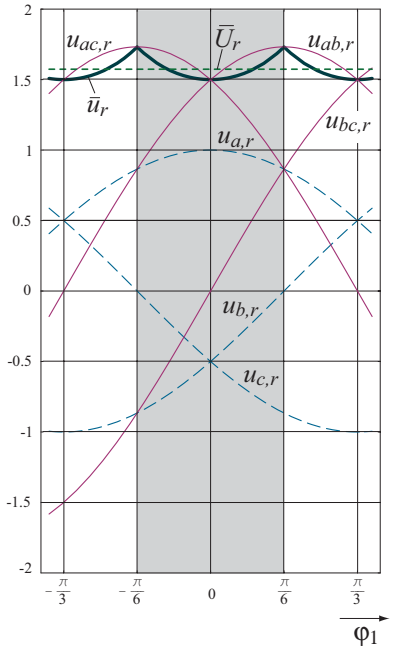

Fig. 2: Time behavior of the mains phase voltages u_a, u_b, u_c, and of the local average $\bar{u}$ of the DC link voltage u; $\bar{U}$ does denote the global average value of u; voltages are normalized (index r) to the mains phase voltage amplitude $\hat{U}_1$. The considerations are limited to the angle interval $\varphi_1 \in (-\pi/6 ... \pi/6)$, which is pointed out by a dotted area.

In order to allow a mathematical formulation of low complexity, in a first approximation we only consider the average modulation index of the output stage and/or a global average value $\bar{U}$ of the DC link voltage. Thereby, the matrix converter is transferred into a constant DC link voltage system and the relation of mains frequency and output frequency is not longer of importance. Considering the limited range of variation of the local average value $\bar{u}$ of the DC link voltage (cf. Fig. 2) and/or of the average DC link current $\bar{\imath}$ we could expect a sufficiently accurate approximation of the actual circuit behavior despite this drastic simplification. This is finally verified by a comparison to the results of a digital simulation (cf. Figs.9 and 10).

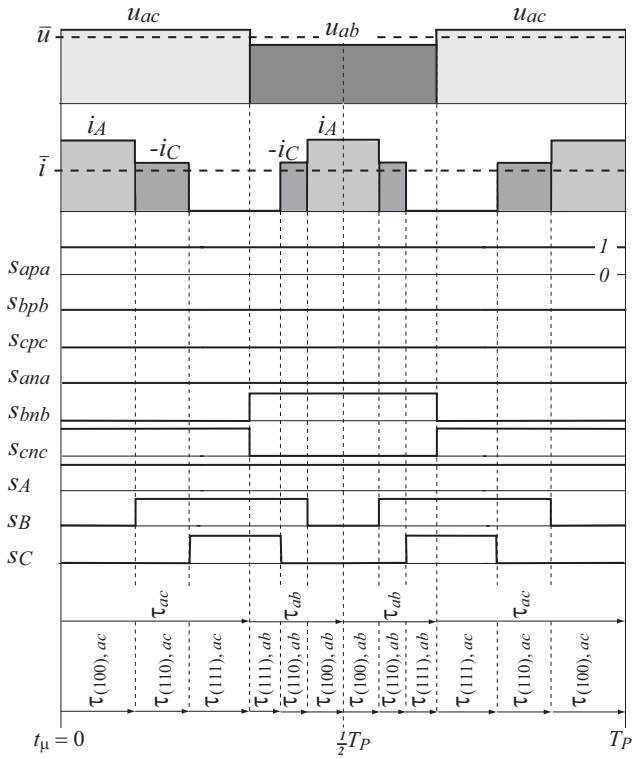

Fig. 3: Formation of the DC link voltage u and DC link current i within a pulse period and corresponding switching functions of the rectifier and inverter stage being characteristic for $\varphi_1 \in (-\pi/6...\pi/6)$ and $\varphi_2 \in (0...\pi/3)$. Switching state changes of the rectifier stage do occur at zero DC link current. The DC link current does show equal average values (denoted by $\bar{i}$) within τ_{ac} and τ_{ab}. The switching frequency ripple of the input line-to-line voltages u_{ac} and u_{ab} and of the output phase currents i_A and i_C is neglected for the sake of clarity.

Assuming a constant DC link voltage $\bar{U}$ and/or constant DC link current $\bar{I}$ the calculation of the stresses on the components can be carried out essentially equal as given in the literature for voltage DC link inverters and/or current DC link rectifiers (cf. [4], and [5]).

Two steps of current averaging have to be performed, i.e. in a first step

- the *local* average value $\bar{i}$ over one pulse period is calculated based on the instantaneous value i of the DC link current, and in a subsequent step
- the *global* average value $\bar{I}$ of the DC link current is determined by averaging of $\bar{i}$ over a $\pi/3$–wide interval of the mains period.

The same procedure has to be applied for the calculation of the local and global DC link current rms values, i_{rms} , and I_{rms}.

With reference to **Fig. 4** it is immediately clear that the sign of the DC link current i has to be considered in the following investigations. The current carrying power semiconductors and/or the conduction losses are determined directly by the actual direction of i (cf. Fig.4).

In general, the time behavior of i is dependent on the phase displacement Φ_2 of output current and output voltage fundamental. For the sake of clearness we will refer to the space vectors $\underline{\bar{u}}_2$ and $\underline{i}_2$ (cf. **Fig.5**) related to the phase quantities $\bar{u}_i$ and i_i, $i=A,B,C$, in the following, where $\bar{u}_i$ denotes the local average value and/or the fundamental of a phase voltage $\bar{u}_i$. In Fig.5 the $\pi/3$–wide interval $\varphi_2 \in (0...\pi/3)$ which will be considered for the calculation of the semiconductor conduction losses is pointed out by a dotted area.

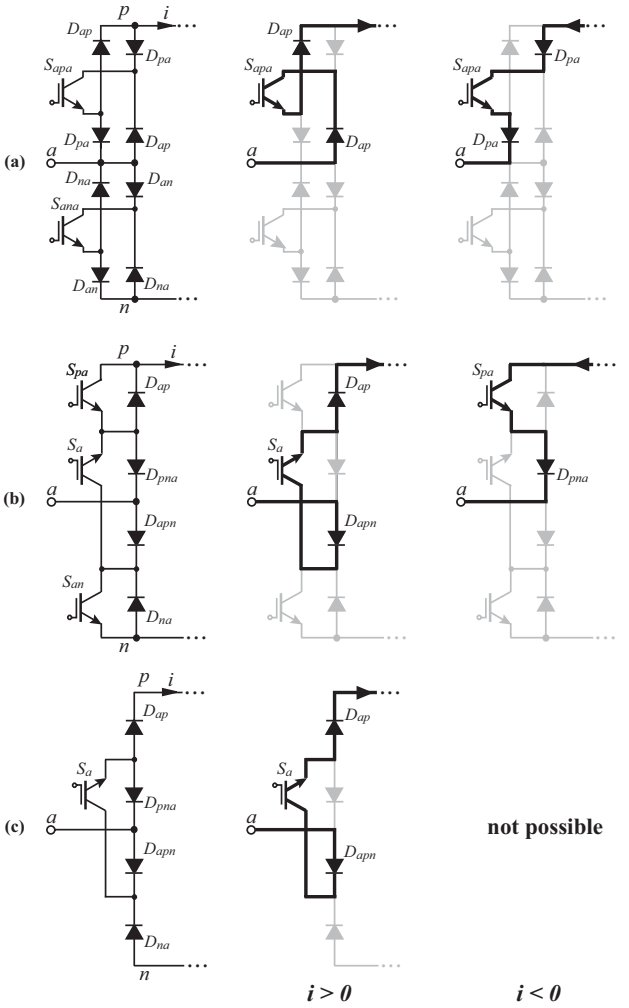

Fig.4: Structure and denomination of the diodes and power transistors of a bridge leg of the input stage of a VSMC **(a)**, SMC **(b),** and USMC **(c).** Identical denominations of components for the different bridge leg topologies do indicate equal current stresses, e.g. the average and rms current stress on diode D_{pa} of the VSMC is identical to the current stress on diode D_{pa} of the USMC. The current paths shown by bold lines are valid for a positive and/or negative DC link current i in case input phase a is connected to the positive rail p of the DC link (as given within the considered angle intervals $\varphi_1 \in (-\pi/6...\pi/6)$ and $\varphi_2 \in (0...\pi/3)$, cf. **Fig. 3**). The operation of the USMC is restricted to positive DC link currents.

According to [4] the DC link current i is determined by the output phase currents and by the inverter stage switching state and/or by the corresponding switching functions s_i, $i=A,B,C$ (in case an output $i=A,B,C$ is connected to the positive DC bus s_i=1 is valid, for the connection to the negative bus we have $s_i = 0$)

$$i = i_A s_A + i_B s_B + i_C s_C \,. \tag{1}$$

In $\varphi_2 \in (0...\pi/3)$ the phase currents i_A and i_C which can be derived by projecting $\underline{i}_2$ onto the corresponding phase axes A and C are involved in the formation of i. The following investigations will be limited to phase displacements $\Phi_2 \in (0...\pi/2)$ for the sake of clearness as in this case $i_C \leq 0$ is valid within $\varphi_2 \in (0...\pi/3)$. Hence, only two cases have to be distinguished:

a) $i_A \geq 0$ and/or $i > 0$ within each pulse period in $\varphi_2 \in (0...\pi/3)$. This is valid in general for $\Phi_2 \in (0...\pi/6)$ and valid in a section of $\varphi_2 \in (0...\pi/3)$ for $\Phi_2 \in (\pi/6...\pi/2)$ which is determined by $\varphi_2 + \Phi_2 \leq \pi/2$; a typical case is represented by space vector $\underline{i}_2^a$ in Fig. 5.

b) For $\varphi_2 + \Phi_2 > \pi/2$ we have $i_A < 0$ in a section of $\varphi_2 \in (0...\pi/3)$ which is determined by the actual value of $\Phi_2 \in (\pi/6...\pi/2)$. The DC link current i then shows positive ($i = -i_C$) and a negative ($i = i_A$) values within a pulse period. A typical case is represented by current vector $\underline{i}_2^b$ in Fig. 5.

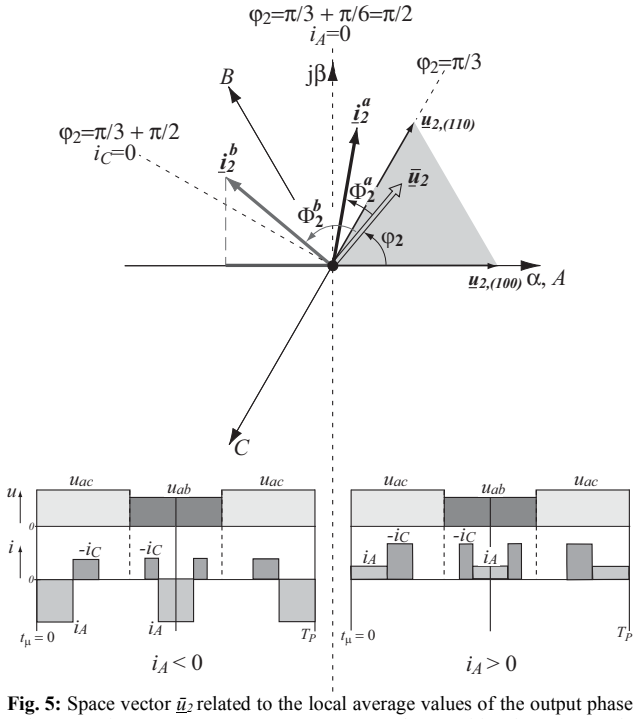

Fig. 5: Space vector $\underline{u}_2$ related to the local average values of the output phase voltages and output current space vector $\underline{i}_2$. The considered output angle interval $\varphi_2 \in (0...\pi/3)$ where the active voltage space vectors $\underline{u}_{(100)}$ and $\underline{u}_{(110)}$ are employed for the formation of $\underline{u}_2$ is indicated by a dotted area. The phase currents i_i, $i=A,B,C$, are obtained by projecting $\underline{i}_2$ onto the phase axes A,B,C. Two current space vectors corresponding to different phase displacements of output voltage fundamental and output current are depicted. For both cases, the resulting time behavior of the DC link currents i within a pulse period is shown; $\underline{i}_2^a$ is located in right half plane, i.e. $i_A > 0$, thus $i > 0$ is valid within the whole pulse period; $\underline{i}_2^b$ is located in left half plane, accordingly we have $i_A < 0$ with i being comprised of positive and negative current segments. If $\Phi_2 > \pi/6$ is valid, i_A and/or i will show negative values for a section of $\varphi_2 \in (0...\pi/3)$ being defined by $\varphi_2 + \Phi_2 > \pi/2$.

II.A GLOBAL AVERAGE MODULATION INDEX

Neglecting the fundamental voltage drop across the inner mains impedance and/or across explicit filtering inductors connected in series the mains voltage space vector

$$\underline{u}_1 = \hat{U}_1 \cdot e^{j\omega_1 t} \tag{2}$$

and/or the corresponding phase voltages

$$\begin{aligned} u_a &= \hat{U}_1 \cos(\varphi_1) \\ u_b &= \hat{U}_1 \cos(\varphi_1 - \tfrac{2\pi}{3}) \\ u_c &= \hat{U}_1 \cos(\varphi_1 + \tfrac{2\pi}{3}) \end{aligned} \tag{3}$$

are impressed at the system input side. There $\varphi_1 = \omega_1 t$ denotes the phase and/or the position within a mains period.

The system output current which is assumed to show a purely sinusoidal shape is impressed by the inductive behavior of the load and should be represented by a current space vector

$$\underline{i}_2 = \hat{I}_2 \cdot e^{j(\omega_2 t + \Phi_2)} \tag{4}$$

and/or by the corresponding phase currents

$$\begin{aligned} i_A &= \hat{I}_2 \cos(\varphi_2 + \Phi_2) \\ i_B &= \hat{I}_2 \cos(\varphi_2 - \tfrac{2\pi}{3} + \Phi_2) \\ i_C &= \hat{I}_2 \cos(\varphi_2 + \tfrac{2\pi}{3} + \Phi_2) \end{aligned} \tag{5}$$

According to [1], Fig.2 and (3) we have within the considered $\pi/3$–wide interval of the mains period $\varphi_1 \in (-\pi/6...\pi/6)$ for the local average value $\bar{u}$ of the DC link voltage

$$\bar{u} = \tfrac{3}{2}\hat{U}_1 \frac{1}{\cos(\varphi_1)} \cdot \tag{6}$$

Therefore, the global average value of DC link voltage can be calculated as

$$\overline{U} = \frac{1}{\pi/3} \int_{-\pi/6}^{\pi/6} \bar{u} d\varphi_1 = \frac{9}{\pi} \ln(\sqrt{3}) \hat{U}_1 \tag{7}$$

and the inverter stage modulation index as

$$m_2 = \frac{\hat{U}_2}{\frac{1}{2}\bar{u}} = \frac{4}{3} \frac{\hat{U}_2}{\hat{U}_1} \cdot \cos(\varphi_1) \cdot \tag{8}$$

With reference to [1] the local average value of the DC link current is

$$\bar{i} = \hat{I}_2 \frac{\hat{U}_2}{\hat{U}_1} \cos(\varphi_1) \cdot \cos(\Phi_2) \tag{9}$$

resulting in a global average value of

$$\bar{I} = \frac{3}{\pi} \int_{-\pi/6}^{\pi/6} \bar{i} d\varphi_1 = \frac{3}{\pi} \cdot \frac{\hat{U}_2}{\hat{U}_1} \cdot \hat{I}_2 \cos(\Phi_2). \tag{10}$$

By defining a global modulation index

$$M_2 = \tfrac{3}{\pi} \int_{-\pi/6}^{\pi/6} m_2 d\varphi_1 = \tfrac{4}{\pi} \cdot \frac{\hat{U}_2}{\hat{U}_1} \tag{11}$$

the global average value of the DC link current can be expressed as

$$\bar{I} = \tfrac{3}{4} M_2 \hat{I}_2 \cos(\Phi_2) \cdot \tag{12}$$

There, one has to note that the global modulation index M_2 according to (11) shows only a minor difference to a definition according to (8), i.e. we have

$$\frac{\hat{U}_2}{\frac{1}{2}\overline{U}} \approx M_2 \tag{13}$$

(the relative difference of the definitions according to (11) and (8) is 0.18 %).

According to **Fig.3,** in the considered interval $\varphi_2 = (0...\pi/3)$ the active switching states $s_{ABC} = (100)$ and (110) are employed for output voltage formation. Therefore, we have for the DC link current

$$i = \begin{cases} i_A & \text{for } s_{ABC} = (100) \text{ eg. within } \tau_{(100),ac} \\ i_A + i_B = -i_C & \text{for } s_{ABC} = (110) \text{ eg. within } \tau_{(110),ac} \end{cases} \tag{14}$$

and the local rms value of the DC link current is defined by

$$i^2_{rms} = \frac{1}{\tau_{ac}} \cdot [\int_{\tau_{(100),ac}} i_A^2 dt_\mu + \int_{\tau_{(110),ac}} i_C^2 dt_\mu] \cdot \tag{15}$$

(as in τ_{ac} and τ_{ab} the active switching states show equal relative on-times [1] one also could refer to the section τ_{ab} of a pulse period, cf. Fig.3, for calculating i^2_{rms}).

Due to the neglection of the ripple components of the output phase currents (cf. (5), [4]) i_A and i_C show an approximately constant

value within a pulse period for pulse frequencies being considerably higher than the output frequency; accordingly, (15) results in

$$i_{rms}{}^2 = \delta_{(100)}(\varphi_1,\varphi_2)\cdot i_A{}^2(\varphi_2) + \delta_{(110)}(\varphi_1,\varphi_2)\cdot i_C{}^2(\varphi_2) \qquad (16)$$

where, with reference to [1], the duty cycles $\delta_{(100)}$ and $\delta_{(110)}$ are defined as

$$\begin{aligned}\delta_{(100)}(\varphi_1,\varphi_2) &= \frac{\tau_{(100),ac}}{\tau_{ac}} = \frac{\sqrt{3}}{2} m_2(\varphi_1)\cdot\cos(\varphi_2+\tfrac{\pi}{6}) \\ \delta_{(110)}(\varphi_1,\varphi_2) &= \frac{\tau_{(110),ac}}{\tau_{ac}} = \frac{\sqrt{3}}{2} m_2(\varphi_1)\cdot\sin(\varphi_2).\end{aligned} \qquad (17)$$

For eliminating the dependency of i^2_{rms} on φ_1 we now replace the local modulation index $m_2(\varphi_1)$ by the global average modulation index M_2 (cf. (11)) in a first approximation. The global rms value of the DC link current then directly follows as

$$\begin{aligned}I_{rms}{}^2 &= \frac{3}{\pi}\int_0^{\pi/3}[\delta_{(100)}(\varphi_2)\cdot i_A{}^2(\varphi_2) + \delta_{(110)}(\varphi_2)\cdot i_C{}^2(\varphi_2)]d\varphi_2 = \\ &= \frac{\sqrt{3}}{\pi} M_2 \hat{I}_2{}^2[\tfrac{1}{4} + \cos^2(\Phi_2)].\end{aligned} \qquad (18)$$

II.A.1 Components of the Global DC Link Current Average Value

With reference to Fig.4 for calculating the conduction losses of the power semiconductors the DC link current i has to be split into a positive component i_+ ($i_+ = i$ for $i>0$ and $i_+=0$ for $i \le 0$) and a negative component i_- ($i_- = -i$ for $i \le 0$ and $i_-=0$ for $i>0$). There, as detailed in connection with Fig.5, the cases $\Phi_2 \in (0...\pi/6)$ and $\Phi_2 \in (\pi/6...\pi/2)$ have to be distinguished.

II.A.1.1 Phase Displacement $\Phi_2 \in (0...\pi/6)$ - Case (a)

For $\Phi_2 \in (0...\pi/6)$ the DC link current is comprised of only positive output current segments, i.e. we have within each pulse period $i > 0$. Accordingly ,

$$\bar{I}_+ = \bar{I} \quad \text{and} \quad \bar{I}_- = 0 \qquad (19)$$

is valid ($\bar{I}_+$ does denote the global average value of the positive components i_+ of i, $\bar{I}_-$ does denote the negative components). Due to $i > 0$ the diodes D_{ap} will not be involved in the current conduction.

II.A.1.2 Phase Displacement $\Phi_2 \in (\pi/6...\pi/2)$ - Case (b)

Considering (1) and (14) we can write for the local average value of the DC link current in analogy to (16)

$$\bar{i} = \delta_{(100)}(\varphi_1,\varphi_2)\cdot i_A(\varphi_2) + \delta_{(110)}(\varphi_1,\varphi_2)\cdot i_C(\varphi_2) \qquad (20)$$

(considering (5) and (17), (20) does result in (9)). As can be seen from **Fig.5**, for a position

$$\varphi_2 = \pi/2 - \Phi_2 \qquad (21)$$

of the output voltage space vector $\underline{\bar{u}}_2$ the output phase current i_A crosses zero what does result in a negative value of $\delta_{(100)}\, i_A$ in (20) for $\varphi_2 > \pi/2 - \Phi_2$.

Hence, we have for the global average value of the positive DC link current component i_+ which is carried e.g. by the diodes D_{ap}

$$\begin{aligned}\bar{I}_+ &= \frac{3}{\pi}[\int_0^{\pi/3}(-i_C)\cdot\delta_{(110)}(\varphi_1,\varphi_2)d\varphi_2 + \int_0^{\pi/2-\Phi_2} i_A\cdot\delta_{(100)}(\varphi_1,\varphi_2)d\varphi_2] = \\ &= \frac{3}{4} M_2 \hat{I}_2[\cos\Phi_2 + \frac{\sqrt{3}}{\pi}((\tfrac{\pi}{6}-\Phi_2)\sin(\tfrac{\pi}{3}+\Phi_2) + \sin(\Phi_2 - \tfrac{\pi}{6}))].\end{aligned} \qquad (22)$$

and accordingly, for the global average value of the negative component i_- of i

$$\begin{aligned}\bar{I}_- &= \frac{3}{\pi}\int_{\pi/2-\Phi_2}^{\pi/3}(-i_A)\delta_{(100)}d\varphi_2 = \\ &= \frac{3\sqrt{3}}{4\pi} M_2 \hat{I}_2[(\tfrac{\pi}{6} + \sqrt{3} - \Phi_2)\sin(\Phi_2 + \tfrac{\pi}{3}) - 2\cos\Phi_2]\end{aligned} \qquad (23)$$

where

$$\bar{I} = \bar{I}_+ - \bar{I}_- \qquad (24)$$

is valid. (As in (18), in (22) and (23) the local value m_2 has been replaced by global modulation index M_2 in order to eliminate the dependency on φ_1).

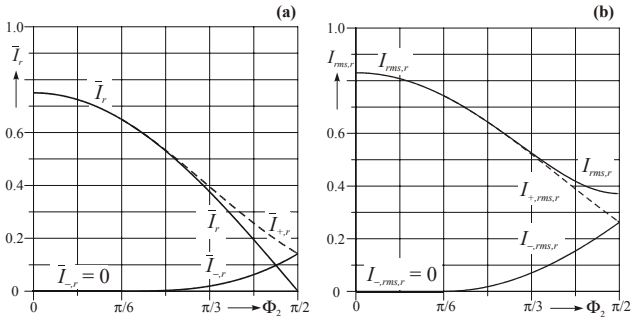

Fig. 5: Graphical representation of the normalized (index r) dependency of the global average value **(a)** and of the global rms value **(b)** of the total DC link current i and of the DC link current components i_+ and i_- (cf. Sections II.A.1 and II.A.2) on the output current phase displacement Φ_2 . Normalization basis: $M_2\hat{I}_2$ (for (a)) and $\sqrt{M_2\hat{I}_2}$ (for (b)).

II.A.2 Components of the Global DC Link Current RMS Value

II.A.2.1 Phase Displacement $\Phi_2 \in (0...\pi/6)$ - Case (a)

As it is immediately clear from the considerations in Section II.A.1.1 we have for the global rms value of the DC link current components

$$I_{rms}{}^2 = I_{+,rms}{}^2 \qquad (25)$$

and

$$I_{-,rms}{}^2 = 0 \qquad (26)$$

II.A.2.2 Phase Displacement $\Phi_2 \in (\pi/6...\pi/2)$ - Case (b)

In analogy to Section II.A.1.2 we have

$$\begin{aligned}I_{+,rms}{}^2 &= \frac{3}{\pi}[\int_0^{\pi/3} i_C{}^2\cdot\delta_{(110)}d\varphi_2 + \int_0^{\pi/2-\Phi_2} i_A{}^2\cdot\delta_{(100)}d\varphi_2] = \\ &= \frac{\sqrt{3}}{\pi} M_2 \hat{I}_2{}^2[\sin(\Phi_2 + \tfrac{\pi}{3}) - \frac{\sqrt{3}}{4}\sin(2\Phi_2 - \tfrac{\pi}{3})]\end{aligned} \qquad (27)$$

and

$$\begin{aligned}I_{-,rms}{}^2 &= \frac{3}{\pi}\int_{\pi/2-\Phi_2}^{\pi/3} i_A{}^2\cdot\delta_{(100)}d\varphi_2 = \\ &= \frac{\sqrt{3}}{\pi} M_2 \bar{I}_2{}^2[\tfrac{3}{4} + \tfrac{1}{4}\sin(2\Phi_2 + \tfrac{\pi}{6}) - \sin(\Phi_2 + \tfrac{\pi}{3})]\end{aligned} \qquad (28)$$

where

$$I_{rms}{}^2 = I_{+,rms}{}^2 + I_{-,rms}{}^2 \qquad (29)$$

is valid as i_+ and i_- do not overlap in time.

II.B STRESSES ON THE POWER SEMICONDUCTORS OF THE INPUT STAGE

II.B.1 Phase Displacement $\Phi_2 \in (0...\pi/6)$ - Case(a)

II.B.1.1 CURRENT AVERAGE VALUES

Due to the symmetric distribution of the DC link current i to the rectifier bridge legs we have

$$\begin{aligned} \bar{I}_{Dap} &= \frac{1}{3}\bar{I} = \frac{1}{4} M_2 \hat{I}_2 \cos\Phi_2 \\ \bar{I}_{Sapa} &= \bar{I}_{Dpna} = \bar{I}_{ap} \\ \bar{I}_{Sa} &= 2\bar{I}_{Dap}. \end{aligned} \tag{30}$$

According to $i>0$ the diodes D_{pa}, D_{an} and the switches S_{pa}, S_{an} do not participate in the current conduction, i.e. $i_{Dpa} = i_{Spa} = 0$ and/or

$$\bar{I}_{Dpa} = \bar{I}_{Spa} = 0 \tag{31}$$

is valid.

II.B.1.2 CURRENT RMS VALUES

In analogy to Section II.B.1.1 we have

$$\begin{aligned} I_{Dap,rms}{}^2 &= \frac{1}{3} I_{rms}{}^2 = \frac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 (\frac{1}{4} + \cos^2\Phi_2) \\ I_{Sapa,rms}{}^2 &= I_{Dpna,rms}{}^2 = I_{Dap,rms}{}^2 \\ I_{Sa,rms}{}^2 &= 2 I_{Dap,rms}{}^2 \end{aligned} \tag{32}$$

and

$$I_{Dpa,rms} = I_{Spa,rms} = 0\ . \tag{33}$$

II.B.2 Phase Displacement $\Phi_2 \in (\pi/6...\pi/2)$ - Case(b)

II.B.2.1 CURRENT AVERAGE VALUES

Positive components i_+ of i are carried by the diodes D_{ap}, negative components i_- of i are taken over by the diodes D_{pa}. Accordingly, there results for the global average current stress on the devices

$$\begin{aligned} \bar{I}_{Dap} &= \frac{1}{3}\bar{I}_+ = \\ &= \frac{1}{4} M_2 \hat{I}_2 [\cos\Phi_2 + \frac{\sqrt{3}}{\pi}((\frac{\pi}{6} - \Phi_2)\sin(\frac{\pi}{3} + \Phi_2) + \sin(\Phi_2 - \frac{\pi}{6}))] \\ \bar{I}_{Dpa} &= \frac{1}{3}\bar{I}_- = \frac{\sqrt{3}}{4\pi} M_2 \hat{I}_2 [(\frac{\pi}{6} + \sqrt{3} - \Phi_2)\sin(\Phi_2 + \frac{\pi}{3}) - 2\cos\Phi_2] \\ \bar{I}_{Sapa} &= \bar{I}_{Dpna} = (\bar{I}_{Dap} + \bar{I}_{Dpa}) \\ \bar{I}_{Sa} &= 2\bar{I}_{Dap} \\ \bar{I}_{Spa} &= \bar{I}_{Dpa} \end{aligned} \tag{34}$$

II.B.2.2 CURRENT RMS VALUES

In analogy to Section II.B.2.1 we have

$$\begin{aligned} I_{Dap,rms}{}^2 &= \frac{1}{3} I_{+,rms}{}^2 = \frac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 [\sin(\Phi_2 + \frac{\pi}{3}) - \frac{\sqrt{3}}{4}\sin(2\Phi_2 - \frac{\pi}{3})] \\ I_{Dpa,rms}{}^2 &= \frac{1}{3} I_{-,rms}{}^2 = \frac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 [\frac{3}{4} + \frac{1}{4}\sin(2\Phi_2 + \frac{\pi}{6}) - \sin(\Phi_2 + \frac{\pi}{3})] \\ I_{Sapa,rms}{}^2 &= I_{Dpna,rms}{}^2 = (I_{Dap,rms}{}^2 + I_{Dpa,rms}{}^2) = \frac{1}{3} I_{rms}{}^2 = \\ &= \frac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 (\frac{1}{4} + \cos^2\Phi_2) \\ I_{Sa,rms}{}^2 &= 2 I_{Dap,rms}{}^2 \\ I_{Spa,rms}{}^2 &= I_{Dpa,rms}{}^2. \end{aligned} \tag{35}$$

II.C STRESSES ON THE POWER SEMICONDUCTORS OF THE OUTPUT STAGE

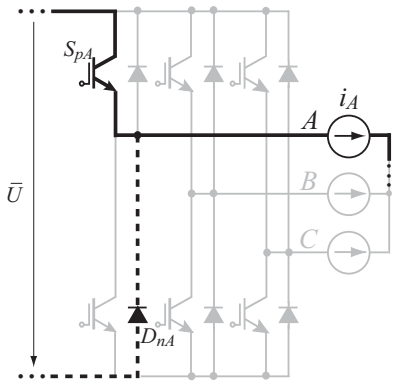

Fig.6: Structure of the output stage of the SMC, VSMC, and USMC. The current impressing inductive load is replaced by current sources. For $i_A>0$ power transitor S_{pA} and diode D_{nA} are involved in current conduction (see current paths pointed out by bold lines).

For the analytical calculation of the conduction losses the inverter output stage is treated as voltage source inverter with the constant input voltage $\bar{U}$ and constant global average modulation index M_2 (cf. (11)). This simplification is near at hand and does a priori neglect the actual variation of the inverter stage modulation index with six times the mains frequency (cf. (8)) which would be averaged out in any case in the course of the calculation of the global current average and rms values. A comparison of the results to the actual current stresses determined by a digital simulation finally justifies this considerable simplification.

Due to the symmetries of the output stage circuit topology the investigation can be limited to the analysis of a transistor and the corresponding free-wheeling diode, e.g. S_{pA} and D_{nA} of phase leg A. As the results derived in the following are valid for any transistor and any diode of the output stage, the denominations S_A and D_A instead of S_{pA} and D_{nA} will be used in the following. There, the index A should refer to the output stage in general and should not indicate that the results are restricted to bridge leg A.

II.C.1 Power Transistor

For calculating the conduction losses of S_A we have to consider the fundamental of the output voltage of the phase A (cf. (4))

$$u_A = \hat{U}_2 \cdot \cos(\varphi_2) \tag{36}$$

and/or the corresponding relative on-time of S_A

$$d_{SA} = \frac{1}{2} + \frac{1}{2}\frac{u_A}{\bar{U}/2}\ . \tag{37}$$

With reference to (13) and (36) we then have

$$d_{SA} = \frac{1}{2} + \frac{1}{2} M_2 \cdot \cos(\varphi_2)\ . \tag{38}$$

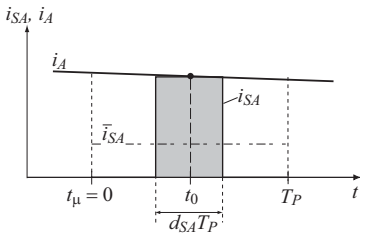

Fig.7: Approximation of the current flow in S_A within one pulse period T_P and related local transistor current average value $\bar{i}_{SA}$.

As the modulation index of the output stage shows equal values in the sections τ_{ac} and τ_{ab} of a pulse period T_P (cf. Fig.3), d_{SA} is

representative for the whole pulse period. The current flow in S_A can be approximated as shown in **Fig.7**.

Assuming a high switching frequency $f_P=1/T_P$, the phase current i_A can be treated as being approximately constant within one pulse period and we get for the local average value of i_{SA} [4]

$$\bar{i}_{SA}=\frac{1}{T_P}\int_{t_0-\frac{T_P}{2}}^{t_0+\frac{T_P}{2}} i_{SA}dt_\mu=\frac{1}{T_p}\cdot i_A\int_{t_0-d_{SA}\frac{T_P}{2}}^{t_0+d_{SA}\frac{T_P}{2}} dt_\mu=i_A(\varphi_2)\cdot d_{SA}(\varphi_2). \quad (39)$$

The global average value of i_{SA} (related to an output voltage period) then follows from averaging over the interval where S_A is participating in the current conduction and/or where $i_A > 0$ is valid (cf. **Fig.6**)

$$\bar{I}_{SA}=\frac{1}{2\pi}\int_{-\frac{\pi}{2}-\phi_2}^{\frac{\pi}{2}-\phi_2}\bar{i}_{SA}(\varphi_2)d\varphi_2=\frac{1}{2}\hat{I}_2(\frac{1}{\pi}+\frac{1}{4}M_2\cdot\cos(\Phi_2)). \quad (40)$$

For the global rms value of the power transistor current there results based on analogous considerations

$$I_{SA,rms}{}^2=\hat{I}_2{}^2(\tfrac{1}{8}+\tfrac{1}{3\pi}M_2\cos\Phi_2). \quad (41)$$

II.C.2 Power Diode

According to the assumption of a continuous output current (cf. (5)) the relative on-time of the power diode D_A is determined by d_{DA} where we have $d_{DA} = 1\text{-}d_{SA}$. The global average value and global rms value of i_{DA} can then be calculated analogously to (40) as

$$\begin{aligned}\bar{I}_{DA}&=\tfrac{1}{2}\hat{I}_2(\frac{1}{\pi}-\frac{1}{4}M_2\cdot\cos(\Phi_2))\\ I_{DA,rms}{}^2&=\hat{I}_2{}^2(\tfrac{1}{8}-\tfrac{1}{3\pi}M_2\cos\Phi_2).\end{aligned} \quad (42)$$

II.D GRAPHICAL REPRESENTATION OF THE RESULTS OF THE ANALYTICAL CALCULATIONS

The results of the analytical calculation of the current stresses on the input stage power semiconductors of the SMC, VSMC, and USMC performed in Section II.B are depicted in **Fig.8** exemplary for the VSMC.

According to the linear dependency of the relative on-time of the active switching states of the output stage which do result in a DC link current i there is a linear dependency of average current values and of the square of the rms current values on the global modulation index M_2.

For $\Phi_2= 0$ and $M_2 > 0.8$ and/or for maximum power transfer via the DC link the average stress on S_{apa} and D_{ap} is approximately equal to $0.2\hat{I}_2$, while the rms value is in a first approximation $0.4\hat{I}_2$ (D_{pa} is not carrying any current in this case)**.**

For increasing the output current phase displacement Φ_2 there follows a reduction of the current stresses on S_{apa} and D_{ap} corresponding to the reduction of the power transferred from the input to the output.

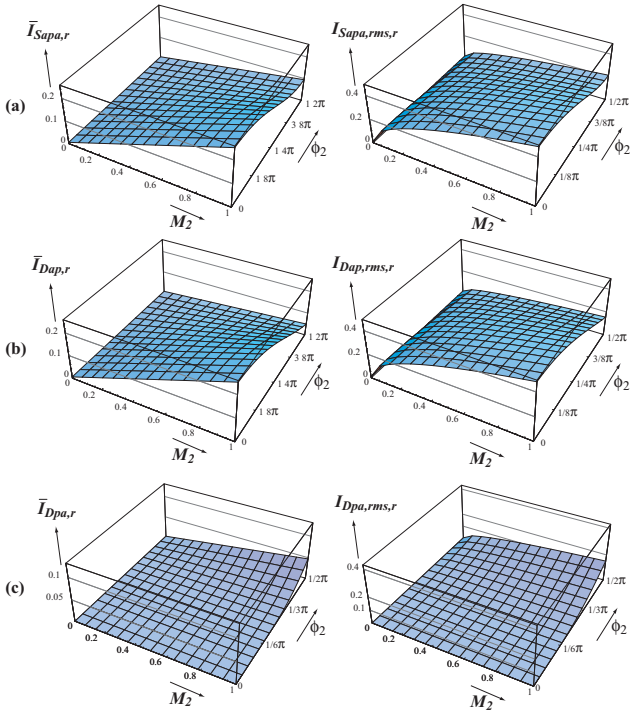

Fig.8: Normalized representation (index r, normalization basis $\hat{I}_2$) of the analytical results derived in Section II.B for the current stresses on the power semiconductors of the VSMC input stage; **(a)** transistor S_{apa} which conducts current independently of the direction of i; **(b)** diode D_{ap} conducting current for $i>0$; **(c)** diode D_{pa} conducting current for $i\leq 0$. The average current values of the components are shown on the left hand side, rms current stresses are depicted on the right hand side.

As for $\Phi_2>\pi/6$ negative components of i do occur the average current stress on D_{pa} does increase starting from 0 at $\Phi_2=\pi/6$ and does reach a maximum of approximately $0.05\hat{I}_2$ at $\Phi_2=\pi/2$ and M_2=1.0. In this case the rms current stress on D_{pa} is approximately equal to $0.15\hat{I}_2$.

II.E COMPARISON TO DIGITAL SIMULATION

The analytical results derived in Sections II.B and II.C have been verified with excellent consistency by extensive digital simulations within a wide operating range characterized by the ratio of the input frequency f_1 and output frequency f_2, the output stage modulation index M_2 and output current phase displacement Φ_2.

For limiting to the essentials only the relative deviation of the analytical results for the VSMC and for the output stage from the results of the digital simulations are compiled in **Figs. 9** and **10**. There, the employed current reference value I_{Ref} is derived from the nominal output power

$$P_{2N}=\frac{3}{2}\hat{U}_2\hat{I}_2\cos\Phi_2=10kW. \quad (43)$$

With Φ_2=0 and the maximal feasible output voltage amplitude $\hat{U}_2=\hat{U}_{2,\max}=\sqrt{3}/2\ \hat{U}_1$ ($\hat{U}_1$=325V) one gets

$$I_{\mathrm{Ref}}=\frac{4}{3\sqrt{3}}\frac{P_{2N}}{\hat{U}_1}=23.67A. \quad (44)$$

Remark: As for the analytical calculations purely sinusoidal output currents also have been employed in the digital simulations. Including the output current ripples would introduce two further parameters (load inductances and switching frequency) and would not allow to gain a clear picture of the influence of the main simplification used in the analytical calculations, i.e. of the approximation of the time-varying output stage modulation index by a constant global average value M_2.

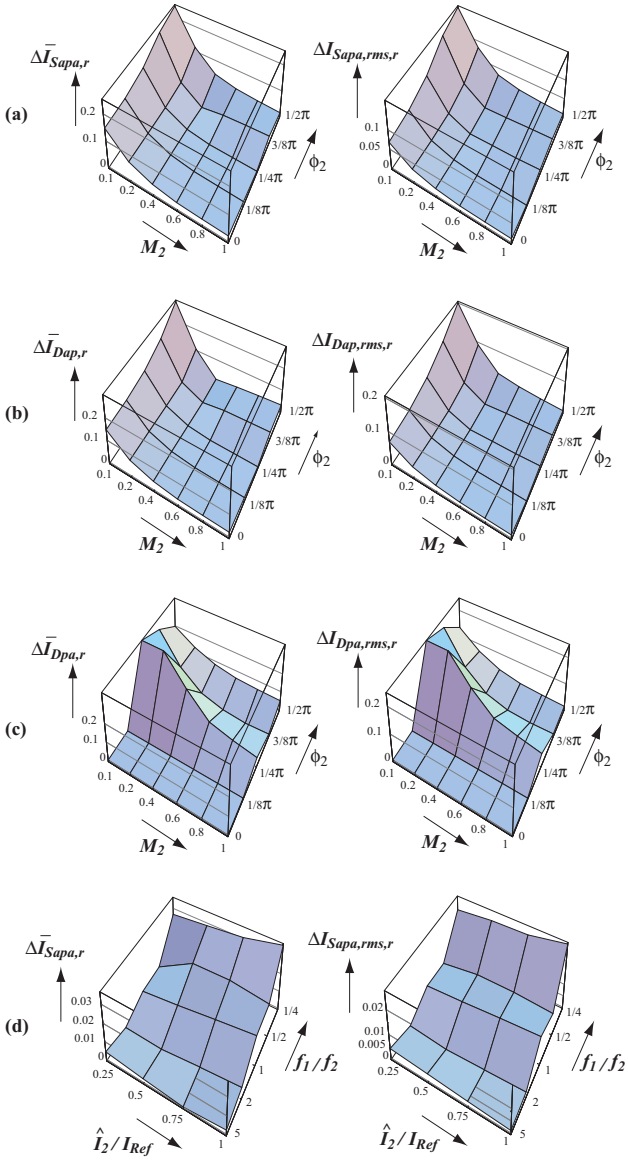

Fig.9: Relative deviation of the analytically calculated current stresses on the power semiconductors S_{apa} (cf. **(a)**), D_{ap} (cf. **(b)**), and D_{pa} (cf. **(c)**) of the VSMC from the results of a digital simulation in dependency on the output stage global average modulation index M_2 and the output current phase displacement Φ_2 for $f_1/f_2 = 1/2$, f_1=50Hz, $\hat{U}_1$= 325V and $\hat{I}_2/I_{Ref}$= 3/4. Average current stresses are shown on the left hand side; rms current stresses are depicted on the right hand side. Furthermore shown in **(d)**: Influence of a varying frequency ratio f_1/f_2 on the relative deviation for transistor S_{apa} in dependency on the normalized output current amplitude (normalization basis: $I_{\mathrm{Ref}} = 4P_N/(3\sqrt{3}\hat{U}_1) = 23.67A$) and on the input and output frequency ratio (for M_2=0.8, Φ_2= 3π/8, f_1=50Hz, $\hat{U}_1$= 325V).

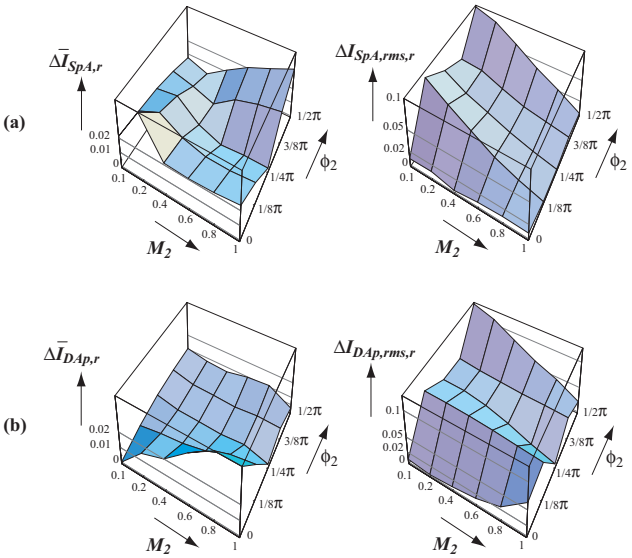

Fig.10: Relative deviation of the analytically calculated current stresses on the output stage power semiconductors S_A (cf. **(a)**), and D_A (cf. **(b)**) from the results of a digital simulation in dependency on the output stage global average modulation index M_2 and the output current phase displacement Φ_2 for f_1/f_2 = 1/2, f_1=50Hz, $\hat{U}_1$= 325V and $\hat{I}_2/I_{Ref}$= 3/4. Average current stresses are shown on the left hand side, rms current stresses are depicted on the right hand side.

According to Figs.9 and 10 the relative deviations of the analytical calculations from the results of a digital simulation for S_{apa} and D_{ap} are limited to about 5% in a wide operating range. Only for M_2<0.2 and $\Phi_2=\pi/2$ a larger errors does occur.

The relatively low accuracy of the analytically calculated current stress on D_{pa} has to be seen in connection with the low absolute value of $\bar{I}_{Dap}$ and $I_{Dpa,rms}$ (cf. Fig.8(c)). Therefore, the impact of an approximation of given value is higher as compared to the higher absolute values of the current stresses on S_{apa} and D_{ap}.

Furthermore, according to Fig.10(c) a changing output current fundamental amplitude $\hat{I}_2$ does not result in a deviation of the results of the analytical calculations and the digital simulations. Also, the deviation does not exceed about 3% within a wide output frequency range of 10…200Hz (f_1=50Hz).

For the output stage power semiconductors S_A and D_A the deviation of the analytically calculated current stresses from the results of a digital simulation is very low, i.e. about 2% for the current average values and about 5% for the current rms values.

Therefore, in summary the analytical calculations do provide an excellent basis for the dimensioning of the SMC, VSMC and USMC power circuit concerning conduction losses.

III. Converter Switching Losses

For the analytical calculation of the average switching losses of a power transistor and/or power diode one has to refer to the dependency of the energy loss of the respective switching actions on the switching voltage and switching current (cf. Section III.5 in [6]) which has to be determined experimentally for the final circuit layout in order to achieve a sufficiently high accuracy.

III.A EXPERIMENTAL ANALYSIS OF THE VSMC SWITCHING LOSSES

In the case at hand the experimental switching loss analysis is performed on a $400V_{rms}$ line-to-line input 10kW VSMC prototype realized in IGBT technology [1], [7] (cf. **Fig.11**). Auxiliary DC voltage sources are used for simulating different input voltage conditions as occurring within $\varphi_1 \in (-\pi/6...\pi/6)$, the output current is impressed by inductors connected in between two output terminals (phases *A* and *B*). The applied control signals forming a switching state sequence are shown in **Fig.12** (the transistors S_{pA} and S_{cnc} are turned on continuously, as always two power transistors remain in the on-state within a pulse period, cf. Fig.3).

For turning on S_{apa} and S_{Bn} in $t = 0$, U_{ac} is applied to the output side inductors, accordingly i_L will increase until a given current level is reached at t_1 and S_{Bn} is turned off. By turning off S_{Bn}, i_L is commutated into D_{Bp}, where the turn-off losses of an output stage transistor could be measured. Subsequently, S_{apa} is turned off at t_2 with minor delay in order to ensure, that the commutation into D_{Bp} already is completed; this turn-off is at zero current and no turn-off losses do occur. Next, in t_3, S_{bpb} is turned on. As a detailed analysis shows, there for delay times $\Delta t = t_3 - t_2$ lower than ≈500ns switching losses do occur in S_{apa} and S_{bpb} as charge carriers are still available for current conduction in S_{apa} which has been remaining at zero current within $(t_1 \ldots t_3)$. Furthermore, the state of charge of the parasitic DC link capacitance which is mainly formed by the output capacitances of the power semiconductors and charged according to U_{ac} is changed by switching over from U_{ac} to U_{bc} (turning on S_{bpb}) resulting in a corresponding discharging current (for $U_{bc} < U_{ac}$) over S_{bpb}. Subsequently, S_{Bn} is turned on again in t_4, where the turn-on losses of an output stage power transistor and turn-off losses of an output stage power diode could be measured. There, S_{bpb} and S_{cnc} and the corresponding diodes are immediately required to conduct current, accordingly a forward recovery voltage does occur which lowers the turn-on voltage and/or the turn-on losses of S_{Bn} and turn-off losses of D_{Bp}. The switching state sequence is completed by turning off S_{Bn} again and subsequently turning off S_{apa} and S_{bpb} what does result in continuous free-wheeling of i_L across S_{pA} and D_{Bp}. Selecting a sufficiently low repetition rate of ≈ 1Hz (considerably larger than the load inductor time constant) the junction temperature rise of the power semiconductors due to the switching action is limited to low values and/or the junction temperature can be set by pre-heating of the VSMC heat sink. This does allow the analysis of the dependency of the switching losses on the junction temperature.

The results gained from the switching loss analysis will be discussed in more detail in a future paper. Here, it only should be pointed out that a switching loss of the input stage power semiconductors does occur despite no DC link current *i* is present at the input stage switching instants as the load i_L current is free-wheeling via the output stage.

For the sake of brevity all following considerations are limited to the switching energy loss of the output stage power semiconductors. Therefore, with reference to Fig.12 only the switching actions at t_1 and t_4 are relevant. In t_1 turn-off losses $w_S^{off \to on}$ of S_{Bn} do occur (forward recovery losses of D_{Bp} are negligible), where a DC link voltage of U_{ac} is present. In t_4 the load current i_L is commutated from D_{Bp} back into S_{Bn} at a DC link voltage U_{bc}, here the reverse recovery losses $w_D^{on \to off}$ of D_{Bp} and the turn-on losses $w_S^{off \to on}$ of S_{Bn} are relevant. Exemplary, the dependency of the reverse recovery losses $w_D^{on \to off}$ of D_{Bp} on the switching voltage and current as determined by the experimental analysis is shown in **Fig.13**.

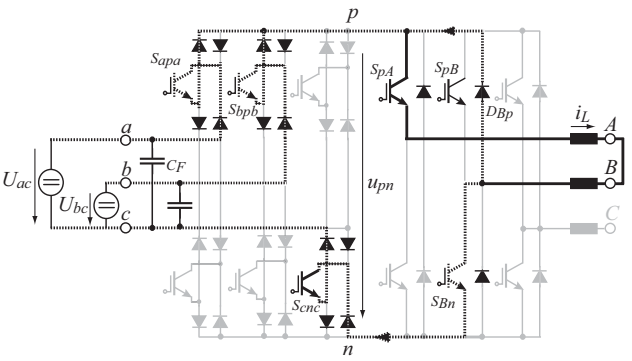

Fig.11: Circuit employed for the experimental determination of the the switching losses of the input- and the output stage of the VSMC. Current paths and power semiconductors being active for the switching state sequence considered (cf. Fig.12) are pointed out by bold lines, where continuous lines do indicate circuit parts which are continuously carrying current within $t \in (0, t_4)$.

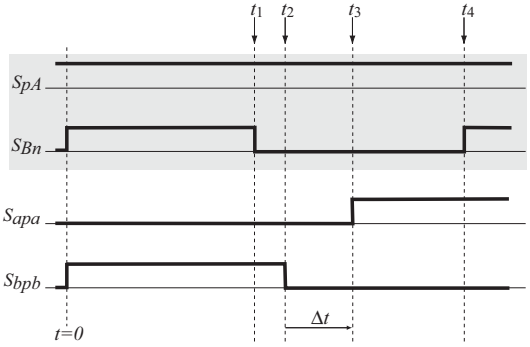

Fig.12: Switching state sequence employed for the experimental switching loss analysis.

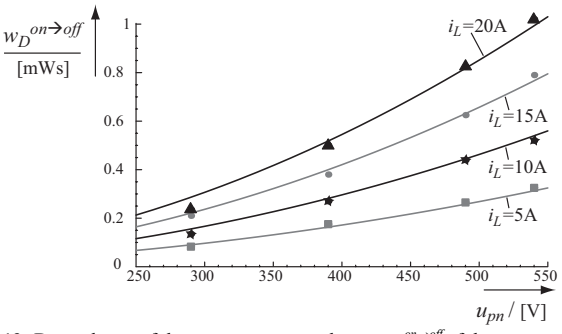

Fig.13: Dependency of the reverse recovery losses $w_D^{on \to off}$ of the output stage power diode D_{Bp} on the switching current i_L and on switching voltage (DC link voltage u_{pn} being present at the time of the switching action). Quadratic least-square approximations (cf. Tab.2) of the experimental results are shown by continuous lines.

In order to provide a basis for calculation of the average switching energy losses of the output stage power semiconductors the dependency of the measured switching energy losses $w_S^{on \to off}$, $w_D^{on \to off}$, and $w_S^{off \to on}$ on the switching voltage and current is

approximated by quadratic polynomials applying the least-squares method (cf. **Tab.2** and Fig.13).

Remark: The terms being dependent only on the switching voltage do originate from parasitic capacitances of the power semiconductors. Due to changing potentials during the switching actions of the input stage, those capacitances are partly discharged lossless. The following calculations neglect this minor impact and therefore do give a worst case approximation of the output stage switching losses.

As shown in Fig.13 the polynomials do give a sufficiently accurate approximation of the measurement results.

t_i	switching energy loss
t_1	$w_S^{on\to off} = 114.8\frac{\mu J}{A}\cdot i_L + 2.4\frac{nJ}{V^2}\cdot u_{pn}^2$
t_4	$w_D^{on\to off} = 155.5\frac{pJ}{AV^2}\cdot i_L\cdot u_{pn}^2 + 295.7\frac{pJ}{V^2}\cdot u_{pn}^2$
t_4	$w_S^{off\to on} = 122.6\frac{pJ}{AV^2}\cdot i_L\cdot u_{pn}^2 + 678.8\frac{pJ}{V^2}\cdot u_{pn}^2$

Tab.2: Polynomial approximation of the dependency of the switching energy loss of the output stage power semiconductors on the switching voltage u_{pn} and switching current i_L.

Based on the analytical expressions compiled in Tab.2 the calculation of the average switching losses of the inverter stage could be performed by digital simulation. There, due to the symmetry of the power circuit topology only a power transistor and the respective free-wheeling diode of one phase leg have to be considered and global average switching losses have to be determined by summation of the local switching energy loss contributions over a time interval defined by the minimum integer multiple of input and output voltage fundamental periods.

Alternatively, analogous to the calculation of the conduction losses analytical approximations of the average switching losses could be derived in order to provide insight into the dependency of the switching losses on the system operating parameters and to considerably simplify the system dimensioning.

Both aforementioned approaches have been employed in the case at hand. There, the results of the digital simulation served as basis for the evaluation of the approximations calculated in analytically closed form for extreme ratios, $f_1 \gg f_2$ and $f_1 \ll f_2$, of the input and output frequency as shown in the following.

III.B Analytical Calculation of the Output Stage Switching Losses

An analytical calculation of the output stage switching losses is feasible only for extreme ratios of the input and output frequency, as for $f_1 \approx f_2$ the time-behavior of the input and output quantities within an input and output voltage period would have to be considered in detail and the phase relation of the input and output voltage would be relevant resulting in countless case distinctions. Therefore, the following considerations are limited to the extreme cases $f_1 \gg f_2$ and $f_1 \ll f_2$.

For $f_1 \gg f_2$, the values of the impressed output currents (e.g. of i_A), can be assumed to be constant over a whole input voltage period (e.g. of u_a). The time behavior of the input and output quantities for this operating condition is shown in **Fig.14**. There, the hatched areas point out those intervals of an output voltage period where the considered phase leg A is being switched and therefore subject to switching losses.

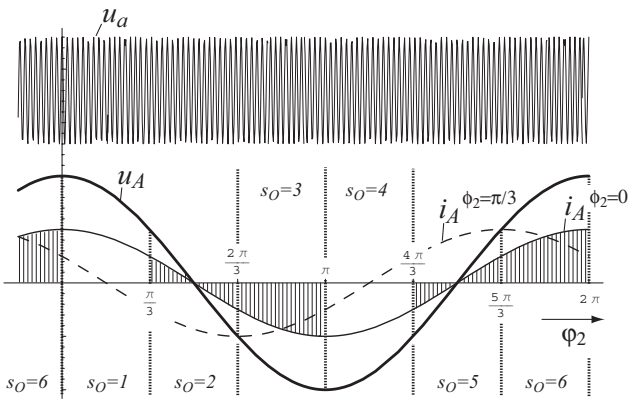

Fig.14: First case of extreme input/output frequency ratios: $f_1 \gg f_2$. During a whole period of u_a (oscillating with the frequency f_1) the value of i_A can be assumed to be constant. i_A is displayed for two values of displacement angle, $\Phi_2=0$ and $\Phi_2=\pi/3$. The intervals/sectors s_O of an output period in which the phase leg A is being switched are marked.

Analogously, for $f_1 \ll f_2$ the values of the input voltages are considered to be constant for an output current period (cf. **Fig.15**).

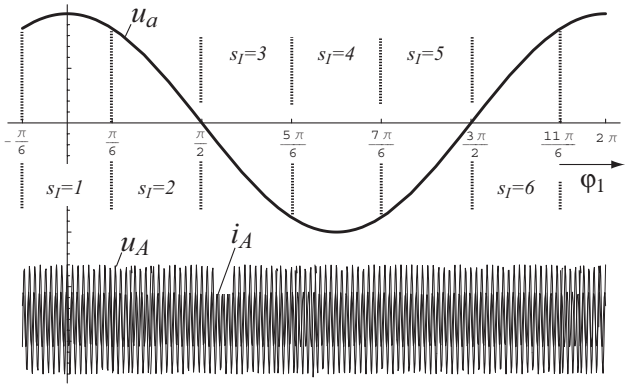

Fig.15: Second case (cf. Fig.14) of extreme frequency ratios: $f_1 \ll f_2$. During a whole period of i_A (oscillating with the frequency f_2) the value of u_a can be assumed as being constant. The numbering s_I denotes the input voltage sectors.

For the sake of brevity, the derivation of an analytically closed solution is restricted to the operating condition $f_1 \gg f_2$ in the following:[1]

Considering an input frequency of f_1=50Hz, two kinds of averaged switching losses are relevant for the dimensioning of the converter system;

a) the losses, averaged over one input period (T_1 =20ms $\ll T_2$, cf. Fig.14) which determine the local junction temperature of the power semiconductor modules. These losses are denoted as *local switching losses p* in the following.
b) the losses, averaged over an input- and output period. These losses are relevant for the heat sink dimensioning and are denoted as *global switching losses P* in the following.

[1] The calculation procedure for $f_1 \ll f_2$ is analogous. Moreover, the final result P_{tot} (cf. (51)) is identical to the result for $f_1 \gg f_2$.

By summing up the energy losses for single switching actions (which are given in analytical form in Tab.2) over a whole pulse period (cf. Fig.3) one gets as result e.g. for phase leg *A*

$$w_{16,A} = (u_{ab}^2(\varphi_1) + u_{ac}^2(\varphi_1)) \cdot [K_1 + K_2 \cdot i_A(\varphi_2,\Phi_2)] + K_3 \cdot i_A(\varphi_2,\Phi_2) \qquad (45)$$

Thereby, (45) depends on the combination of the active input voltage sector (determining the voltages being switched) and the active output voltage sector (determining the current being switched). Here, (45) is valid only for input sector 1 and output sector 6, which is indicated by the index 16. Beyond this, the displacement angle Φ_2 determines the sign of i_A in (45); the calculations given here are limited to the case $\Phi_2 \in (-\pi/6...\pi/6)$. The constants (K_1,K_2,K_3) are composed of the coefficients of the polynomials in Tab.2.

In order to gain the local switching losses, (45) has to be averaged over a mains period (corresponds to averaging over input sector 1) and multiplied by the switching frequency f_s

$$p_{x6,A} = f_s \frac{6}{2\pi} \cdot \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} w_{16,A}(\varphi_1,\varphi_2,\Phi_2) d\varphi_1 = \qquad (46)$$

$$= f_s[3(\frac{3\sqrt{3}}{4\pi}+1) \cdot \hat{U}_1^2 \cdot (K_1 + K_2 \cdot i_A) + K_3 \cdot i_A].$$

Equation (46)[2] is valid only for output voltage sector 6. The resulting general solution for the local switching losses in phase leg *A* is given in (47):

$$p_A(\varphi_2,\Phi_2) = \begin{cases} 0 & for\ s_O \in \{1;4\} \\ f_s[3(\frac{3\sqrt{3}}{4\pi}+1) \cdot \hat{U}_1^2 \cdot (K_1 + K_2 \cdot |i_A|) + K_3 \cdot |i_A|] & for\ s_O \in \{2;3;5;6\} \end{cases} \qquad (47)$$

There, s_O denotes the output voltage sector. i_A is defined in (4). **Figure 16** shows the dependency of p_A on φ_2 and Φ_2 in a three dimensional representation.

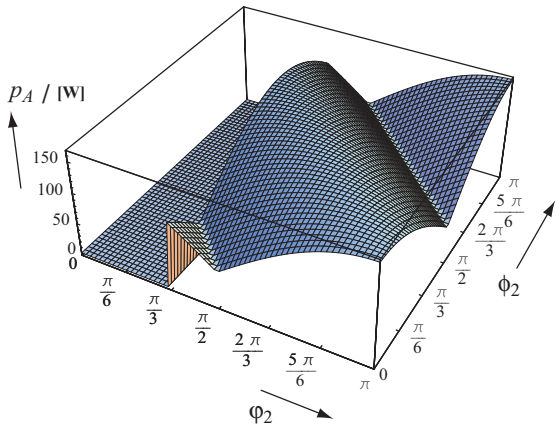

Fig.16: Graphical representation of the analytically gained result for the *local switching losses* occurring at the integrated phase leg module of output phase *A* in dependency of the position φ_2 within the output voltage period and the displacement angle Φ_2. Obviously, during the clamping interval of phase *A* no switching losses do occur.

The quantities are given for an operating point of:

$$\hat{U}_1 = \sqrt{2} \cdot 230V$$
$$\hat{I}_2 = 15A$$
$$f_s = 20kHz$$
$$K_1 = 6.4 \frac{nJ}{V^2}$$
$$K_2 = 278.2 \frac{pJ}{AV^2}$$
$$K_3 = 229.5 \frac{\mu J}{V^2}$$

As is also clear from Fig.14, a maximum of the local switching losses in phase leg *A* does occur at the output phase angle $\varphi_2=\pi$ for a displacement of $\Phi_2=0$, because the maximum value of current is being switched at this point.

This maximum is given by

$$p_{A,\max} = f_s \cdot [\hat{I}_2 K_3 + 3(1+\frac{3\sqrt{3}}{4\pi}) \cdot \hat{U}_1^2 \cdot (K_1 + \hat{I}_2 K_2)] = \qquad (48)$$
$$= 164W.$$

Analogously to (46), the *total* local switching losses (caused by all three output phase currents) for output voltage sector 6 can be calculated as

$$p_{x6,tot,ic>0} = f_s[3(\frac{3\sqrt{3}}{4\pi}+1) \cdot \hat{U}_1^2 \cdot (K_1 + K_2 \cdot (i_A + i_C)) + K_3 \cdot (i_A + i_C)]. \qquad (49)$$

Because of the following integration, a case differentiation distinguishing the sign of i_C, which is changing within output voltage sector 6 has to be performed

$$p_{x6,tot,ic<0} = f_s[3(\frac{3\sqrt{3}}{4\pi}+1) \cdot \hat{U}_1^2 \cdot (K_1 + K_2 \cdot (i_A - i_C)) + K_3 \cdot (i_A - i_C)]. \qquad (50)$$

The averaging of $p_{x6,tot}$ over the respective voltage sector finally yields the expression of the total global switching losses being valid for $\Phi_2 \in (-\pi/6...\pi/6)$

$$P_{tot}(\Phi_2) =$$
$$= \frac{6}{2\pi}[\int_{5\pi/3}^{(7\pi/6)-\phi_2} p_{x6,tot,ic>0}(\varphi_2,\phi_2) d\varphi_2 + \int_{(7\pi/6)-\phi_2}^{2\pi} p_{x6,tot,ic<0}(\varphi_2,\phi_2) d\varphi_2]$$
$$= \frac{3f_s}{8\pi^2}[4\pi \cdot \hat{I}_2 K_3(4-\sqrt{3}\cos\Phi_2 + \sin\Phi_2) + \qquad (51)$$
$$+ \hat{U}_1^2[(3\sqrt{3}+4\pi) \cdot (12\hat{I}_2 K_2 + 2\pi K_1 + 3\hat{I}_2 K_2 \sin\Phi_2) -$$
$$- 3\hat{I}_2 K_2(9+4\sqrt{3}\pi)\cos\Phi_2]].$$

By considering five further case differentiations for different displacement angles Φ_2, similar expressions are obtained. **Figure 17** shows the resulting dependency of P_{tot} on Φ_2.

[2] Index *x* indicates the independence of the input sector.

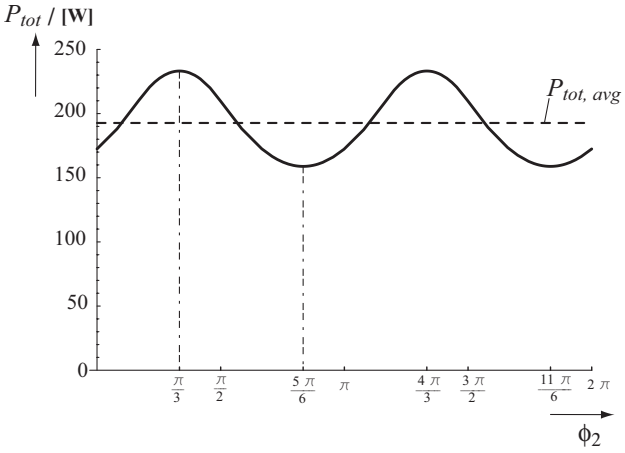

Fig.17: *Global switching losses P_{tot}* as caused by all three output phase currents in dependency on the output displacement angle. P_{tot} is relevant for the dimensioning of the heat sink. $P_{tot,\,avg}$ is the respective average value.

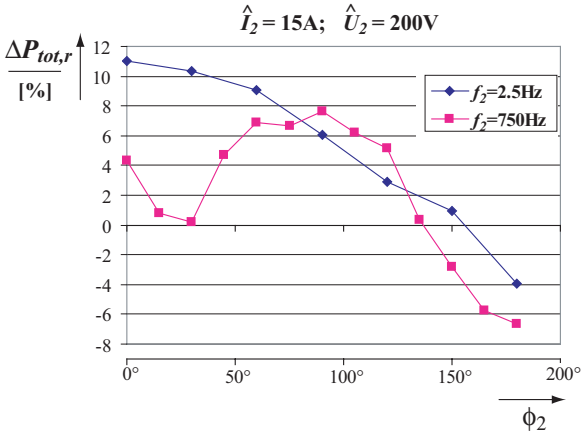

Fig.18: Relative errors (index r) of the analytically calculated g*lobal switching losses* in dependency of the displacement angle for both cases of extreme frequency proportions. Upper curve: f_1=50Hz, f_2=2.5Hz. Lower curve: f_1=50Hz, f_2=750Hz.

Thereby, the maximum value of P_{tot} can be specified as

$$\begin{aligned} &P_{tot,\max} = \\ &= \frac{3}{8\pi^2} f_s \cdot [6\sqrt{3}\pi \cdot \hat{I}_2 K_3 + \hat{U}_1^{\,2} \cdot (3\sqrt{3} + 4\pi) \cdot (\frac{9}{2}\sqrt{3}\hat{I}_2 K_2 + 2\pi K_1)] + \\ &+ \frac{1}{2}\hat{I}_2[27K_2 \cdot \hat{U}_1^{\,2} + 4\sqrt{3}\pi(K_3 + 3K_2 \cdot \hat{U}_1^{\,2})] = \\ &= 233W. \end{aligned} \tag{52}$$

This maximum does occur at a displacement angle of $\Phi_2=\pi/3$. Again, this is obvious as the current i_A in this case is switched in the vicinity of its maximum (cf. Fig.14).

The respective minimum value occurring at $\Phi_2=5\pi/6$ is

$$\begin{aligned} &P_{tot,\min} = \frac{3}{8\pi^2} f_s \cdot [8\pi \cdot \hat{I}_2 K_3 + \hat{U}_1^{\,2} \cdot [(3\sqrt{3} + 4\pi) \cdot (\frac{21}{2}\hat{I}_2 K_2 + 2\pi K_1) - \\ &- (9 + 4\sqrt{3}\pi) \cdot \frac{3}{2}\sqrt{3}\hat{I}_2 K_2]] = \\ &= 159W. \end{aligned} \tag{53}$$

Finally, by a last step of averaging the average value of the total global switching losses is obtained

$$\begin{aligned} &P_{tot,avg} = \\ &= \frac{f_s}{12\pi^2} \cdot 3\pi(3\sqrt{3} + 4\pi) \cdot \hat{U}_1^{\,2} K_1 + 4\hat{I}_2[3(3\sqrt{3} + 4\pi) \cdot \hat{U}_1^{\,2} K_2 + 4\pi K_3] = \\ &= 193W. \end{aligned} \tag{54}$$

III.C Comparison to Digital Simulation

Figure 18 depicts for both cases of extreme frequency ratios the relative errors of the analytically calculated global switching losses in dependency of the displacement angle Φ_2.

Based on the foregoing calculations the following conclusions can be drawn:

- f_2 = 2.5Hz = 1/20 f_1:
  The maximum of the relative error does occur at Φ_2=0 and is equal to 11%.
- f_2 = 750Hz = 15 f_1:
  The maximum of the relative error does occur at Φ_2=π/2 and is equal to 8%.

VI. Conclusions

In this paper the stresses on the power components of novel three-phase AC-AC matrix converter topologies, SMC, VSMC, and USMC are calculated analytically with high accuracy. This does provide an excellent basis for the dimensioning and for a comparative evaluation of the systems for a given application.

Further research is focused on the VSMC and on the zero current commutation of the rectifier section in order to achieve a low complexity of the power and of the control circuit. There, important issues are:

1) evaluation of alternative modulation schemes concerning the stresses on the power components and the derivation of a modulation scheme showing minimal switching losses for a given load current phase angle

2) application of the proposed concept for deriving analytical expression for the stresses on the power components to a CMC

3) verification of theoretical considerations by a 10kW laboratory prototype of the VSMC fully realized in SiC technology; there the input voltage will be 400V_{rms} line-to-line, the switching frequency will be set to 200kHz.

Results of the research will be published at conferences in near future.

References

[1] **Kolar, J.W., Baumann, M., Schafmeister, F., and Ertl, H.:** *Novel Three-Phase AC-DC-AC Sparse Matrix Converter.* To be published at the 17th IEEE Applied Power Electronics Conference, March 10 - 14, Dallas (TX), 2002.

[2] **Kolar, J.W.:** *Vorrichtung zur quasi-direkten pulsbreitengesteuerten Energieumformung zwischen Dreiphasennetzen.* Austrian Patent Application (in German), filed July 2001

[3] **Kolar, J.W.:** *Dreiphasiger Hybrid-Wechselspannungs-Wechselspannungs-Direktumrichter minimaler Komplexität und hoher Kommutierungssicherheit.* Austrian Patent Application (in German), filed Aug. 2001.

[4] **Kolar, J.W., Ertl, H., and Zach, F.C.:** *Calculation of the Passive and Active Component Stresses of Three-Phase PWM Converter Systems with High Pulse Rate*. Proceedings of the 3rd European Conference on Power Electronics and Applications, Aachen, Germany, Oct. 9-12, Vol. 3, pp. 1303-1311 (1989).

[5] **Baumann, M., and Kolar, J.W.:** *Comparative Evaluation of Modulation Methods for a Three-Phase/Switch Buck Power Factor Corrector Concerning the Input Capacitor Voltage Ripple.* Proceedings of the 32nd IEEE Power Electronics Specialists Conference, Vancouver/Canada, June 17 – 21, vol. 3, pp. 1327 – 1332 (2001).

[6] **Baumann, M., Stögerer, F., Kolar, J.W., and Lindemann, A.:** *Design of a Novel Multi-Chip Power Module for a Three-Phase Buck+Boost Unity Power Factor Utility Interface Supplying the Variable Voltage DC Link of a Square-Wave Inverter Drive.* Proceedings of the 16th IEEE Applied Power Electronics Conference, Anaheim, California U.S.A., March 4-8, Vol. 2, pp. 820-827 (2001).

[7] **IXYS Corporation:** *FIO 50-12BD Bidirectional Switch with IGBT and Fast Diode. Advanced technical information (2001).*

[6] **Lindemann, A.:** *A New IGBT With Reverse Blocking Capability.* Record of the 9th European Conference on Power Electronics and Applications, Graz, Austria, Aug. 27-29 (2001).

[9] **Klumpner, C., Blaabjerg, F., and Nielsen, P.:** *Speeding-up the Maturation Process of the Matrix Converter Technology*. Proceedings of the 32nd IEEE Power Electronics Specialists Conference, Vancouver, Canada, Vol. 2, pp. 1083-1088 (2001).

[10] **Kolar, J.W., Ertl, H., and Zach, F.C.:** *Influence of the Modulation Method on the Conduction and Switching Losses of a PWM Converter System*. IEEE Transactions on Industry Applications, vol. 27, No.6, pp. 1063 – 1075 (1991).

[11] **Baumann, M., and Kolar, J.W.:** *Experimental Analysis of a 5kW Wide Input Voltage Range Three-Phase Buck+Boost Power Factor Corrector.* Proceedings of the 23rd IEEE International Telecommunications Energy Conference, Edinburgh, U.K., Oct. 14-18, pp. 146-153 (2001).