Analytically Closed Calculation of the Conduction Losses of Three-Phase AC-AC Sparse Matrix Converters

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Abstract

For three-phase a.c.-a.c. power conversion a conventional matrix converter (CMC) or a d.c. side connection of a current DC link rectifier and a voltage d.c. link inverter comprising no energy storage components in the d.c. link could be employed. The combination of d.c. link converters does show a lower number of turn-off power semiconductors and, therefore, has been denoted as Sparse Matrix Converter (SMC) or Very Sparse Matrix Converter (VSMC). A limitation of the phase displacement of the current and voltage fundamentals at the input and at the output to ± π/6 does allow a further reduction of the system complexity, accordingly the respective topology has been introduced in the literature as Ultra Sparse Matrix Converter (USMC).

In this paper a novel concept for the analytical calculation of the current stresses on the power semiconductors of the Sparse Matrix Converter Topologies (SMC, VSMC, and USMC) is proposed. As a comparison to a digital simulation shows, the analytical results do show a very good accuracy in a wide modulation range and for widely varying load current phase angle and widely varying ratio of output and mains frequency. Therefore, the analytical results provide an excellent basis for the dimensioning of the SMC, VSMC or USMC and/or for the determination of the rated output power and efficiency which could be achieved by employing given power transistors and diodes.

Introduction

In [1] novel topologies of three-phase a.c.-a.c. PWM converter systems have been proposed, which do show a reduced number of power transistors and a lower control complexity as compared to a conventional matrix converter (CMC). As Fig.1 shows, the system topologies which have been denoted as Sparse Matrix Converter (SMC, cf. Fig. 1(a),[2]), Very Sparse Matrix Converter (VSMC, cf. Fig. 1(b),[3]), and Ultra Sparse Matrix Converter (USMC, cf. Fig. 1(c)) are formed by the d.c. side coupling of a current d.c. link rectifier and a voltage d.c. link inverter. There, the impression of the d.c. link voltage is by the a.c. side filtering capacitors via the rectifier stage, the d.c. link current is formed by segments of the inductive load current and is impressed via the inverter stage. Accordingly, no energy storage components have to be provided in the d.c. link.

As for the CMC the switching frequency harmonics of the SMC, VSMC, USMC input current and output voltage are suppressed by an input filter and by the inductive characteristic of the load. Therefore, for proper control mains and load current do show a sinusoidal shape. Via the d.c. link only active power is transferred, accordingly the input current displacement angle can be defined independently of the load current phase angle.

However, the formation of reactive power at the input is possible only in case a sufficiently large d.c. link current and/or an active power flow to the output is present [1]. Additionally, for the USMC the admissible current/voltage phase displacement at the input and output is limited to $\Phi_1, \Phi_2 \in \pm \pi/6$ in order to ensure a d.c. link current $i > 0$, as $i < 0$ is prevented by the rectifier stage diodes.

As for the CMC, a phase displacement Φ_1 of input current and input voltage does reduce the amplitude of the fundamental which could be formed at maximum at the output. A maximum output voltage range is given for ohmic input characteristic, i.e. for $\Phi_1 = 0$. Accordingly, all further considerations will be limited to this case.

An essential advantage of the SMC, VSMC and USMC topologies does consist in the possibility of changing the switching state of the rectifier stage at zero current. If the inverter output stage is switched into the free-wheeling state in advance to commutating the rectifier stage the d.c. link current is reduced to zero and no continuous connection of the d.c. link to the mains has to be considered for changing the rectifier switching state. Therefore, the complex multi-step commutation in dependency on the sign of the d.c. link current or in dependency on the phase voltage difference of the commutating phases [1] being characteristic for the CMC can be omitted what does result in a higher system reliability. Furthermore, the switches of the input stage of the SMC which do provide an individual controllability of both current directions can be replaced by four-quadrant switches formed by a single transistor and a diode bridge resulting in the VSMC topology (cf. Fig. 1(a) and (b)).

The aforementioned advantages do motivate a closer analysis of the novel circuit topologies. There, besides a comprehensive discussion of the basic principle of operation as given in [1], for an industrial application the stresses on the power components and/or guidelines for the dimensioning of the components and a comparison of the conduction and switching losses and/or loss balances and estimated efficiencies of the individual systems are of special interest.

In this paper the calculation of analytical approximations of the current stresses on the power components which has been treated only briefly in [1] will be discussed in detail. As a comparison to the results of a digital simulation verifies, the analytical results do

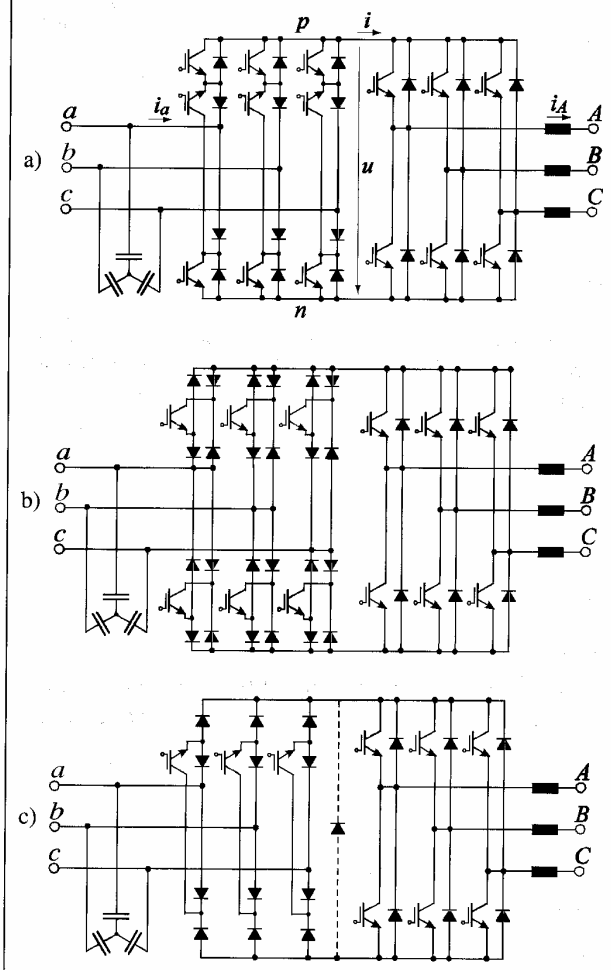

Fig.1: Basic structure of the power circuit of the:
– Sparse Matrix Converter (SMC) (a),
– Very Sparse Matrix Converter (VSMC) (b),
– and of the Ultra Sparse Matrix Converter (USMC) (c),
as proposed in [1].

show a very good accuracy in a wide modulation range and for widely varying load current phase angle and widely varying ratio of output and mains frequency. In the next section based on a brief discussion of the PWM scheme being employed in equal form for SMC, VSMC and USMC, the rms and average values of the power transistor and diode currents are calculated analytically. All analytical approximations are verified by digital simulations and the relative errors are determined in dependency on the system operating parameters. Finally, in the conclusions topics to be covered in the continuation of the research are discussed, where the transfer of the analytical calculation of the stresses on the components to the CMC, and the realization of a 10 kW SMC using SiC/Si-cascode power switches and SiC-diodes should be pointed out.

Current stresses on the power semiconductors

According to Tab.1, Fig. 2 and Fig. 3, within a π/3-wide interval of the mains period always two line-to-line voltages are switched into the d.c. link and no free-wheeling interval of the rectifier stage is considered. Accordingly, the local average value of the d.c. link voltage does show a variation with six times the mains frequency f_1. In order to achieve sinusoidally varying local average values of the inverter output phase voltages this variation has to be compensated by an inverse variation of the inverter modulation index. Accordingly, the exact calculation of the average stresses on the components being determined by the varying modulation index and by the load current amplitude and phase angle is relatively involved. The averaging interval is directly defined only in case the ratio of the mains and output frequency does constitute a rational number and in general a wide averaging interval has to be considered if the output frequency is close to the mains frequency.

In order to allow a mathematical formulation of low complexity, in a first approximation we only consider the average modulation index of the output stage and/or a global average value $\bar{U}$ of the d.c. link voltage. Thereby, the matrix converter is transferred into a constant d.c. link voltage system and the relation of mains fre-

$\varphi_1 = \omega_1 t$	u_p	u_n	u
0 ... π/6	u_a	u_b, u_c	u_{ab}, u_{ac}
π/6 ... π/2	u_a, u_b	u_c	u_{ac}, u_{bc}
π/2 ... 5π/6	u_b	u_a, u_c	u_{ba}, u_{bc}
5π/6 ... 7π/6	u_b, u_c	u_a	u_{ba}, u_{ca}
7π/6 ... 3π/2	u_c	u_a, u_b	u_{ca}, u_{cb}
3π/2 ... 11π/6	u_a, u_c	u_b	u_{ab}, u_{cb}
11π/6 ... 0	u_a	u_b, u_c	u_{ab}, u_{ac}

Table 1: Intervals of a mains voltage period, and corresponding potentials of the positive and negative d.c. link bus, u_p and u_n (given with reference to the mains star point), and d.c. link voltage u for the PWM scheme proposed in [1]. The clamping of a phase input to p or n is pointed out by a dotted areas.

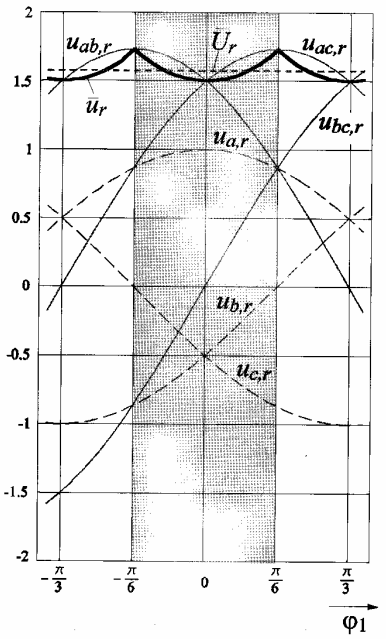

Fig. 2: Time behavior of the mains phase voltages u_a , u_b , u_c , and of the local average value $\bar{u}$ of the d.c. link voltage u; $\bar{U}$ does denote the global average value of u; voltages are normalized (index r) to the mains phase voltage amplitude $\hat{U}_1$. The considerations are limited to the angle interval $\varphi_1 \in (-\pi/6 ... \pi/6)$, which is pointed out by a dotted area.

quency and output frequency is not longer of importance. Considering the limited range of variation of the local average value $\bar{u}$ of the d.c. link voltage (cf. Fig. 2) and/or of the average d.c. link current $\bar{i}$ we could expect a sufficiently accurate approximation of the actual circuit behavior despite this drastic simplification. This is finally verified by a comparison to the results of a digital simulation (cf. Figs. 9 and 10).

Assuming a constant d.c. link voltage $\bar{U}$ and/or constant d.c. link current $\bar{I}$ the calculation of the stresses on the components can be carried out essentially equal as given in the literature for voltage d.c. link inverters and/or current d.c. link rectifiers (cf. [4], and [5]).

Two steps of current averaging have to be performed, i.e. in a first step:

– the local average value $\hat{i}$ over one pulse period is calculated based on the instantaneous value i of the d.c. link current, and in a subsequent step
– the global average value $\bar{I}$ of the d.c. link current is determined by averaging of $\hat{i}$ over a $\pi/3$-wide interval of the mains period.

The same procedure has to be applied for the calculation of the local and global d.c. link current rms values, i_{rms} and I_{rms}.

With reference to Fig. 4 it is immediately clear that the sign of the d.c. link current i has to be considered in the following investigations as the current carrying power semiconductors and/or the conduction losses are determined directly by the actual direction of i.

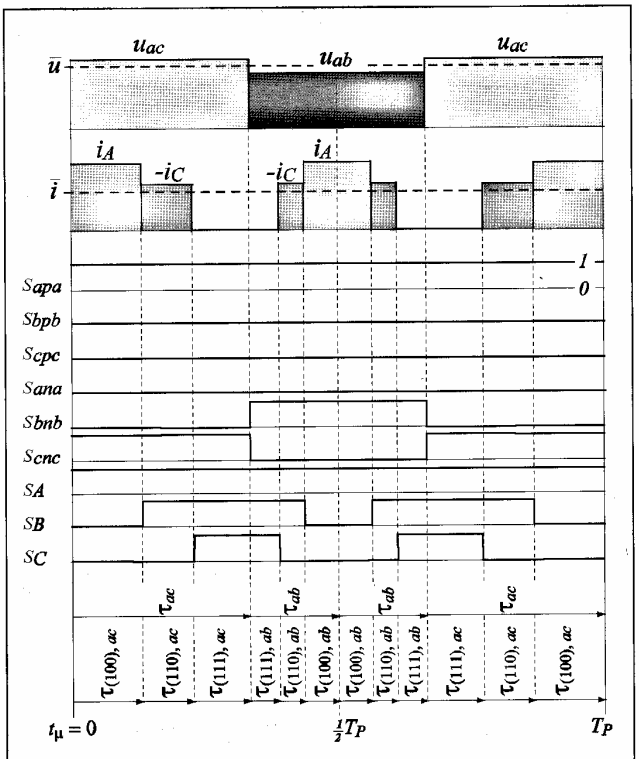

Fig. 3: Formation of the d.c. link voltage u and d.c. link current i within a pulse period and corresponding switching functions of the rectifier and inverter stage being characteristic for $\varphi_2 \in (-\pi/6...\pi/6)$ and $\varphi_2 \in (0...\pi/3)$. Switching state changes of the rectifier stage do occur at zero d.c. link current. The d.c. link current does show equal average values (denoted by $\hat{i}$) within τ_{ac} and τ_{ab}. The switching frequency ripple of the input line-to-line voltages u_{ac} and u_{ab} and of the output phase currents i_A and i_C is neglected for the sake of clarity.

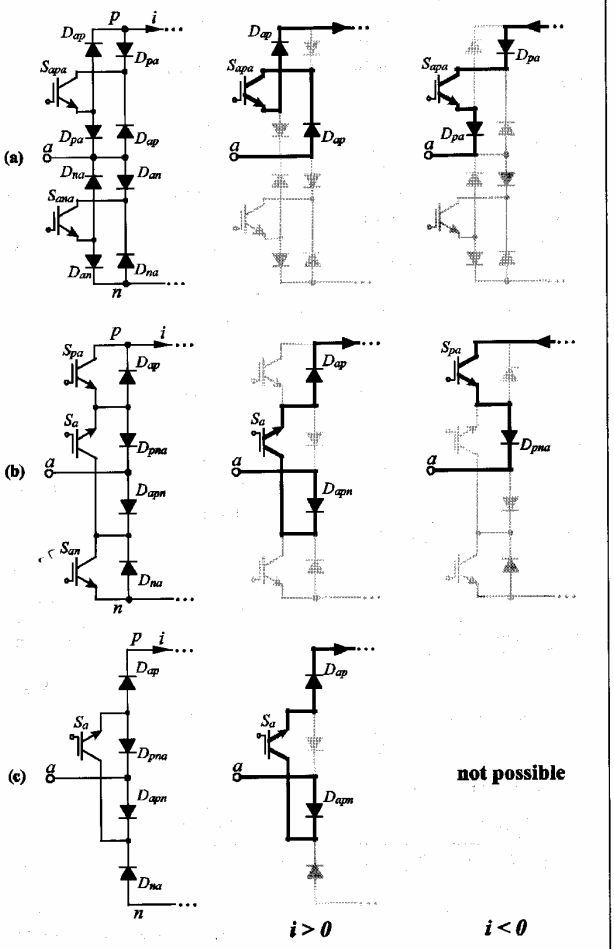

Fig.4: Structure and denomination of the diodes and power transistors of a bridge leg of the input stage of a VSMC (a), SMC (b), and USMC (c). Identical denominations of components for the different bridge leg topologies do indicate equal current stresses, e.g. the average and rms current stress on diode D_{ap} of the VSMC is identical to the current stress on diode D_{ap} of the USMC. The current paths shown by bold lines are valid for a positive and/or negative d.c. link current i in case input phase a is connected to the positive rail p of the d.c. link (as given within the considered angle intervals $\varphi_1 \in (-\pi/6...\pi/6)$ and $\varphi_2 \in (0...\pi/3)$, cf. Fig. 3). The operation of the USMC is restricted to positive d.c. link currents $i > 0$.

In general, the time behavior of i is dependent on the phase displacement Φ_2 of output current and output voltage fundamental. For the sake of clearness we will refer to the space vectors $\bar{u}_2$ and $\underline{i}_2$ (cf. Fig. 5) related to the phase quantities $\bar{u}_i$ and i_i, i = A,B,C, in the following, where $\bar{u}_i$ denotes the local average value and/or the fundamental of a phase voltage u_i. In Fig. 5 the $\pi/3$-wide interval $\varphi_2 \in (0...\pi/3)$ which will be considered for the calculation of the semiconductor conduction losses is pointed out by a dotted area.

According to [4] the d.c. link current i is determined by the output phase currents and by the inverter stage switching state and/or by the corresponding switching functions s_i, i = A,B,C (in case an

output i = A,B,C is connected to the positive d.c. bus $s_i = 1$ is valid, for the connection to the negative bus we have $s_i = 0$)

$$i = i_A s_A + i_B s_B + i_C s_C \tag{1}$$

In $\varphi_2 \in (0...\pi/3)$ the phase currents i_A and i_C which can be derived by projecting i_2 onto the corresponding phase axes A and C are involved in the formation of i. The following investigations will be limited to phase displacements $\Phi_2 \in (0...\pi/2)$ for the sake of clearness as in this case $i_C \leq 0$ is valid within $\varphi_2 \in (0...\pi/3)$. Hence, only two cases have to be distinguished:

a) $i_A \geq 0$ and/or $i > 0$ within each pulse period in $\varphi_2 \in (0...\pi/3)$. This is valid in general for $\Phi_2 \in (0...\pi/6)$ and valid in a section of $\varphi_2 \in (0...\pi/3)$ for $\Phi_2 \in (\pi/6...\pi/2)$ which is determined by $\varphi_2 + \Phi_2 \leq \pi/2$; a typical case is represented by space vector $\underline{i}_2^a$ in Fig. 5.

b) For $\varphi_2 + \Phi_2 > \pi/2$ we have $i_A < 0$ in a section of $\varphi_2 \in (0...\pi/3)$ which is determined by the actual value of $\Phi 2 \in (\pi/6...\pi/2)$. The d.c. link current i then shows positive ($i = -i_C$) and negative ($i = i_A$) values within a pulse period. A typical case is represented by current vector $\underline{i}_2^b$ in Fig. 5.

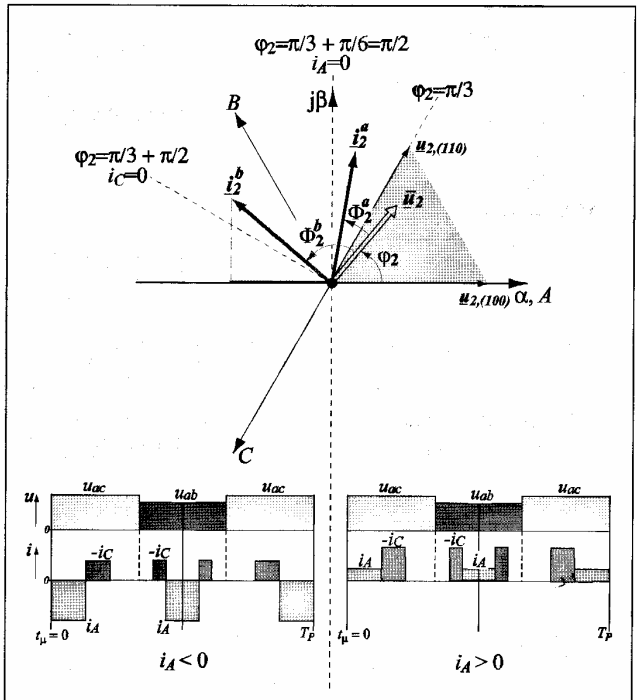

Fig. 5: Space vector $\underline{u}_2$ related to the local average values of the output phase voltages and output current space vector i_2. The considered output angle interval $\varphi_2 \in (0...\pi/3)$ where the active voltage space vectors $\underline{u}_{2,(100)}$ and $\underline{u}_{2,(110)}$ are employed for the formation of $\underline{u}_2$ is indicated by a dotted area. The phase currents i_i, i = A,B,C, are obtained by projecting $\underline{i}_2$ onto the phase axes A,B,C. Two current space vectors corresponding to different phase displacements of output voltage fundamental and output current are depicted. For both cases, the resulting time behavior of the d.c. link currents i within a pulse period is shown; i_2^a is located in right half plane, i.e. $i_A > 0$, thus $i > 0$ is valid within the whole pulse period; i_2^b is located in left half plane, accordingly we have $i_A < 0$ with i being comprised of positive and negative current segments.
If $\Phi_2 > \pi/6$ is valid, i_A and/or i will show negative values for a section of $\varphi_2 \in (0...\pi/3)$ being defined by $\varphi_2 + \Phi_2 > \pi/2$.

Global average modulation index

Neglecting the fundamental voltage drop across the inner mains impedance and/or across explicit filtering inductors connected in series on the mains side the mains voltage space vector

$$\underline{u}_1 = \hat{U}_1 \cdot e^{j\cdot\omega_1 t} \tag{2}$$

and/or the corresponding phase voltages

$$\begin{aligned} u_a &= \hat{U}_1 \cos(\varphi_1) \\ u_b &= \hat{U}_1 \cos(\varphi_1 - \frac{2\pi}{3}) \\ u_c &= \hat{U}_1 \cos(\varphi_1 + \frac{2\pi}{3}) \end{aligned} \tag{3}$$

are impressed at the system input side. There $\varphi_1 = \omega_1 t$ denotes the phase and/or the position within a mains period.

The system output current which is assumed to show a purely sinusoidal shape is impressed by the inductive behavior of the load and should be represented by a current space vector

$$\underline{i}_2 = \hat{I}_2 \cdot e^{j\cdot(\omega_2 t + \Phi_2)} \tag{4}$$

and/or by the corresponding phase currents

$$\begin{aligned} i_A &= \hat{I}_2 \cos(\varphi_2 + \Phi_2) \\ i_B &= \hat{I}_2 \cos(\varphi_2 - \frac{2\pi}{3} + \Phi_2) \\ i_C &= \hat{I}_2 \cos(\varphi_2 + \frac{2\pi}{3} + \Phi_2) \end{aligned} \tag{5}$$

According to [1], Fig. 2 and (3) we have within the considered $\pi/3$-wide interval of the mains period $\varphi_1 \in (-\pi/6...\pi/6)$ for the local average value $\bar{u}$ of the d.c. link voltage

$$\bar{u} = \frac{3}{2}\hat{U}_1 \frac{1}{\cos(\varphi_1)} \cdot \tag{6}$$

Therefore, the global average value of d.c. link voltage can be calculated as

$$\bar{U} = \frac{1}{\pi/3}\int_{-\pi/6}^{\pi/6} \bar{u}\,d\varphi_1 = \frac{9}{\pi}\ln(\sqrt{3})\hat{U}_1. \tag{7}$$

The inverter stage modulation index results as

$$m_2 = \frac{\hat{U}_2}{\frac{1}{2}\bar{u}} = \frac{4}{3}\frac{\hat{U}_2}{\hat{U}_1}\cdot\cos(\varphi_1). \tag{8}$$

With reference to [1] the local average value of the d.c. link current is

$$\bar{i} = \hat{I}_2 \frac{\hat{U}_2}{\hat{U}_1}\cos(\varphi_1)\cdot\cos(\Phi_2) \tag{9}$$

resulting in a global average value of

$$\bar{I} = \frac{3}{\pi}\int_{-\pi/6}^{\pi/6} \bar{i}\,\mathrm{d}\varphi_1 = \frac{3}{\pi}\cdot\frac{\hat{U}_2}{\hat{U}_1}\cdot\hat{I}_2\cos(\Phi_2). \tag{10}$$

By defining a global modulation index

$$M_2 = \frac{3}{\pi}\int_{-\pi/6}^{\pi/6} m_2\mathrm{d}\varphi_1 = \frac{4}{\pi}\cdot\frac{\hat{U}_2}{\hat{U}_1} \tag{11}$$

the global average value of the d.c. link current can be expressed as

$$\bar{I} = \frac{3}{4}M_2\hat{I}_2\cos(\Phi_2). \tag{12}$$

There, one has to note that the global modulation index M_2 according to (11) shows only a minor difference to a definition according to (8), i.e. we have

$$\frac{\hat{U}_2}{\frac{1}{2}\bar{U}} \approx M_2 \tag{13}$$

(the relative difference of the definitions according to (11) and (8) considering (7) is 0.18 %).

According to Fig.3, in the considered interval $\varphi_2 = (0...\pi/3)$ the active switching states $s_{ABC} = (100)$ and (110) are employed for output voltage formation. Therefore, we have for the d.c. link current

$$i = \begin{cases} i_A & \text{for } s_{ABC} = (100) \text{ e.g. within } \tau_{(100),ac} \\ i_A + i_B = -i_C & \text{for } s_{ABC} = (110) \text{ e.g. within } \tau_{(110),ac} \end{cases} \tag{14}$$

and the local rms value of the d.c. link current is defined by

$$i^2{}_{rms} = \frac{1}{\tau_{ac}}\cdot[\int_{\tau_{(100),ac}} i_A{}^2\mathrm{d}t_\mu + \int_{\tau_{(110),ac}} i_C{}^2\mathrm{d}t_\mu]. \tag{15}$$

(as in τ_{ac} and τ_{ab} the active switching states show equal relative on-times [1] one also could refer to the section τ_{ab} of a pulse period, cf. Fig. 3, for the calculation of i^2_{rms}).

Due to the neglection of the ripple components of the output phase currents (cf. (5), [4]) i_A and i_C show an approximately constant value within a pulse period for pulse frequencies being considerably higher than the output frequency; accordingly, (15) results in

$$i_{rms}{}^2 = \delta_{(100)}(\varphi_1,\varphi_2)\cdot i_A{}^2(\varphi_2) + \delta_{(110)}(\varphi_1,\varphi_2)\cdot i_C{}^2(\varphi_2) \tag{16}$$

where, with reference to [1], the duty cycles $\delta_{(100)}$ and $\delta_{(110)}$ are defined as

$$\delta_{(100)}(\varphi_1,\varphi_2) = \frac{\tau_{(100),ac}}{\tau_{ac}} = \frac{\sqrt{3}}{2}m_2(\varphi_1)\cdot\cos(\varphi_2+\frac{\pi}{6})$$
$$\delta_{(110)}(\varphi_1,\varphi_2) = \frac{\tau_{(110),ac}}{\tau_{ac}} = \frac{\sqrt{3}}{2}m_2(\varphi_1)\cdot\sin(\varphi_2). \tag{17}$$

For eliminating the dependency of i^2_{rms} on φ_1 we now replace the local modulation index $m_2(\varphi_1)$ by the global average modulation index M_2 (cf. (11)) in a first approximation. The global rms value of the d.c. link current then directly follows as

$$I_{rms}{}^2 = \frac{3}{\pi}\int_0^{\pi/3}[\delta_{(100)}(\varphi_2)\cdot i_A{}^2(\varphi_2) + \delta_{(110)}(\varphi_2)\cdot i_C{}^2(\varphi_2)]\mathrm{d}\varphi_2 =$$
$$= \frac{\sqrt{3}}{\pi}M_2\hat{I}_2{}^2[\frac{1}{4}+\cos^2(\Phi_2)]. \tag{18}$$

Components of the global d.c. link current average value

With reference to Fig. 4, for calculating the conduction losses of the power semiconductors the d.c. link current i has to be split into a positive component i_+ ($i_+ = i$ for $i > 0$ and $i_+ = 0$ for $i \le 0$) and a negative component i_- ($i_- = -i$ for $i \le 0$ and $i_- = 0$ for $i > 0$). There, as detailed in connection with Fig. 5, the cases $\Phi_2 \in (0...\pi/6)$ and $\Phi_2 \in (\pi/6...\pi/2)$ have to be distinguished.

Phase displacement $\Phi_2 \in (0...\pi/6)$ - case (a)

For $\Phi_2 \in (0...\pi/6)$ the d.c. link current is comprised of only positive output current segments, i.e. we have within each pulse period $i > 0$. Accordingly,

$$\bar{I}_+ = \bar{I} \quad \text{and} \quad \bar{I}_- = 0 \tag{19}$$

is valid ($\bar{I}_+$ does denote the global average value of the positive components i_+ of i, $\bar{I}_-$ does denote the global average value of the negative components). Due to $i > 0$ the diodes D_{pa} will not be involved in the current conduction.

Phase displacement $\Phi_2 \in (\pi/6...\pi/2)$ - case (b)

Considering (1) and (14) we can write for the local average value of the d.c. link current in analogy to (16)

$$\bar{i} = \delta_{(100)}(\varphi_1,\varphi_2)\cdot i_A(\varphi_2) + \delta_{(110)}(\varphi_1,\varphi_2)\cdot i_C(\varphi_2) \tag{20}$$

(considering (5) and (17), (20) does result in (9)). As can be seen from Fig. 5, for a position

$$\varphi_2 = \pi/2 - \Phi_2 \tag{21}$$

of the output voltage space vector $\bar{u}_2$ the output phase current i_A crosses zero what does result in a negative value of $\delta_{(100)}\, i_A$ in (20) for $\varphi_2 > \pi/2 - \Phi_2$.

Hence, we have for the global average value of the positive d.c. link current component i_+ which is carried e.g. by the diodes D_{ap}

$$\bar{I}_+ = \frac{3}{\pi}[\int_0^{\pi/3}(-i_C)\cdot\delta_{(110)}(\varphi_1,\varphi_2)\mathrm{d}\varphi_2 + \int_0^{\pi/2-\Phi_2} i_A\cdot\delta_{(100)}(\varphi_1,\varphi_2)\mathrm{d}\varphi_2] =$$
$$= \frac{3}{4}M_2\hat{I}_2[\cos\Phi_2 + \frac{\sqrt{3}}{\pi}((\frac{\pi}{6}-\Phi_2)\sin(\frac{\pi}{3}+\Phi_2)+\sin(\Phi_2-\frac{\pi}{6}))]. \tag{22}$$

and accordingly, for the global average value of the negative component i_- of i

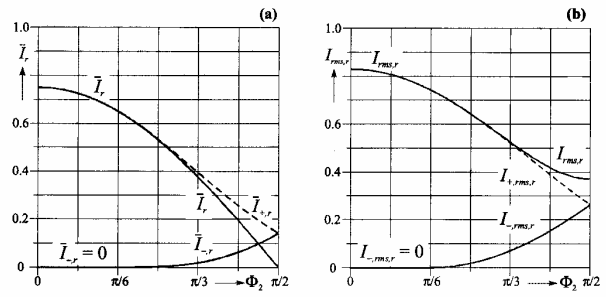

Fig. 6: Graphical representation of the normalized dependency (index r) of the global average value (a) and of the global rms value (b) of the total d.c. link current i and of the d.c. link current components i_+ and i_- on the output current phase displacement Φ_2. Normalization basis: $M_2\hat{I}_2$ (for (a)) and $\sqrt{M_2\hat{I}_2}$ (for (b)).

$$\bar{I}_- = \frac{3}{\pi}\int_{\pi/2-\Phi_2}^{\pi/3}(-i_A)\delta_{(100)}\mathrm{d}\varphi_2 = \\ = \frac{3\sqrt{3}}{4\pi}M_2\hat{I}_2[(\frac{\pi}{6}+\sqrt{3}-\Phi_2)\sin(\Phi_2+\frac{\pi}{3})-2\cos\Phi_2] \quad (23)$$

where

$$\bar{I} = \bar{I}_+ - \bar{I}_- \quad (24)$$

is valid. (As in (18), in (22) and (23) the local modulation index m_2 has been replaced by global modulation index M_2 in order to eliminate the dependency on φ_1) (Fig. 6).

Components of the global d.c. link current RMS value

Phase displacement $\Phi_2 \in (0...\pi/6)$ - case (a)

As is immediately clear from the considerations in case (a) above we have for the global rms value of the d.c. link current components

$$I_{\mathrm{rms}}{}^2 = I_{+,\mathrm{rms}}{}^2 \quad (25)$$

and

$$I_{-,\mathrm{rms}}{}^2 = 0 \cdot \quad (26)$$

Phase displacement $\Phi_2 \in (\pi/6...\pi/2)$ - case (b)

In analogy to case (b) above we have

$$I_{+,\mathrm{rms}}{}^2 = \frac{3}{\pi}[\int_0^{\pi/3} i_C{}^2\cdot\delta_{(110)}\mathrm{d}\varphi_2 + \int_0^{\pi/2-\Phi_2} i_A{}^2\cdot\delta_{(100)}\mathrm{d}\varphi_2] = \\ = \frac{\sqrt{3}}{\pi}M_2\hat{I}_2{}^2[\sin(\Phi_2+\frac{\pi}{3})-\frac{\sqrt{3}}{4}\sin(2\Phi_2-\frac{\pi}{3})] \quad (27)$$

and

$$I_{-,\mathrm{rms}}{}^2 = \frac{3}{\pi}\int_{\pi/2-\Phi_2}^{\pi/3} i_A{}^2\cdot\delta_{(100)}\mathrm{d}\varphi_2 = \\ = \frac{\sqrt{3}}{\pi}M_2\hat{I}_2^2[\frac{3}{4}+\frac{1}{4}\sin(2\Phi_2+\frac{\pi}{6})-\sin(\Phi_2+\frac{\pi}{3})] \quad (28)$$

where

$$I_{\mathrm{rms}}{}^2 = I_{+,\mathrm{rms}}{}^2 + I_{-,\mathrm{rms}}{}^2 \quad (29)$$

is valid as i_+ and i_- do not overlap in time.

Stresses on the power semiconductors of the input stage

Phase Displacement $\Phi_2 \in (0...\pi/6)$ - case(a)

Current average values

Due to the symmetric distribution of the d.c. link current i to the rectifier bridge legs we have

$$\bar{I}_{\mathrm{Dap}} = \frac{1}{3}\bar{I} = \frac{1}{4}M_2\hat{I}_2\cos\Phi_2 \\ \bar{I}_{\mathrm{Sapa}} = \bar{I}_{\mathrm{Dpna}} = \bar{I}_{\mathrm{Dap}} \\ \bar{I}_{\mathrm{Sa}} = 2\bar{I}_{\mathrm{Dap}}. \quad (30)$$

According to $i > 0$ the diodes D_{pa}, D_{an} and the switches S_{pa}, S_{an} do not participate in the current conduction, i.e. $i_{\mathrm{Dpa}} = i_{\mathrm{Spa}} = 0$ and/or

$$\bar{I}_{\mathrm{Dpa}} = \bar{I}_{\mathrm{Spa}} = 0 \quad (31)$$

is valid.

Current rms values

In analogy to the calculation of the current average values we have

$$I_{\mathrm{Dap,rms}}{}^2 = \frac{1}{3}I_{\mathrm{rms}}{}^2 = \frac{1}{\sqrt{3}\pi}M_2\hat{I}_2{}^2(\frac{1}{4}+\cos^2\Phi_2) \\ I_{\mathrm{Sapa,rms}}{}^2 = I_{\mathrm{Dpna,rms}}{}^2 = I_{\mathrm{Dap,rms}}{}^2 \\ I_{\mathrm{Sa,rms}}{}^2 = 2I_{\mathrm{Dap,rms}}{}^2 \quad (32)$$

and

$$I_{\mathrm{Dpa,rms}} = I_{\mathrm{Spa,rms}} = 0 \cdot \quad (33)$$

Phase Displacement $\Phi_2 \in (\pi/6...\pi/2)$ - Case(b)

Current average values

Positive components i_+ of i are carried by the diodes D_{ap}, negative components i_- of i are taken over by the diodes D_{pa}. Accordingly, there results for the global average current stresses on the devices

$$\bar{I}_{\mathrm{Dap}} = \frac{1}{3}\bar{I}_{+} = \frac{1}{4}M_2\hat{I}_2[\cos\Phi_2 + \\ + \frac{\sqrt{3}}{\pi}((\frac{\pi}{6}-\Phi_2)\sin(\frac{\pi}{3}+\Phi_2)+\sin(\Phi_2-\frac{\pi}{6}))]$$

$$\bar{I}_{\mathrm{Dpa}} = \frac{1}{3}\bar{I}_{-} = \frac{\sqrt{3}}{4\pi}M_2\hat{I}_2[(\frac{\pi}{6}+\sqrt{3}-\Phi_2)\sin(\Phi_2+\frac{\pi}{3})-2\cos\Phi_2]$$

$$\bar{I}_{\mathrm{Sapa}} = \bar{I}_{\mathrm{Dpna}} = (\bar{I}_{\mathrm{Dap}} + \bar{I}_{\mathrm{Dpa}}) \qquad (34)$$

$$\bar{I}_{\mathrm{Sa}} = 2\bar{I}_{\mathrm{Dap}}$$

$$\bar{I}_{\mathrm{Spa}} = \bar{I}_{\mathrm{Dpa}}$$

Current rms values

In analogy to the calculation of the current average values we have

$$I_{\mathrm{Dap,rms}}{}^2 = \frac{1}{3}I_{+,\mathrm{rms}}{}^2 = \frac{1}{\sqrt{3}\pi}M_2\hat{I}_2{}^2[\sin(\Phi_2+\frac{\pi}{3})-\frac{\sqrt{3}}{4}\sin(2\Phi_2-\frac{\pi}{3})]$$

$$I_{\mathrm{Dpa,rms}}{}^2 = \frac{1}{3}I_{-,\mathrm{rms}}{}^2 = \frac{1}{\sqrt{3}\pi}M_2\hat{I}_2{}^2[\frac{3}{4}+\frac{1}{4}\sin(2\Phi_2+\frac{\pi}{6})-\sin(\Phi_2+\frac{\pi}{3})]$$

$$I_{\mathrm{Sapa,rms}}{}^2 = I_{\mathrm{Dpna,rms}}{}^2 = (I_{\mathrm{Dap,rms}}{}^2 + I_{\mathrm{Dpa,rms}}{}^2) = \frac{1}{3}I_{\mathrm{rms}}{}^2$$

$$= \frac{1}{\sqrt{3}\pi}M_2\hat{I}_2{}^2(\frac{1}{4}+\cos^2\Phi_2)$$

$$I_{\mathrm{Sa,rms}}{}^2 = 2I_{\mathrm{Dap,rms}}{}^2$$

$$I_{\mathrm{Spa,rms}}{}^2 = I_{\mathrm{Dpa,rms}}{}^2. \qquad (35)$$

Stresses on the power semiconductors of the output stage

For the analytical calculation of the conduction losses the inverter output stage is treated as voltage source inverter with a constant input voltage $\bar{U}$ and constant global average modulation index M_2 (cf. (11)). This simplification is near at hand and does a priori neglect the actual variation of the inverter stage modulation index with six times the mains frequency (cf. (8)) which would be averaged out in any case in the course of the calculation of the global current average and rms values. A comparison of the results to the actual current stresses determined by a digital simulation finally justifies this considerable simplification.

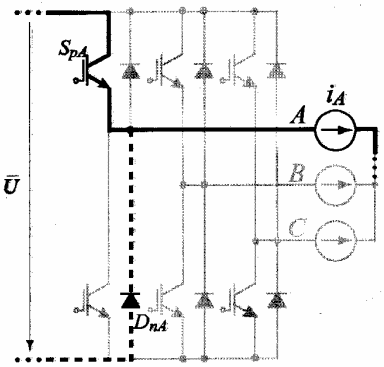

Fig. 7: Structure of the output stage of the SMC, VSMC, and USMC. The current impressing inductive load is replaced by current sources. For $i_A > 0$ power transitor S_{pA} and diode D_{nA} are involved in current conduction (see current paths pointed out by bold lines).

Due to the symmetries of the output stage circuit topology the investigation can be limited to the analysis of a transistor and the corresponding free-wheeling diode, e.g. to S_{pA} and D_{nA} of phase leg A. As the results derived in the following are valid for any transistor and any diode of the output stage, the denominations S_A and D_A instead of S_{pA} and D_{nA} will be used in the following. There, the index A should refer to the output stage in general and should not indicate that the results are restricted to bridge leg A.

Power transistor

For calculating the conduction losses of S_A we have to consider the fundamental of the output voltage of the phase A (cf. (4))

$$u_A = \hat{U}_2 \cdot \cos(\varphi_2) \qquad (36)$$

and/or the corresponding relative on-time of S_A

$$d_{SA} = \frac{1}{2} + \frac{1}{2}\frac{u_A}{\bar{U}/2}. \qquad (37)$$

With reference to (13) and (36) we then have

$$d_{SA} = \frac{1}{2} + \frac{1}{2}M_2 \cdot \cos(\varphi_2). \qquad (38)$$

As the modulation index of the output stage shows equal values in the sections τ_{ac} and τ_{ab} of a pulse period T_P (cf. Fig. 3), d_{SA} is representative for the whole pulse period and the current flow in S_A can be approximated as shown in Fig. 8.

Assuming a high switching frequency $f_P = 1/T_P$, the phase current i_A can be treated as being approximately constant within one pulse period and we get for the local average value of i_{SA} [4]

$$\bar{i}_{SA} = \frac{1}{T_P}\int_{t_0-\frac{T_P}{2}}^{t_0+\frac{T_P}{2}} i_{SA}\,\mathrm{d}t_\mu = \frac{1}{T_p}\cdot i_A \int_{t_0-d_{SA}\frac{T_P}{2}}^{t_0+d_{SA}\frac{T_P}{2}} \mathrm{d}t_\mu = i_A(\varphi_2)\cdot d_{SA}(\varphi_2). \qquad (39)$$

The global average value of i_{SA} (related to an output voltage period) then follows from averaging over the interval where S_A is participating in the current conduction and/or where $i_A > 0$ is valid (cf. Fig. 7)

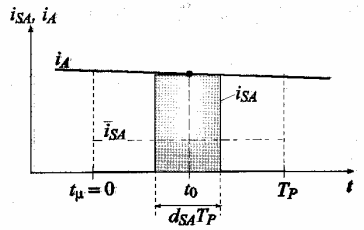

Fig. 8: Approximation of the current flow in S_A within one pulse period T_P and related local transistor current average value $\bar{i}_{SA}$.

$$\bar{I}_{SA} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}-\phi_2}^{\frac{\pi}{2}-\phi_2} \bar{i}_{SA}(\varphi_2)\mathrm{d}\varphi_2 = \frac{1}{2}\hat{I}_2\left(\frac{1}{\pi} + \frac{1}{4}M_2 \cdot \cos(\Phi_2)\right). \quad (40)$$

For the global rms value of the power transistor current, results are based on analogous considerations

$$I_{SA,rms}{}^2 = \hat{I}_2{}^2\left(\frac{1}{8} + \frac{1}{3\pi}M_2 \cos\Phi_2\right) \quad (41)$$

Power diode

According to the assumption of a continuous output current (cf. (5)) the relative on-time of the power diode D_A is determined by d_{DA} where we have $d_{DA} = 1 - d_{SA}$. The global average value and global rms value of i_{DA} can then be calculated analogously to (40) as

$$\bar{I}_{DA} = \frac{1}{2}\hat{I}_2\left(\frac{1}{\pi} - \frac{1}{4}M_2 \cdot \cos(\Phi_2)\right)$$
$$I_{DA,rms}{}^2 = \hat{I}_2{}^2\left(\frac{1}{8} - \frac{1}{3\pi}M_2 \cos\Phi_2\right). \quad (42)$$

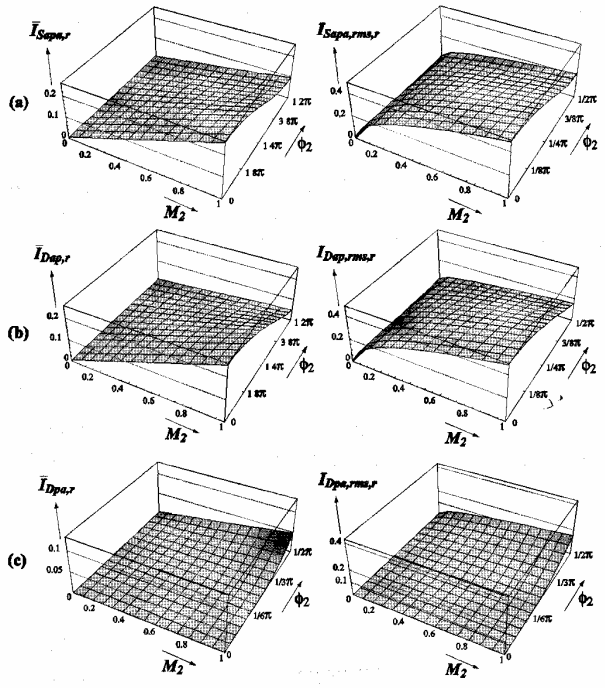

Fig. 9: Normalized representation (index r, normalization basis $\hat{I}_2$) of the analytical results derived for the current stresses on the power semiconductors of the VSMC input stage; (a) transistor S_{apa} which conducts current independently of the direction of i; (b) diode D_{ap} conducting current for $i > 0$; (c) diode D_{pa} conducting current for $i < 0$. The average current stresses on the components are shown on the left hand side, rms current stresses are depicted on the right hand side.

Graphical representation of the results of the analytical calculations

The results of the analytical calculation of the current stresses on the input stage power semiconductors of the SMC, VSMC, and USMC performed above are depicted in Fig. 9 exemplarly for the VSMC.

According to the linear dependency of the relative on-time of the active switching states of the output stage which do result in a d.c. link current i there is a linear dependency of average current values and of the square of the rms current values on the global modulation index M_2.

For $\Phi_2 = 0$ and $M_2 > 0.8$ and/or for maximum power transfer via the d.c. link the average stress on S_{apa} and D_{ap} is approximately equal to $0.2\hat{I}_2$, while the rms value is in a first approximation equal to $0.4\hat{I}_2$ (D_{pa} is not carrying any current in this case).

For increasing output current phase displacement Φ_2 there follows a reduction of the current stresses on S_{apa} and D_{ap} corresponding to the reduction of the power transferred from the input to the output.

As for $\Phi_2 > \pi/6$ negative components of i do occur the average current stress on D_{pa} does increase starting from 0 at $\Phi_2 = \pi/6$ and does reach a maximum of approximately $0.05\hat{I}_2$ at $\Phi_2 = \pi/2$ and $M_2 = 1.0$. In this case the rms current stress on D_{pa} is approximately equal to $0.15\hat{I}_2$.

Comparaison to digital simulation

The analytical results derived above have been verified with excellent consistency by extensive digital simulations within a wide operating range characterized by the ratio of the input frequency f_1 and output frequency f_2, by the output stage modulation index M_2 and by the output current phase displacement Φ_2.

For limiting to the essentials only the relative deviation of the analytical results for the VSMC and for the output stage from the results of the digital simulations are compiled in Figs. 10 and 11. There, the employed current reference value I_{Ref} is related to a nominal output power

$$P_{2N} = \frac{3}{2}\hat{U}_2\hat{I}_2 \cos\Phi_2 = 10 \text{ kW}. \quad (43)$$

With $\Phi_2 = 0$ and the maximal feasible output voltage amplitude

$\hat{U}_2 = \hat{U}_{2,max} = \sqrt{3}/2\hat{U}_1 (\hat{U}_1 = 325 \text{ V})$ we have

$$I_{Ref} = \frac{4}{3\sqrt{3}}\frac{P_{2N}}{\hat{U}_1} = 23.67 \text{ A}. \quad (44)$$

Remark: As for the analytical calculations purely sinusoidal output currents also have been employed in the digital simulations. Including the output current ripples would introduce two further parameters (load inductances and switching frequency) and would not allow to gain a clear picture of the influence of the main simplification used in the analytical calculations, i.e. of the approximation of the time-varying output stage modulation index by a constant global average value M_2.

According to Figs. 10 and 11 the relative deviations of the analytical calculations from the results of a digital simulation for S_{apa} and D_{ap} are limited to about 5 % in a wide operating range. Only for $M_2 < 0.2$ and $\Phi_2 = \pi/2$ larger errors do occur.

The relatively low accuracy of the analytically calculated current stress on D_{pa} has to be seen in connection with the low absolute

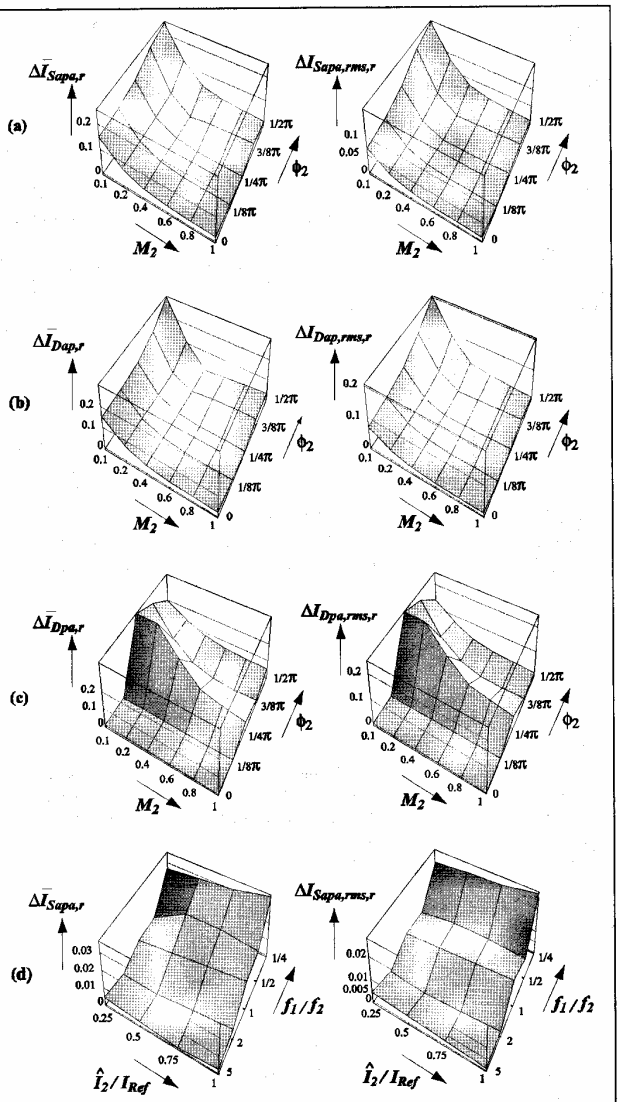

Fig. 10: Relative deviation of the analytically calculated current stresses on the power semiconductors S_{apa} (cf. (a)), D_{ap} (cf. (b)), and D_{pa} (cf. (c)) of the VSMC from the results of a digital simulation in dependency on the output stage global average modulation index M_2 and the output current phase displacement Φ_2 for $f_1/f_2 = 1/2, f_1 = 50$ Hz, $\hat{U}_1 = 325$ V and $\hat{I}_2/I_{Ref} = 3/4$. Average current stresses are shown on the left hand side; rms current stresses are depicted on the right hand side. Furthermore shown in (d): Influence of a varying frequency ratio f_1/f_2 on the relative deviation for transistor S_{apa} in dependency on the normalized output current amplitude (normalization basis: $I_{Ref} = 4P_N/(3\sqrt{3}\hat{U}_1) = 23.67A$) and on the input and output frequency ratio (for $M_2 = 0.8$, $\Phi_2 = 3\pi/8, f_1 = 50$ Hz, $\hat{U}_1 = 325$ V).

value of $\bar{I}_{Dpa}$ and $I_{Dpa,rms}$ (cf. Fig. 9(c)). Therefore, the impact of an approximation of given value is higher as compared to the higher absolute values of the current stresses on S_{apa} and D_{ap}.

Furthermore, according to Fig. 11(c) a changing output current fundamental amplitude $\hat{I}_2$ does not result in a deviation of the results of the analytical calculations and the digital simulations.

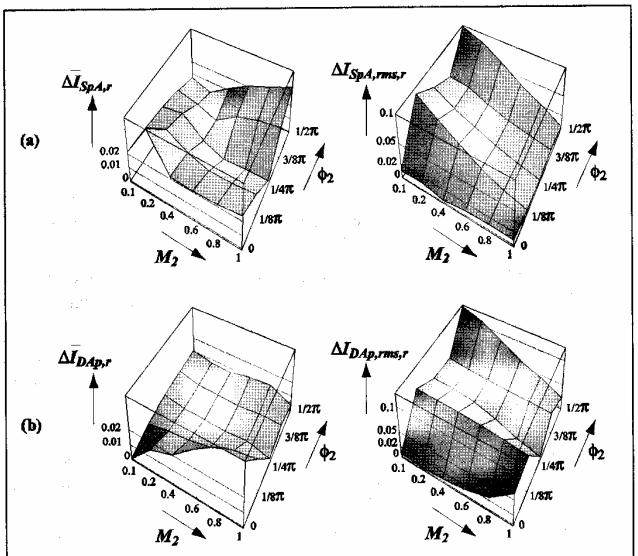

Fig. 11: Relative deviation of the analytically calculated current stresses on the output stage power semiconductors S_A (cf. (a)), and D_A (cf. (b)) from the results of a digital simulation in dependency on the output stage global average modulation index M_2 and the output current phase displacement Φ_2 for $f_1/f_2 = 1/2, f_1 = 50$ Hz, $\hat{U}_1 = 325$ V and $\hat{I}_2/I_{Ref} = 3/4$. Average current stresses are shown on the left hand side, rms current stresses are depicted on the right hand side.

Also, the deviation does not exceed about 3 % within a wide output frequency range of 10...200 Hz ($f_1 = 50$ Hz).

For the output stage power semiconductors S_A and D_A the deviation of the analytically calculated current stresses from the results of a digital simulation is very low, i.e. about 2 % for the current average values and about 5% for the current rms values.

Therefore, in summary the analytical calculations do provide an excellent basis for the dimensioning of the SMC, VSMC and USMC power circuit concerning conduction losses.

Conclusions

In this paper the stresses on the power components of novel three-phase a.c.-a.c. matrix converter topologies, SMC, VSMC, and USMC, are calculated analytically with high accuracy. This does provide an excellent basis for the dimensioning and for a comparative evaluation of the systems for a given application.

Further research is focused on the VSMC in order to achieve a low complexity of the power and of the control circuit. There, important issues are the:

– evaluation of alternative modulation schemes concerning the stresses on the power components and the derivation of a modulation scheme showing minimal switching losses for a given load current phase angle;
– application of the proposed concept for deriving analytical expression for the stresses on the power components to a CMC;
– verification of theoretical considerations by a 10 kW laboratory prototype of the VSMC fully realized in SiC technology; there the input voltage will be 400 V_{rms} line-to-line, the switching frequency will be set to 200 kHz.

Results of the research will be published at conferences in near future.

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