An Ultra Sparse Matrix Converter with a Novel Active Clamp Circuit

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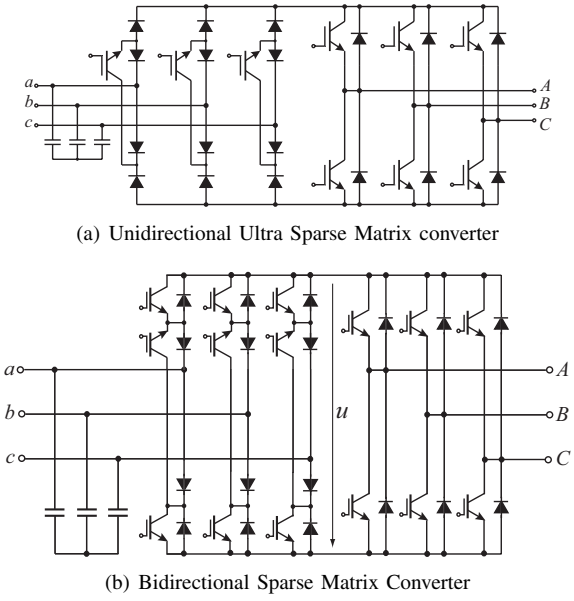
***Abstract*— The Ultra Sparse Matrix Converter (USMC) is a AC-DC-AC converter that requires only 9 power switches compared to the 18 switches required for a conventional matrix converter. The simplified input switch configuration restricts this converter to unidirectional power flow applications in which the maximum displacement angle between input and output voltages and currents is $\pm\pi/6$. A novel clamp circuit is therefore used to protect the converter from overvoltages incurred under regeneration conditions. This paper presents the design of a 5.5 kVA USMC which uses space vector modulation in combination with a zero current commutation scheme at the input rectifier stage. The design of the system is detailed and the hardware implementation of the converter is described. Experimental results demonstrate the operation of the clamp circuit and show that the converter draws sinusoidal currents from the input and supplies sinusoidal currents to the output with a conversion efficiency of up to 94%.**

***Index Terms*— Active clamp, matrix converter, reverse current, ultra sparse.**



(a) Unidirectional Ultra Sparse Matrix converter

(b) Bidirectional Sparse Matrix Converter

Fig. 1. Reduced switch indirect matrix converter topologies

I. Introduction

The interest in matrix converters is increasing since they can convert AC-AC without using large electrolytic storage capacitors as conventional back to back converters do [1]. Matrix converters consequently offer higher reliability and reduced size and weight since they are essentially an 'all-silicon' converter [2]. A matrix converter that is of particular interest is the indirect matrix converter (IMC) since its two-stage structure affords simpler switch commutation requirements and a simplified modulation strategy [3].

From the IMC topology, a number of novel sparse converter topologies can be derived [3]. These topologies, the sparse, very sparse and ultra sparse matrix converter, are functionally-equivalent to the standard IMC converter but have a reduced number of input switches. The ultrasparse matrix converter (USMC), shown in Fig. 1(a), is the most simple form of the IMC, comprising only 9 individual switches and 18 diodes. The USMC itself is a variant of the sparse matrix converter (SMC), shown in Fig. 1(b).

The USMC and SMC operate by creating a dc link, u, with the input stage and by using the output stage to provide inversion. The converter is switched using a modulation strategy which synchronizes the switching of the input and output stages to reduce switching losses. The output switches are set into a free-wheeling state during input transitions to allow zero-current switching of the input stage. Since the output stage makes two transitions for each input cycle, it effectively operates at twice the frequency of the input stage.

The main difference between the IMC and SMC is that the USMC only permits unidirectional power flow due to the arrangement of the input switches. An additional clamp circuit is consequently employed to protect the converter from experiencing excessive voltages under regeneration conditions. Clamp circuits for matrix converters have previously been presented [4], [5]; however, the clamp circuit presented in this paper uses an active topology to achieve a greater degree of controllability. The active clamp circuit is integrated with the auxiliary power supply capacitor since this configuration offers advantages such as the ability to achieve controlled ride-through during power outages.

Although the inability to sustain reverse power flow may be viewed as a disadvantage, one niche field of application that can use this feature to its advantage is the aerospace industry, as stringent regulations prohibit reverse power flow into an aircraft's power system. For this application, the USMC is typically required to convert a variable frequency ac input of 360 to 800 Hz into a variable frequency output for motor

loads. The reliability and compact size afforded by the matrix topology make it well-suited for this area of application.

In this paper, the design of a USMC is presented. The complete specifications for the USMC design are given in Table I. The converter has a thermal rating of up to 5.5 kVA and operates at a switching frequency of 50 kHz to ensure high-quality current waveforms are produced for aerospace-type applications as the input and output frequencies increase. This paper explains the operation of the USMC, describes the hardware implementation of the converter and presents the operating principles and design of the clamp circuit. Experimental results are included to demonstrate the performance of the converter with a resistive-inductive (RL) and permanent magnet (PM) motor load.

TABLE I
SYSTEM SPECIFICATIONS

Input voltage	3 x 230 Vrms, 50 Hz
Output voltage	3 x 0-199 Vrms, 0-200 Hz
Power rating	5.5 kVA
Input stage switching frequency	25 kHz
Output stage switching frequency	50 kHz

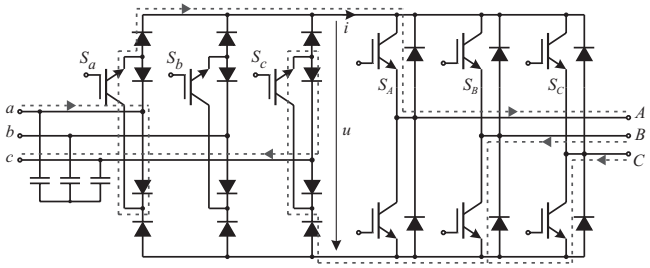
II. PRINCIPLE OF OPERATION

In a conventional matrix converter, a complex, multi-step commutation strategy is employed to prevent short-circuits between the input phases and open circuits in the output phases [2]. However, with the USMC, a simpler zero dc link current commutation scheme can be used since the converter is separated into input and output stages [3]. To commutate the input stage, the output inverter stage is set into freewheeling mode, allowing the input stage to commutate under zero current. Consequently the input stage does not incur switching losses.

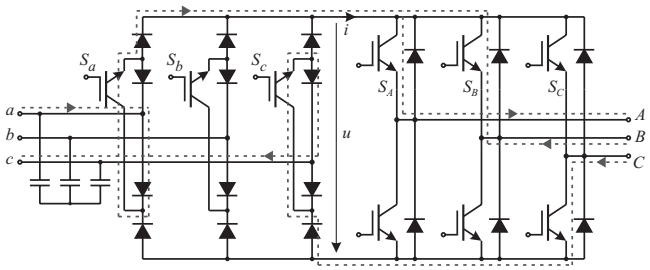
A. Modulation

A space vector modulation strategy which permits zero-current commutation is employed to provide sinusoidal input and output currents for the USMC [3]. The input phase with the highest absolute value is clamped for a sector that is $\pi/6$ wide while the other two phases are switched. Switching of the output stage is coordinated with the input stage to ensure the output stage is in freewheeling mode when input stage is switched.

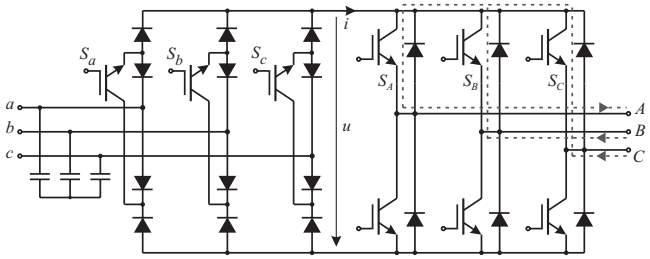
This modulation strategy is summarized in Fig 2. The operation of the converter is shown with the input stage and output stages both operating in sector 1, where input phase a has the most positive value for a $\pi/6$ interval and the output stage is formed by a combination of the (100) and (110) vectors of the output stage. However, it should be noted that under normal operation, the input and output sectors are not necessarily synchronized. It is assumed that the output current remains constant during the switching cycle due to the inductive nature of the load.



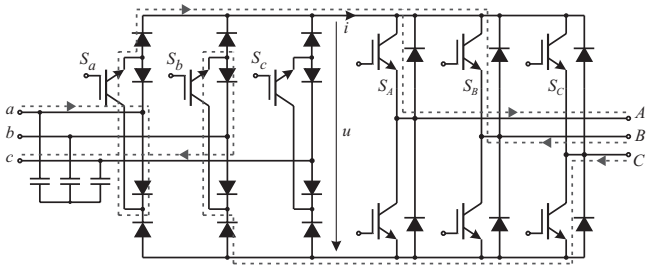
(a) State 1: $u = u_{ac}, i = i_A$



(b) State 2: $u = u_{ac}, i = -i_C$



(c) State 3, 4: u switched from u_{ac} to $u_{ab}, i = 0$



(d) State 5: $u = u_{ab}, i = -i_C$

Fig. 2. Figure summarizing the operation of the modulation strategy and zero-current commutation during an output switching cycle

In state 1 input phase a is at its peak positive value and is clamped to the positive dc link rail by input switch S_a. Switch S_c is also turned on to conduct the return current. During this interval output leg S_A has its high side switch active while the other output switches have their low side switches active.

In state 2, the input stage remains unchanged while the output leg S_B switches from low side to high side operation. In states 3 and 4, the zero current switching of the input stage occurs. Firstly output leg S_C is switch to high-side operation to create a freewheeling state at the output. The input stage then commutates from S_c to S_b under zero current.

The converter then switches into state 5, which is similar to

state 2 except the dc link voltage is now u_{ab} and input switch S_b conducts the return current. In the final state, which is not shown, output leg B switches from high to low side operation such that the output stage is the same as shown in state 1.

The time intervals for the different switching states of both input and output stages, τ_n, are calculated based on space vector modulation to ensure sinusoidal input and output currents [3].

B. Reverse Current Flow

Reverse current flow occurs in the USMC when the output current is more than 30° out of phase with the output voltage. The conditions under which reverse current flow occurs are described mathematically in [3] and are depicted in Fig. 3 for a particular operating point.

The desired output voltage vector, u_2^*, is formed by a combination of the A and -C vectors, which correspond to bridge leg combinations of (100) and (110) respectively. The dc link current is thus a combination of i_A and $-i_C$ as shown in Fig. 2. For the depicted operating conditions, reverse current flows during the time intervals that vector A is switched since the projection of i_2 onto the A axis is negative. However, reverse current flow into the mains is prevented by the outer diodes in each input stage leg. In order to avoid reverse current flow for all operating points, the output current phase angle must therefore meet the condition $-30° < \Phi_2 < 30°$. However, it should be mentioned operating conditions exist where Φ_2 can exceed $\pm 30°$ without causing reverse current. For example, while u_2^* is aligned directly with vector (100), Φ_2 can be up to $\pm 90°$.

Due to this operating restriction, the USMC is not well-suited for supplying induction motor loads since the output current typically exceeds the $\pm 30°$ limit in the steady state. However, the USMC can be used for PM motors, where load current typically stays within this limit under normal operation.

III. Hardware Implementation

A schematic diagram of the USMC is shown in Fig. 4 and the hardware implementation of the final system is depicted in Fig 5. The schematic shows the main system components and in particular the connection of the clamp circuit.

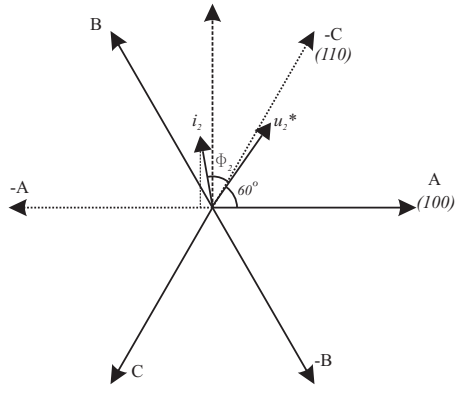


Fig. 3. Example of conditions that cause reverse current flow

The USMC power circuit is designed with a low inductance layout to help minimize switching losses in the output stage. A custom made bank of high-performance ceramic capacitors is situated in the center of the power PCB to supply the ripple currents drawn by the input stage. All power switching components are then placed directly around this bank to minimize the series parasitic inductance.

The EMC filter is designed to mitigate conducted electromagnetic emissions such that the converter meets the CISPR 11 specifications for Class A equipment. Optimized for size, the filter consists of two common mode and differential stages. The common mode stage provides an attenuation of -36 dB at 150 kHz and the differential stage an attenuation of -94 dB.

The power switches are based on IXYS IGBT modules. Each output phase leg is a FII50-12E module and each input switch and inner diode combination is an FII50-12BD module. Both input and output modules have an average current rating of 32 A at 90°C.

The power board accommodates an auxiliary supply rated at 25 W to supply the voltages needed by the measurement and control circuits. The supply, based on the flyback topology, provides the auxiliary voltages needed for the measurement and control circuitry. The flyback converter is integrated with the clamp to provide extra dissipation and ride through operation.

The control circuit is divided into a DSP board and measurement board as shown in Fig. 6. The DSP board contains an Analogue Devices ADSP-2199x DSP which implements the main motor control loop. The signal interface board provides level shifting and signal conditioning for the measurement and control signals travelling between the DSP and power board, allowing the DSP to measure bipolar values. In addition, it includes an FPGA to convert the vector times calculated by the

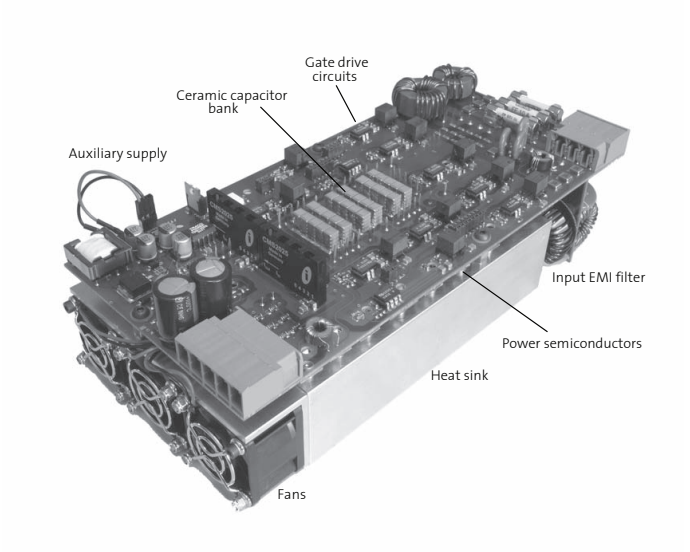


Fig. 5. Implementation of USMC. DSP and measurement boards are not shown. Dimensions are 76 x 120 x 260 mm and power density is 2.32 kW/dm^3 (38 W/in^3)

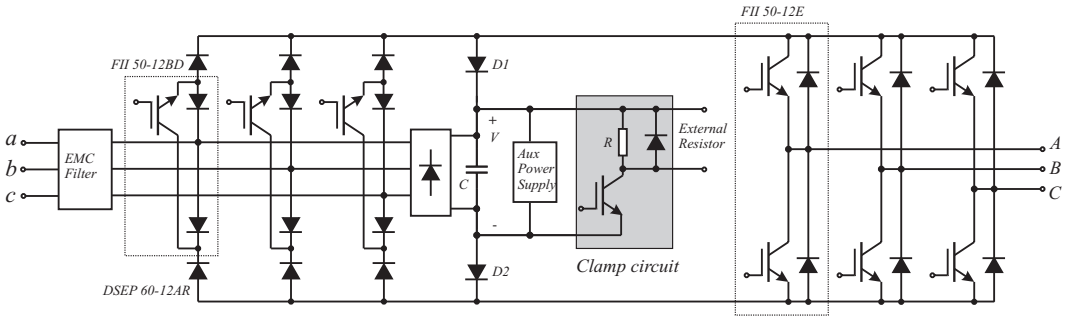


Fig. 4. Ultra Sparse matrix converter schematic

DSP into physical interlocked gate drive signals. Both control boards are stacked and plugged directly on top of the main power PCB.

The losses are calculated according to the equations derived in [6] and [7] for the worst-case conditions of Φ_2 = 0° and M = 1, where Φ_2 is the output current phase angle and M the modulation index. The semiconductor loss parameters for the IGBT bridge-leg modules (FII50-12E) are adopted from [8], whereas the on-state parameters of the additional rectifier stage diodes (IXYS DSEP 60-12AR) are extracted from characteristics provided by the datasheet.

Table II summarizes the worst case rectifier and inverter losses for an inverter switching frequency $f_{S,Inv}$ of 50 kHz, a modulation index M_{12} of 1 and a junction temperature T_j = 125°C. At the nominal operating point (U_1 = 230 V, P_2 = 5.5 kW) the worst case efficiency η_{WC} is 94.3% neglecting auxiliary power supply losses and assuming 27 W of EMC filter losses.

TABLE II
SEMICONDUCTOR LOSSES

$f_{S,Inv}$	**Rectifier stage**	**Inverter stage**		**Total semi-conductor losses**
	Conduction losses	Conduction losses	Switching losses	
50 kHz	92 W	39 W	157 W	288 W

The cooling system is designed to ensure the maximum junction temperature of the semiconductors does not exceed 130°C. The cooling system, comprising three high-performance SanAce 40/28 fans and a custom-designed heatsink, was designed in accordance with principles presented in [9]. The resultant thermal resistance of the heatsink is 0.07 K/W.

A simulation showing the thermal gradient of the heatsink was performed using ICEPAK to ascertain the maximum surface temperature and to place the output leg modules to prevent the occurrence of hotspots. For an ambient temperature of 45°C the simulation showed that the surface temperature under maximum power conditions did not exceed 89°C. The maximum junction temperature of the hottest devices, the output modules, was calculated to be 139°C.

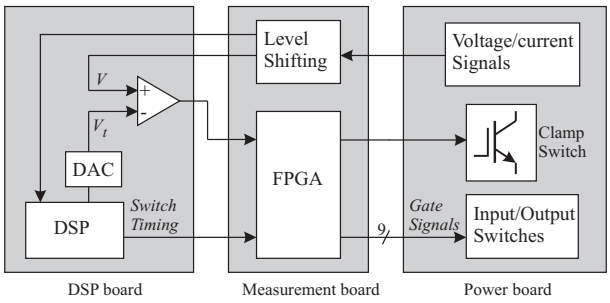


Fig. 6. Block diagram of USMC control circuit

IV. CLAMP CIRCUIT DESIGN

For dynamic regenerative loads such as motors, reverse current flow is unavoidable and a clamp circuit is needed to protect the converter from experiencing overvoltages on the dc link. Clamp circuits have been proposed for bidirectional matrix converters to prevent the switching devices from incurring overvoltages and to permit ride-through under overvoltage conditions.

The clamp circuit typically used for conventional matrix converters connects the input and output lines via two B6 diode bridges to a common capacitor which absorbs the voltage spikes [4]. This topology has been adapted to permit ride-through for a conventional matrix converter during mains failure. The motor is operated in a regenerative manner, such that power flows back into the clamp capacitor, which is used to power the control circuits [10]. This topology has been further extended to permit braking during mains failure by connecting a resistive chopper across the clamp capacitor [11]. The conventional clamp circuit can easily be applied to the USMC by connecting a single B6 diode bridge to the output lines as shown in Fig.7(a). Although this clamp circuit could be adapted to permit reverse power flow using the technique outlined in [11], other simpler clamp topologies permit this adaptation also.

Another clamp circuit that has been proposed for the 9-switch ultra sparse matrix converter consists of a single capacitor and diode connected across the dc bus [5]. This clamp circuit, shown in Fig.7(b), can only be used for overvoltage protection as it has no capability for dissipating significant

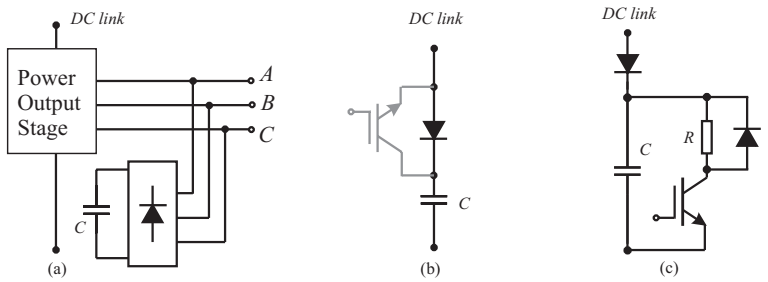


Fig. 7. Clamp topology options. (a) Conventional clamp circuit (b) Capacitor-diode clamp with optional switch (c) Active clamp circuit

voltage rises caused by reverse current flow. An improvement to this circuit which involves connecting an optional switch across the diode to allow the flow of stored energy back into the system has been proposed [12].

Although this diode-capacitor clamp topology is incapable of sustaining reverse current flow, the active clamp circuit, shown in Fig.7(c) can. This topology, chosen for the USMC, allows the connection of a power resistor across the capacitor to dissipate any reverse power. The actual implementation, shown in Fig. 4, is integrated with the auxiliary supply capacitor.

The advantage of connecting the clamp circuit across the auxiliary supply instead of directly across the dc link is twofold: the auxiliary supply bus voltage provides a more stable voltage measurement than the dc link voltage. If clamping were performed on the dc link it would fluctuate significantly since it contains no storage. In addition the steering diodes $D1$ and $D2$ can provide the converter with a controlled ride-through or shut-down capability during power outages. During mains failure, the motor can be decelerated to provide sufficient power to the auxiliary supply, keeping the controller active and thereby ensuring a controlled ride-through or shutdown of the system.

A number of techniques for activating the clamp circuit are possible. One technique is to operate the clamp in a PWM fashion when a reverse current is detected with the duty cycle dependent on the magnitude of the reverse current. Another technique is to operate the clamp based on the voltage level of the dc bus. This technique was chosen for its robustness and simpler implementation. The actual clamp activation circuit, shown in Fig. 6, is based on a comparator that compares the measured auxiliary bus voltage, V, to the clamp trip threshold, V_t. The ideal response of the clamp circuit is shown in Fig. 8.

The DSP sets the trip threshold using a trim DAC to a level such that under normal operation, the nominal auxiliary bus voltage, V_{nom}, is below this value. The nominal bus voltage is 560V, determined by the peak line to line voltage. When V exceeds V_t due to an overcurrent the FPGA immediately activates the clamp switch and leaves it on for the duration of the overvoltage condition. When the overvoltage disappears, the FPGA deactivates the switch after a small time delay of t_d to implement a form of hysteresis.

Using this clamp circuit, the operation of the clamp switch is dependent on the reverse current and size of the clamp resistor.

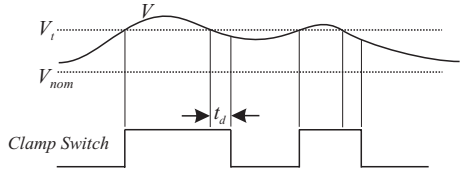


Fig. 8. Ideal time response of clamp circuit

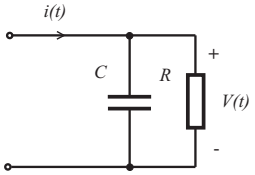


Fig. 9. Equivalent clamp circuit when clamp is active

If the clamp resistor is sufficiently large to dissipate the reverse current, the clamp will operate in a variable frequency pulse mode that is dependent on the instantaneous value of the dc bus. Otherwise it will remain on constantly for the duration of the reverse current flow.

The clamp resistor can be sized with the aid of an equivalent RC circuit, shown in Fig. 9. In the simplified circuit, the motor inductance and mechanical and resistive losses are neglected, as are the diode and effective auxiliary power supply resistance, since these factors have little bearing on the clamp resistor dimensions.

The clamp resistor is sized to prevent the dc bus from rising above the clamp trip voltage threshold. The reverse current and dc bus voltage can be approximated by (1) and (2) respectively,

$$i(t) = -\frac{J}{K_t}\frac{d\omega(t)}{dt} \tag{1}$$

$$V(t) = V_0 e^{\frac{-t}{RC}} + R(1 - e^{\frac{-t}{RC}})i(t) \tag{2}$$

where J is the motor inertia, K_t is the torque constant and $d\omega/dt$ is the angular acceleration. The parameters for the experimental system are $C = 11\mu F, J = 40 \times 10^{-4} kg.m^2$ and $K_t = 0.75\ Nm/A$.

The relationship between the dc bus voltage and the clamp resistance was determined under worst-case conditions using a MATLAB simulation of the equivalent circuit. It was assumed

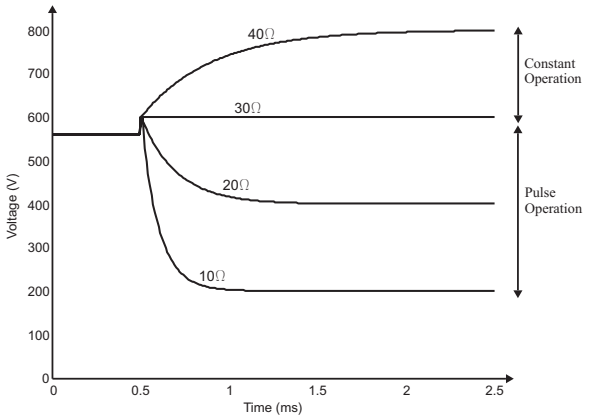


Fig. 10. Relationship between clamp resistance and dc bus voltage rise for a reverse current flow of -20 A occurring at t = 0.5 ms. Initial voltage is 560V and clamp trip threshold is 600V.

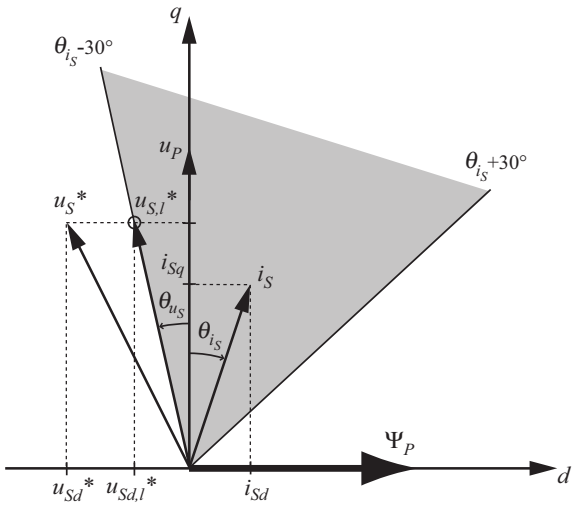


Fig. 11. Modified output stage reference voltage method to avoid a negative dc link current

that the motor was decelerated from 2000 rpm to 0 as fast as possible by setting the reverse current limit in the torque control loop to -20 A. Under these conditions, the time taken to decelerate the motor is 56 ms. The results, depicted in Fig. 10, show the change in bus voltage under reverse current conditions. Initially, the bus voltage is 560 V due to the three phase mains supply charging C. When the reverse current flows at t = 0.5 ms, the bus voltage rapidly increases to the clamp trip threshold of 600 V and the clamp activates. Fig. 10 shows that the clamp resistance should be no greater than 30Ω in order to prevent a rise above the clamp trip threshold. The required peak power rating for a 30Ω resistor is 12 kW. For clamp resistances below 30Ω, the clamp must be operated in a PWM mode to prevent the clamp from dissipating mains power when the bus voltage drops below 560 V. It should be also noted that for this step change in speed, the capacitance has no influence over the final value of the voltage because the settling time of the clamp circuit, $3 \cdot RC$, is significantly shorter than the time taken to implement the step change in speed.

Although the power rating of the clamp resistor for this worst case operating condition is onerous, opportunities exist for reducing the clamp resistor rating. It can be seen from (2) that the voltage rise is dependent on the magnitude of the reverse current, which in turn is dependent on the deceleration. One option is to limit the reverse current flow into the dc bus and another option is to limit $d\omega/dt$ by filtering the speed reference value. Using a first-order speed reference filter, the rate of change in speed and voltage under reverse current conditions are

$$\frac{d\omega}{dt} = -1/T_s(\omega(t) - \omega^*) \tag{3}$$

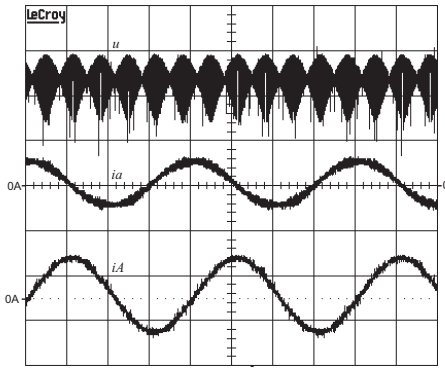
$$V(t) = V_0 e^{\frac{-t}{RC}} + \frac{RJ}{K_t T_s}(1 - e^{\frac{-t}{RC}})(\omega(t) - \omega^*) \tag{4}$$

where ω^* is the speed setpoint and T_s is the time constant of the filter. It can be seen that the rise in bus voltage is now dependent on the filter constant and size of the step change.

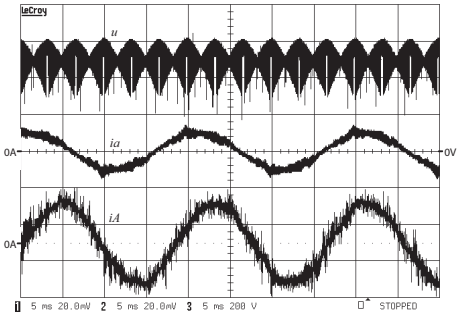
In the final implementation of the USMC a time constant of 20 ms was used, the current limit was selected to be -10 A. The clamp threshold was set to 610 V and the external clamp resistor was sized to be 60Ω with a 6 kW peak rating. A clamp resistor rated 200Ω, 2 kW peak was also mounted on board for dissipating reverse currents of up to -3 A.

Although a clamp resistor is necessary to provide a good dynamic response with regenerative loads, techniques for minimizing or even eliminating use of the clamp are possible. One simple technique which is well-suited for loads with low dynamic requirements such as fans is to reduce the rate of deceleration. This reduces the reverse current and in turn reduces the peak power rating for the clamp resistance.

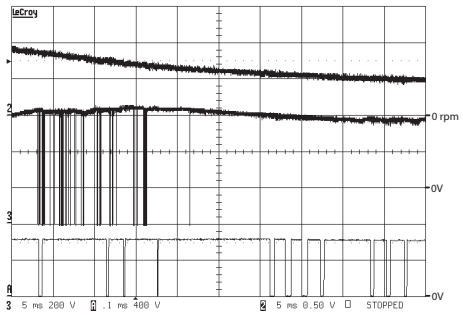
Another technique which is presently being investigated is to use a new modulation strategy to completely avoid negative current. Shown in Fig. 11, the proposed modulation strategy modifies the output voltage such that it remains within the $\pm 30°$ limit without affecting the torque-producing component of the stator voltage. It is assumed that there is an angle of θi_S between the motor stator current i_S and the motor back EMF u_P. To ensure the absence of negative dc link current, the stator voltage must remain within the shaded area. In this example, the motor controller generates a reference stator voltage $u_S{}^*$ that is outside the shaded area. The new strategy modifies the reference stator voltage so it is at the limit of the shaded area and that the torque-producing component of the stator voltage is unchanged. Therefore, $u_S{}^*$ is projected back on to the q-axis and a new reference stator voltage $u_{S,l}{}^*$ is now calculated such that it fulfils the $\pm 30°$ criteria for no reverse dc link current for all operating points of i_S. As a result of this restriction the d-axis reference voltage $u_{Sd,l}{}^*$ is reduced and only influences the magnetic flux in the motor. Although the example has shown this new method for a particular operating point, the new method is applicable to the complete operating region of the machine.



(a) DC link voltage u, input current ia and output current iA with a 2 kW RL load. (200 V, 10 A/division.)



(b) DC link voltage u, input current ia and output current iA with a 2 kW PM motor load. (200 V, 10 A/division.)



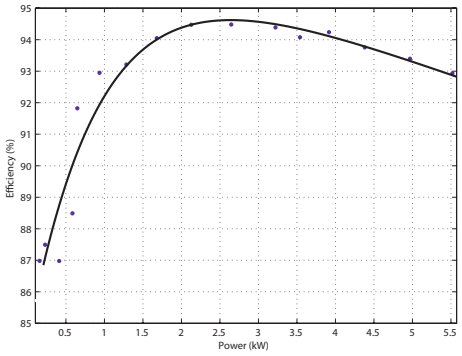
(c) Clamp circuit operation under regeneration conditions. Graph shows motor speed (500 rpm/div), clamp voltage (200V/div) and zoomed view of the clamp voltage at initial activation.

Fig. 12. Experimental results

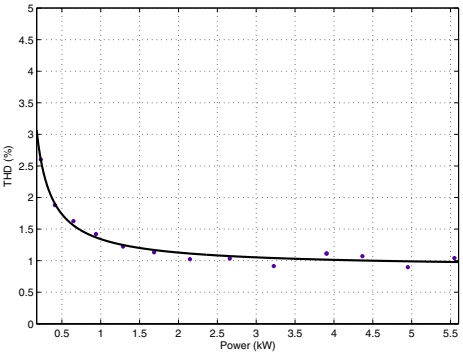
V. Experimental Results

The performance of the USMC was evaluated with an RL and PM motor load. The dc link voltage and input and output currents were measured with a LeCroy Waverunner LT548L oscilloscope and the results are shown in Fig. 12. It can be seen that the average value of the dc link voltage is approximately 560 V, and that its shape is typical of the space vector modulation scheme used for the sparse matrix converter [3]. Efficiency and performance measurements were made, and the results are given in Fig. 13.

The efficiency of the converter was measured with an RL load of 20Ω, 10 mH and the onboard auxiliary supply inactive.



(a) Efficiency vs. input power



(b) THD vs. input power

Fig. 13. Performance of USMC with an RL load

The modulation index was fixed at 0.8 to ensure consistency. The results are portrayed in Fig. 13(a). It can be seen that the converter reaches its peak efficiency of 94.5% with an input power of approximately 2.5 kW. The efficiency at full load is 93%, which is 1.3% lower than the calculated value. This difference can largely be attributed to the lower modulation index used for the efficiency measurements.

The THD of the input current was measured up to the 50th harmonic and the results are shown in Fig. 13(b). It can be seen that at low loads the THD is as high as 3.0%, but this can be attributed due to the capacitive reactance of the EMI filter slightly distorting the input current at low real power levels. At full load, the THD decreases to approximately 1.0%.

The performance of the USMC was also evaluated with a 2 kW PM motor load and the waveforms are shown in Fig. 12. It can be seen that the distortion in the input current has increased slightly due to the non-ideal nature of the load.

The operation of the clamp circuit was tested by forcing the converter to operate under reverse power flow conditions. A motor load running at 800 rpm was connected then the speed was reduced by 50% in order to achieve reverse current flow at the output. The results, portrayed in Fig. 12(c) depict the actual motor speed and the voltage across the clamp switch. When the auxiliary bus voltage reaches the clamp threshold of 610 V, the clamp switch becomes active, switching the 200Ω resistor

across the auxiliary dc bus in PWM mode since the reverse current flow for this small decrease in speed is insufficient to maintain the bus voltage at or above the clamp threshold. It can be seen that after the clamping operation, the bus voltage returns to its nominal value of approximately 560 V due to the auxiliary power supply draining the bus capacitor.

VI. Conclusion

The USMC is the most reduced form of the indirect matrix converter that is well-suited for applications demanding unidirectional power flow. The USMC has minimal semiconductor requirements, comprising only 9 unidirectional switches and 18 diodes. Like the other converters in the indirect matrix family, the USMC uses a simple zero dc-link current commutation scheme to reduce the switching losses of the rectifier stage. This paper has presented the design of a 50 kHz USMC, in particular focusing on the design aspects of the novel active clamp circuit that is integrated with the auxiliary supply capacitor. The experimental results have demonstrated that the USMC produces sinusoidal currents of a high quality at both the input and output. They have also demonstrated the ability of the clamp circuit to protect the converter from experiencing overvoltages under reverse power conditions.

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