Virtual-Flux Decoupling Hysteresis Control for the Five-Level ANPC Inverter Connected to the Grid

L. A. Serpa*, P. K. Steimer† and J. W. Kolar‡
*ABB Corporate Research
Power Electronics Applications, Dätwill, Switzerland
Email: leonardo-augusto.serpa@ch.abb.com
†ABB Switzerland Ltd.
Power Electronics and MV Drives, Turgi, Switzerland
‡Swiss Federal Institute of Technology - ETH
Power Electronics Systems Laboratory, Zürich, Switzerland

***Abstract*—Interest in multilevel power converters has been increased in the last decades due to numerous advantages.Therefore, new control concepts have to be developed or existing control techniques must be extended to take advantage of these benefits.However, although multilevel inverters present numerous advantages, some drawbacks are evident. They require a higher number of semiconductors and either multiple isolated dc sources or a bank of series connected capacitors. Consequently, the control complexity increases considerably, since more switching devices normally result in a higher number of possible combinations and the balance of the capacitors has to be guaranteed. In order to fulfill these requirements, this paper extends the Virtual-Flux Decoupling Hysteresis Control (VF-DHC) scheme previously presented for the classical two-level and the industry standard three-level NPC inverters to operate with the recently introduced five-level Active Neutral-Point Clamped Inverter (ANPC).**

I. Introduction

For low power systems, the classical two-level inverter is typically employed as the interface between dc-supply and load. However, modern applications, which range from hundreds of kilowatts up to a few megawatts, demand special converter structures. One alternative is to connect switching devices in series to cope with the high voltage stress. However, this technique requires a precise method to ensure the voltage share between the devices in dynamic and static situations. Another method that has been well accepted by the industry, and is emerging as the standard solution for high power medium voltage applications, is the Multilevel Converter. These structures have the ability to synthesize the output waveform from several levels of voltages, improving the spectrum quality when compared with the classical two-level topology. Furthermore, it permits the use of power devices with lower voltage rates and reduces electromagnetic compatibility concerns, due to a smaller dv/dt. The basis of this new branch of topologies is the Neutral-Point Clamped (NPC) three-level inverter proposed in 1980's [1]. It utilizes a series connection of dc-sources (generally realized by capacitors) and clamping diodes to generated three output voltage levels. Using the same principle, but with different clamping elements, the three-level Flying Capacitor (FC) [2] topology makes use of capacitors to limit the voltage across the non-conducting switches. An extension of these topologies to higher number of voltages levels may be achieved including extra clamping elements. However, both topologies reveal technical difficulties which complicate their application by the industry. Recently, a new converter topology has been introduced [3] to overcome some of the above mentioned limitations. The five-level active neutral-point clamped (ANPC) converter combines characteristics of the NPC and FC inverters.

However, as new multilevel topologies are proposed, either new control techniques must be developed or existing control methods have to be adapted. Among the existing methods the Virtual-Flux Decoupling Hysteresis Control (VF-DHC) has shown a good performance for the two [4] and the three-level [5] topologies. It combines the simplicity and fast dynamic response of the classical hysteresis controller to a near constant switching frequency operation achieved by employing a decouple network and modulated hysteresis boundaries. The decouple network is applied to avoid the interference between phases that is inherent in isolated neutral three-phases systems.

The VF-DHC to operate with the five-level ANPC inverter proposed in this paper is a natural extensions of the two and three-level approaches. However, the hysteresis strategies used in both concepts must be modified in order to further extend the ability of the controller to select different voltage levels. In addition, the five-level ANPC inverter requires additional control of the mid-point potential and the voltage across the floating capacitors.

II. Five-Level Active Neutral-Point Clamped

The active neutral-point clamped (ANPC) inverter presented by one-phase leg in Fig. 1 produces five distinct output voltage levels by combining the three-level characteristic of the input stage (*Cell 1*) with the two-level of the output parts

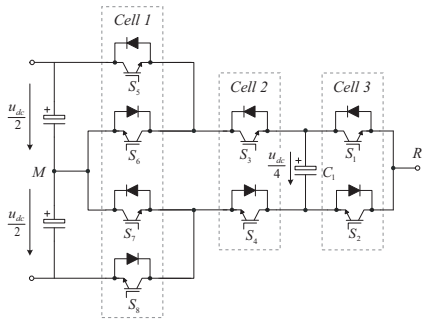


Fig. 1. One phase-leg of a five-level active-neutral point converter.

TABLE I
5-LEVEL ANPC INVERTER OUTPUT VOLTAGE LEVELS

Cell 1				*Cell 2*		*Cell 3*		Phase Voltage	Switching State
S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1		
1	0	1	0	1	0	1	0	$-\frac{u_{dc}}{2}$	u_1
1	0	1	0	1	0	0	1	$-\frac{u_{dc}}{4}$	u_2
1	0	1	0	0	1	1	0	$-\frac{u_{dc}}{4}$	u_3
1	0	1	0	0	1	0	1	0	u_4
0	1	0	1	1	0	1	0	0	u_5
0	1	0	1	1	0	0	1	$\frac{u_{dc}}{4}$	u_6
0	1	0	1	0	1	1	0	$\frac{u_{dc}}{4}$	u_7
0	1	0	1	0	1	0	1	$\frac{u_{dc}}{2}$	u_8

(*Cell 2* and *Cell 3*). Moreover, unlike classical five-level topologies, the ANPC inverter splits the dc-link into only two capacitors and requires only a single floating capacitor for each phase. Consequently, it reduces costs, volume and control complexity.

Five output voltage levels are achieved from eight distinct switching combinations, indicated by the combination of the switching functions of S_1, S_3 and S_5 in Table I. One can note that the switches S_5 and S_7 are operated in the same way and complementarily to S_6 and S_8.

The list of switching combinations also shows the presence of redundant states, which generate the same output voltage level referred to the dc-link mid-point M. The voltage level $-\frac{u_{dc}}{4}$ is generated either by the switching state u_2 or u_3. Nevertheless, they cause an opposite effect on the floating capacitor voltage, due to the different combination of the switches. For a positive output phase current for example, while state u_2 discharges, u_3 charges de floating capacitor.

A similar behavior is observed on the level $\frac{u_{dc}}{4}$ produced by the states u_6 and u_7. Depending on the direction of the output phase current, these states have the ability to charge or discharge the floating capacitor.

Besides that, the redundant combinations have also different impact on the mid-point potential, depending on the switching state of the input stage. For building an output voltage equal to $-\frac{u_{dc}}{4}$, the input stage can be connected either to the negative potential $-\frac{u_{dc}}{4}$ (u_2) or directly to M (u_3). For the voltage level equal to $\frac{u_{dc}}{4}$, the switching state u_6 results in mid-point current flow, while u_7 is connected to the positive potential.

Therefore, this analysis clearly shows a degree of freedom to balance the floating capacitor of each phase individually by properly selecting the switching states according to the direction of the output current and the state of the floating capacitor voltage. The influence of each phase on the mid-point potential can also be regulated using redundant states to create or avoid a link between the output and M.

III. VF-DHC FOR TWO-LEVEL INVERTER

The decoupling hysteresis controller (DHC) [6], as shown by shaded DHC area in Fig. 2, has the same basic outer structure as the standard current hysteresis controller where the phase current is subtracted from a current reference and the hysteresis controller generates a switching signal from the current error.

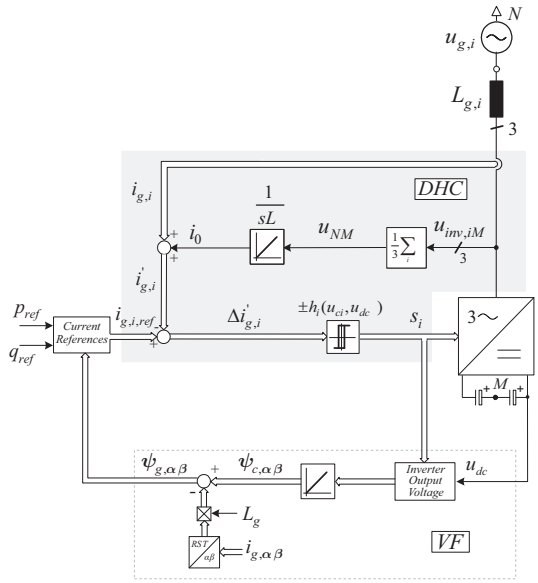


Fig. 2. Virtual-Flux Decoupling Hysteresis Control (VF-DHC) scheme.

The DHC has an additional control loop that generates the current control signal, i_0. By summing the measured line current, $i_{g,i}$ with i_0, a virtual current $i'_{g,i}$ is formed. With the correct formation of i_0 the switching of the hysteresis controller can occur without any interaction between each of the phase controllers. The phase interaction is caused because the dc bus mid-point to neutral voltage is not constant, as it depends on each of the inverter output voltages.

Reducing the phase current interaction results in the switching frequency becoming more uniform and allows for a near constant switching frequency if a variable hysteresis band is implemented.

IV. VF-DHC FOR FIVE-LEVEL ANPC INVERTER

The Virtual-Flux Decoupling Hysteresis Control operation with the five-level ANPC inverter is a natural extension of the two-level VF-DHC. The dashed area in the center of Fig. 3

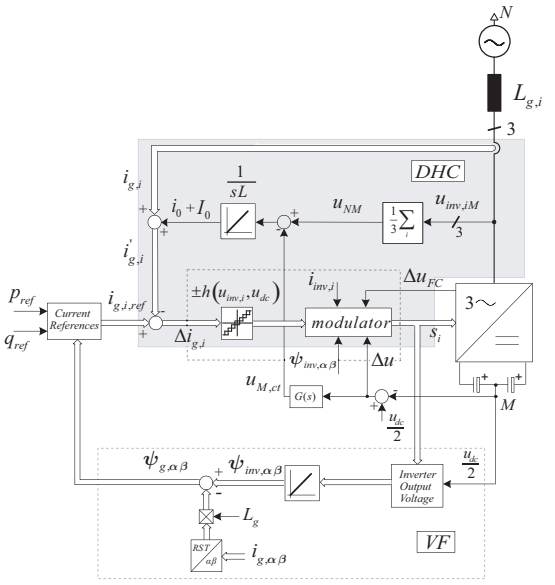


Fig. 3. VF Decoupling Hysteresis Control for 5-level ANPC inverters.

marks the blocks which require special attention.

In order to permit the inverter to switch among five voltage levels, the hysteresis strategy is adapted including two extra hysteresis boundaries. Moreover, the expression which determines the shape of the modulated hysteresis has to be adjusted.

Due to a three-level characteristic of the input cell of the five-level ANPC topology, the method presented for the three-level NPC inverter, which balances the mid-point potential M by injecting an offset I_0 into the phase currents can also be employed. However, since the ANPC inverter demands additional control of the floating capacitors, an extra control block called modulator is included. It balances individually the floating capacitors according to the output currents direction.

A. Hysteresis Strategy

Since the shape of the modulated hysteresis band necessary to achieve near constant switching frequency is highly influenced by the number of voltage levels, the method applied for the calculation of the two and three-level system hysteresis boundaries must be reviewed. The five-level inverter requests a slightly different approach, since during the positive cycle the inverter output voltage can switch either between $\frac{u_{dc}}{4}$ and 0 or $\frac{u_{dc}}{2}$ and $\frac{u_{dc}}{4}$ according to the operating point. Hence, the analysis shall be performed separately.

Within the first interval, the inverter switches to $\frac{u_{dc}}{4}$ allowing the current to increase from the lower hysteresis limit to the upper limit. When the current reaches the upper hysteresis limit, the controller changes the switching state of the switching devices appropriately to generate an output voltage equal to 0. As consequence the load current decreases from the upper to the lower hysteresis limit. Combining both switching times, the hysteresis ensuring a nearly constant switching frequency in the interval where the fundamental inverter output voltage is lower then $\frac{u_{dc}}{4}$ can be expressed as

$$h_{i,1} = \frac{u_{inv,i}\left(\frac{u_{dc}}{4} - u_{inv,i}\right)}{2 \cdot L_g \cdot f_s \cdot \frac{u_{dc}}{4}}. \tag{1}$$

From the point where the inverter loses the capability to regulate the output current by switching only between the two lower voltage levels ($u_{inv,i} > \frac{u_{dc}}{4}$), the controller changes immediately to the next higher level, selecting appropriately either $\frac{u_{dc}}{2}$ or $\frac{u_{dc}}{4}$.

During this second period, to increase the current from the lower to the upper hysteresis limit, the inverter generates an output voltage equal to $\frac{u_{dc}}{2}$. In order to bring the current back to the lower boundary, and to limit Δu at the same time, the controller switches to the next lower level $\frac{u_{dc}}{4}$.

The combination of the on- and off-times provides the switching period and consequently the modulated hysteresis expression

$$h_{i,2} = \frac{\left(\frac{u_{dc}}{2} - u_{inv,i}\right)\left(u_{inv,i} - \frac{u_{dc}}{4}\right)}{2 \cdot L_g \cdot f_s \cdot \frac{u_{dc}}{4}}. \tag{2}$$

Therefore, this analysis shows that depending on the amplitude of the fundamental inverter voltage, the hysteresis shape necessary to achieve a constant switching frequency

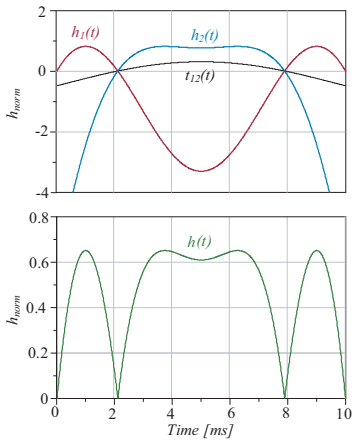


Fig. 4. Modulated hysteresis.

may change. The threshold for changing to another hysteresis shape is the intermediary voltage level $\frac{u_{dc}}{4}$.

The difference between the inverter fundamental voltage and the threshold limit (3) indicates the beginning and end of the application of the different shapes

$$t_{12}(t) = u_{inv,i}(t) - \frac{u_{dc}}{4} \tag{3}$$

Fig. 4 illustrates the time behavior of both hysteresis limits h_1 and h_2, considering a sinusoidal fundamental inverter voltage. The transition between the two boundaries to build the complete hysteresis h is controlled by the function t_{12}. During the interval where the inverter fundamental voltage is lower then $\frac{u_{dc}}{4}$ ($t_{12} < 0$), the controller utilizes h_1, while h_2 is selected for $t_{12} > 0$.

Although the modulated hysteresis allows for a near constant switching frequency, a dedicated multilevel hysteresis strategy has to be employed to switch between multiples output voltage levels as shown in Fig. 5. The current error is maintained inside of the inner bands, allowing the inverter to switch only between two consecutive levels. If the state selected is not able to correct the current error, the controller switches to the next upper (or lower) level when the error crosses the second hysteresis boundary. This finally forces the current error to operate within the inner bands. Even though a double hysteresis band is sufficient to achieve good

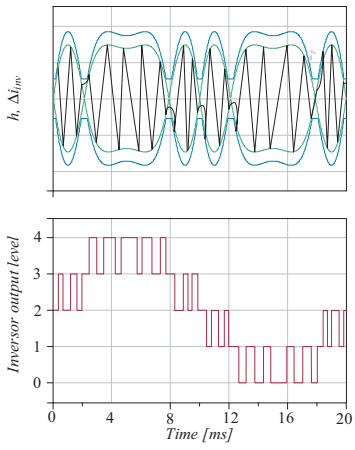


Fig. 5. Hysteresis strategy.

steady-state performance, a four level hysteresis is applied to force the current error back into the inner bands as fast as possible during transients by using extreme dc voltage levels.

B. Mid-Point and Floating Capacitor Balance

The majority of the mid-point voltage balancing schemes rely on some form of manipulation of redundant vectors available in multilevel topologies. In general the regulation is achieved by adjusting the relative on-time of the redundant switching state acting in the direction of a reduction of an existing mid-point unbalance [7].

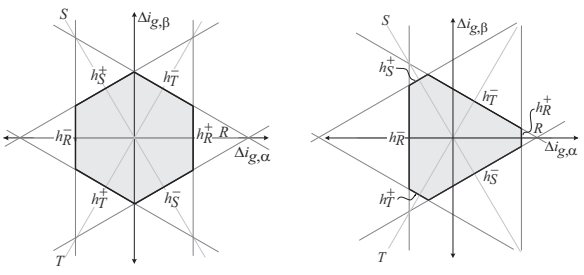
Since in the hysteresis method the control signals are generated directly from the difference between reference and actual value of each phase current according to the hysteresis boundaries, the possibility of controlling the mid-point voltage by influencing the frequency of each redundant state is limited basically to a modification of the reference value shape. Therefore, since the amplitude and sinusoidal shape of the currents references are given by the power requirements, the only remaining degree of freedom is the addition of a zero-component I_0

$$i'_{g,i} = i_{g,i} + I_0 \tag{4}$$

where the offset I_0 is set to be equal in all three phases and consequently, its influence on the current shape is canceled in systems with isolated mains neutral point where the sum of the phase currents is forced to 0 ($i_{g,R} + i_{g,S} + i_{g,T} = 0$).

One can note that I_0 has a direct influence on the location and shape of the tolerance area (Fig. 6), which is defined by the intersection of the tolerance bands of each phase. For a classical operation without offset or $I_0 = 0$, the tolerance area is represented by an equilateral hexagon (Fig. 6(a)), resulting in segments of positive (h_i^+) and negative (h_i^-) switching thresholds with equal length. As consequence, the resulting average mid-point current is zero. However, when a positive offset I_0 is added to the phase currents, the tolerance bands of each phase are shifted to the positive side according to Fig. 6(b). The intersection of the bands now creates an asymmetric tolerance area, where the the positive (h_R^+, h_S^+, h_T^+) and the negative (h_R^-, h_S^-, h_T^-) switching thresholds are of unequal lengths, resulting in a positive average mid-point current.

In the proposed VF-DHC, the zero sequence current I_0 is created by subtracting the signal of the voltage controller $u_{M,ct}$ from the input of the integrator (Fig. 3). The voltage controller compares the voltage across the lower capacitor



(a) $I_0 = 0$ (b) $I_0 > 0$

Fig. 6. Tolerance area of a three-phase hysteresis controller (a) without dc offset and (b) with positive dc offset.

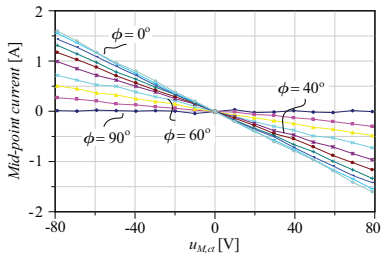


Fig. 7. Transfer characteristic from the controlling signal $u_{M,ct}$ to the average i_M for different values of mains voltage and current phase-shift.

against a reference (5), which is normally half of the total dc-link voltage, and produces a proportional dc control $u_{M,ct}$

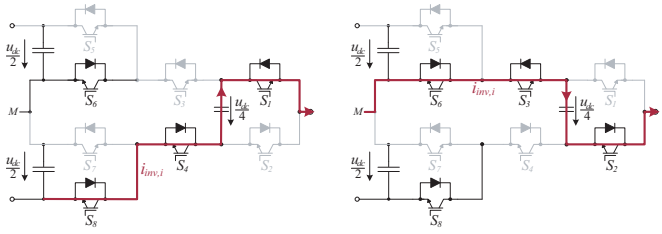
$$\Delta u = u_{C_{l,ref}} - u_{C_l} \tag{5}$$

$$u_{M,ct} = k_p \cdot \Delta u. \tag{6}$$

The influence of the controller output voltage $u_{M,ct}$ on the average mid-point current is shown in Fig. 7. This clearly shows that if for $\phi = 0^o$, e.g. the lower capacitor voltage u_{C_l} is below the reference voltage $u_{C_{l,ref}}$, the resulting positive controller output voltage $u_{M,ct}$, produces a negative average mid-point current, which charges the lower capacitor, balancing the mid-point potential. However, for different values of mains voltage and current phase-shift (ϕ) the controllability of the mid-point current and consequently of the mid-point potential is reduced when ϕ is approaching 90^o.

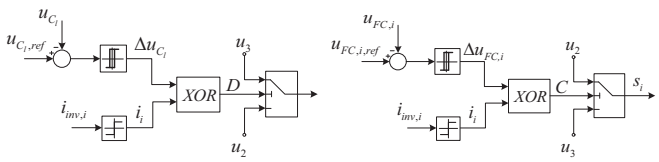
Nevertheless, for the five-level ANPC inverter due to existing redundant switching states to generate the levels $-\frac{u_{dc}}{4}$ and $\frac{u_{dc}}{4}$, there exists an extra degree of freedom to balance the mid-point potential.When the controller of phase i decides to apply an output voltage level of $-\frac{u_{dc}}{4}$, the inverter has two switching state alternatives, u_2 and u_3, which affect differently the mid-point potential. While state u_3 connects the inverter output directly to M to generate the voltage level $-\frac{u_{dc}}{4}$ (Fig. 8), state u_2 establishes a connection to the negative potential. As consequence, only u_3 influences the potential of M dependent on the output phase current. The same situation occurs for the voltage level $\frac{u_{dc}}{4}$. While u_6 makes use of M, u_7 is connected to the positive potential. To use the benefits of this extra degree of freedom, the modulator shall select the switching state which either corrects the mid-point deviation or does not influence M.

A strategy to select the proper switching state to balance the mid-point potential according to the voltage deviation



(a) State u_2 (b) State u_3

Fig. 8. Effect of the redundant switching states u_2 and u_3 on the mid-point potential and floating capacitors.



(a) Mid-Point (b) Floating Capacitors

Fig. 9. Balancing strategy to control the mid-point potential (a) and floating capacitors (b) for the voltage level $-\frac{u_{dc}}{4}$

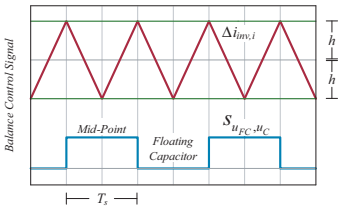


Fig. 10. Switching between floating capacitors and mid-point control.

of the lower dc-link capacitor Δu_{C_l} and the direction of current i_i, is applied as illustrated in Fig. 9(a). Considering that the lower dc-link capacitor must be charged, $\Delta u_{C_l} = 1$, and the inverter is generating a positive phase current, if state u_3 is applied, the resulting positive i_M would continue to discharge the lower capacitor. Therefore, a reasonable alternative is to select state u_2 that although not correcting the deviation, at least does not contribute negatively as state u_3. This logic is repeated for all different combinations of $\Delta u_{C_l,i}$ and i_i, and is extended to the voltage level $\frac{u_{dc}}{4}$ with the switching states u_6 and u_7.

Besides being useful to balance the mid-point potential, the redundant states can also be used to balance the floating capacitors. For a positive output phase current $i_{inv,i}$, state u_2 discharges the floating capacitor (Fig. 8(a)), while state u_3 charges (Fig. 8(b)). For a negative current, the effect on the floating capacitor is reversed. Therefore, the modulator block is in charge to select the proper state to balance the floating capacitor according to the output current direction i_i (1 for positive and 0 for negative current), as illustrated in Fig. 9(b). Additionally, a hysteresis controller provides to the decision block, an input 1 when the capacitor voltage deviation $\Delta u_{FC,i}$ reaches the upper hysteresis limit and 0 for reaching the negative. If the voltage of the floating capacitor $u_{FC,i}$ is below the reference $u_{FC,i,ref}$ minus the limit allowed by the hysteresis controller, i.e. $\Delta u_{FC,i} = 1$, assuming a positive output phase current, i.e. $i_i = 1$, the state u_3 shall be selected to charge the capacitor. On the other hand, for the same voltage condition but negative output phase current, $i_i = 0$, u_2 is the correct choice to balance the floating capacitor.

The same strategy is applied when the current controller selects the voltage level $\frac{u_{dc}}{4}$. To generate this level the modulator has two choices, states u_6 and u_7. While the first state discharges the floating capacitor, considering a positive phase current, the second state increases the capacitor voltage. A similar decision block and logic strategy as shown in Fig. 9 are used to choose among these states, where state u_6 replaces u_2, while u_7 takes the position of u_3.

However, during normal operation the switching state selected to control the floating capacitor might not be necessarily the proper choice to balance the dc-link voltage. Therefore, a method to switch between these two controllers is required.

In the proposed approach, each control is selected every switching period successively, as illustrated in Fig. 10. Due to a nearly constant switching frequency obtained with the five-level VF-DHC, both strategies are applied practically over same interval of a fundamental cycle.

V. Experimental Verification

The experimental verification is performed using the $6kW$ five-level ANPC prototype presented in Fig. 11. A $10mH$ output filter connects a controlled 400V 3-phase AC power source to the inverter, which is operating with a switching frequency of $2.5kHz$. The $800V$ dc power is provided by two $10kW$ - $600V$ dc power supplies connected in series. The controller is implemented fully digitally using an Analog Devices ADSP21991 16-bit $160MHz$ DSP platform.

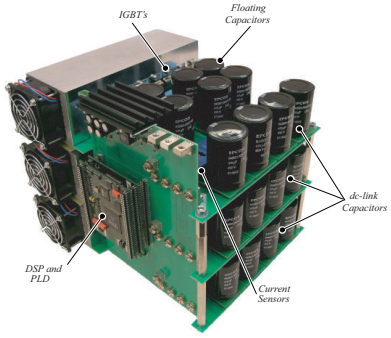
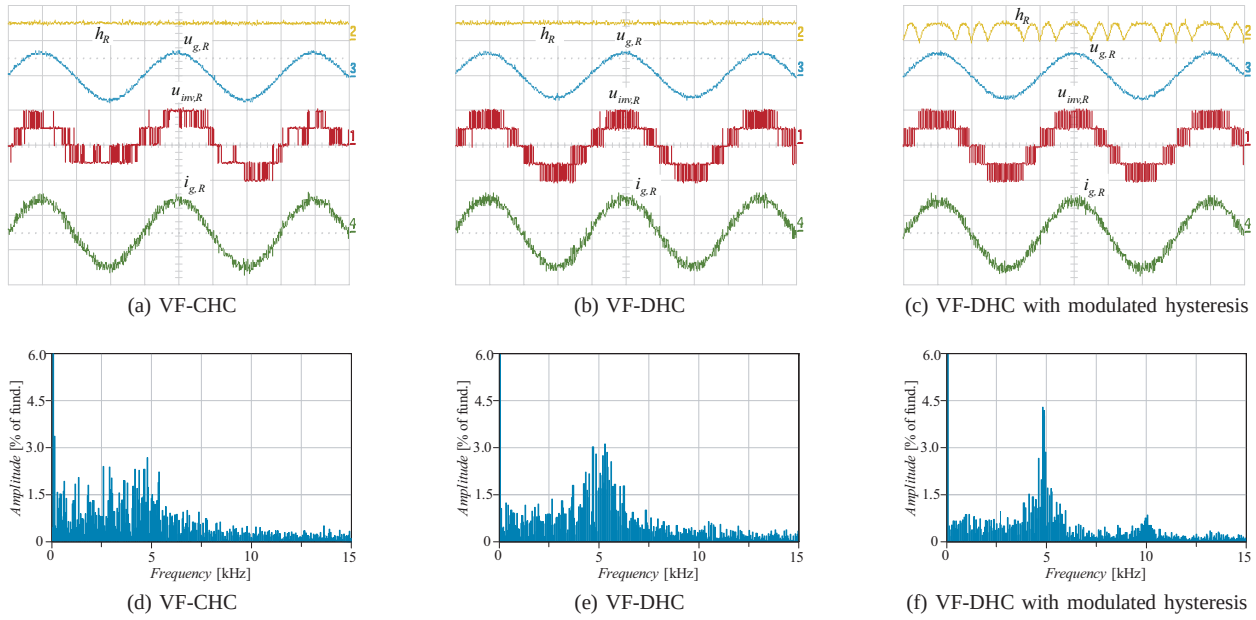


Fig. 11. Photo of the three-phase five-level ANPC prototype.

Initially, the experimentation is focused on the effectiveness of the decoupling method when applied to a five-level ANPC inverter. Fig. 12 shows the static performance concerning output phase current $i_{g,R}$ and voltage $u_{inv,R}$ for the classical hysteresis approach (Fig. 12(a)), the decoupling method (Fig. 12(b)) and the behavior of properly modulating the hysteresis boundaries h_R (Fig. 12(c)). One can note that the inverter output voltage generated by the classical hysteresis controller is very irregular with long intervals without any action. The performance is more consistent when the calculated zero sequence current i_0 is added to the measured phase currents, enabling the decoupling strategy. In this case, the inverter output voltage turns out to be more regular, although there are still some gaps during transitions between levels. Further improvement is achieved by varying the hysteresis limits h_i, where the hysteresis band shows a low width exactly in the moment when the hysteresis controller demands a transition to the next higher (or lower) level. This directly influences in the switching frequency which becomes more constant as shown by the current spectrum analysis of Fig. 12(d)-(f). The inherent wide spread frequency spectrum generated by the classical hysteresis approach is presented in Fig. 12(d). It becomes more centered around the desired switching frequency with the decoupling method (Fig. 12(e)) and nearly constant when the modulated hysteresis is enabled (Fig. 12(f)).



(a) VF-CHC (b) VF-DHC (c) VF-DHC with modulated hysteresis

(d) VF-CHC (e) VF-DHC (f) VF-DHC with modulated hysteresis

Fig. 12. Hysteresis band h_R, grid voltage $u_{g,R}$ (500V/div), inverter output voltage $u_{inv,R}$ (400V/div) and grid current $i_{g,R}$ (10A/div) of five-level (a) VF-CHC, (b) VF-DHC, and (c) VF-DHC with modulated hysteresis band and respective current spectrum (d),(e) and (f).

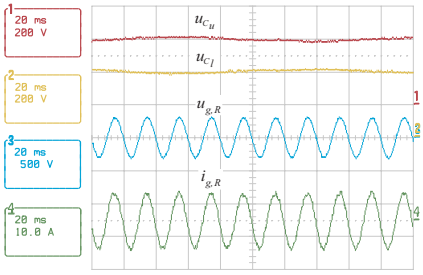


Fig. 13. Experimental results of the voltages $u_{C,u}$ and $u_{C,l}$ across the dc-link capacitors.

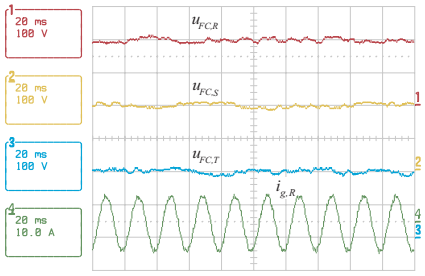


Fig. 14. Experimental results of the voltage across the floating capacitors.

Fig. 13 proves the effectiveness of the strategy applied to balance the mid-point potential. The voltage of the lower dc-link capacitor, and consequently of the upper capacitor, are controlled to $\frac{u_{dc}}{2}$ or $400V$, due to the correct operation of the modulator selecting a proper redundant switching state. Additionally, an offset I_0 calculated according to the voltage deviation is added to the measured currents to influence the resulting mid-point current.

Thanks to redundant switching states, the controller is able to regulate the voltage of the floating capacitors to $\frac{u_{dc}}{4}$ (Fig. 14). The modulator has the possibility of choosing among two redundant states when the current controller decides to apply a voltage level $-\frac{u_{dc}}{4}$ and another two states for the level $\frac{u_{dc}}{4}$.

VI. Conclusion

The decoupling current control (VF-DHC) to use for the five-level ANPC inverter is an extension of the method used for the two-level full-bridge topology. A dedicated modulated hysteresis strategy is used to allow the inverter to select multiple output voltage levels. Furthermore, in order to balance the mid-point potential and the floating capacitor voltages, a modulator is introduced to decode the level selected by the current controller into a correct switching state. The static and dynamic performance of both methods have been verified using a $6kW$ five-level ANPC inverter prototype connected to a $400V$ 3-phase AC power source via a first order L filter.

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