A Modified Direct Power Control Strategy Allowing the Connection of Three-Phase Inverters to the Grid Through LCL Filters

Leonardo Augusto Serpa, *Student Member, IEEE*, Srinivas Ponnaluri,
Peter Mantovanelli Barbosa, *Senior Member, IEEE*, and Johann Walter Kolar, *Senior Member, IEEE*

***Abstract*—This paper proposes a novel approach to adapt a conventional direct power control (DPC) for high-power applications, where a third-order LCL filter is frequently required. The LCL filter can cause a strong resonance and requires additional effort for system control. The application of a DPC for the control of a three-phase voltage source inverter that is connected to the grid through an filter has not yet been considered. The addition of an active damping strategy, together with a harmonic rejection control loop, to the conventional DPC is proposed and analyzed in this paper. The steady-state, as well as the dynamic performance of the proposed system, is verified with simulation results and experimental measurements.**

***Index Terms*—Active damping, direct power control (DPC), grid-connected inverter, LCL filter.**

I. Introduction

THREE-PHASE voltage-source inverters (VSIs) are employed in many grid-connected applications such as static var compensators, uninterruptible power systems, and distributed generating systems (e.g., photovoltaic, wind power, etc.). In order to control the VSIs and achieve a proper power flow regulation in a power system, voltage-oriented control [1], [2], which provides a good dynamic response by an internal current control loop, is widely used. As an alternative to this control method, other control strategies have been proposed in recent publications, such as predictive control [1]–[3] and direct power control (DPC) [4], [5].

DPC has become more widely used over the last few years due to the advantages of fast dynamic performance and simple control implementation when compared with other methods. The main disadvantage of DPC, compared to voltage-oriented control, is a variable switching frequency. The basic idea of DPC is the direct control of active and reactive powers without any internal control loop or pulsewidth-modulation (PWM) modulator. The switching states are selected via a switching table, and the states are chosen based on the instantaneous error between the estimation and the desired active and reactive powers. The DPC concept has previously been presented [4], [5]; however, only simple series inductors were used as a filter interface between the converter and the mains. These filters would easily be implemented if high switching frequencies are employed; however, in high-power applications, where a low switching frequency is required, the implementation of such a concept is restricted. An alternative filter implementation is with a third-order output filter, such as an LCL filter, which can achieve reduced levels of harmonics distortion at lower switching frequencies and with less total inductance. On the other hand, the LCL filter may cause the steady-state and transient distortion of the output current due to resonances. This distortion can be reduced but not solved in PWM converters if the main resonance frequency is selected in a frequency range where no harmonics of the output current exist. In the case of DPC, this approach cannot be considered since the switching harmonic spectrum is not clearly defined but spread due to the variable switching frequency.

Several methods [6], [7] have been proposed to damp the supply current oscillations, but usually, the output damping controller is overriding the modulation index, which is not possible with DPC since the switching states are selected by an optimum switching table, and not through a current control PWM loop. In this paper, a novel strategy for an active damping of an output LCL filter, which is based on active and reactive power modifications, is proposed, and its influence on the converter's behavior is presented.

An important aspect of the proposed damping strategy is that there is a compromise between the active damping factor and the level of the low-order harmonics components since the active damping method reduces the current harmonics within the LCL filter resonance range and, on the other hand, increases the low-order harmonics that are present in the capacitor current. The solution that is implemented in the proposed approach is to provide an individual harmonic rejection based on their respective individual synchronous reference frames.

II. DPC—Main Concept

The basic principle of DPC was proposed by Noguchi *et al.* [4], and it is based on the well-known direct torque control

Paper IPCSD 07-027, presented at the 2005 Industry Applications Society Annual Meeting, Hong Kong, October 2–6, and approved for publication in the IEEE Transactions on Industry Applications by the Industrial Power Conversion Committee of the IEEE Industry Applications Society. Manuscript submitted for review October 16, 2006 and released for publication April 25, 2007.

L. A. Serpa and J. W. Kolar are with Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, ETH Zentrum/ETL H16, 8092 Zurich, Switzerland (e-mail: serpa@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

S. Ponnaluri is with Technology and Development Power Electronics, ABB Switzerland Ltd., 5300 Turgi, Switzerland (e-mail: srinivas.ponnaluri@ch.abb.com).

P. M. Barbosa is with Power Electronics Applications, ABB Corporate Research, 5405 Baden, Switzerland (e-mail: peter.barbosa@ch.abb.com).

Digital Object Identifier 10.1109/TIA.2007.904438

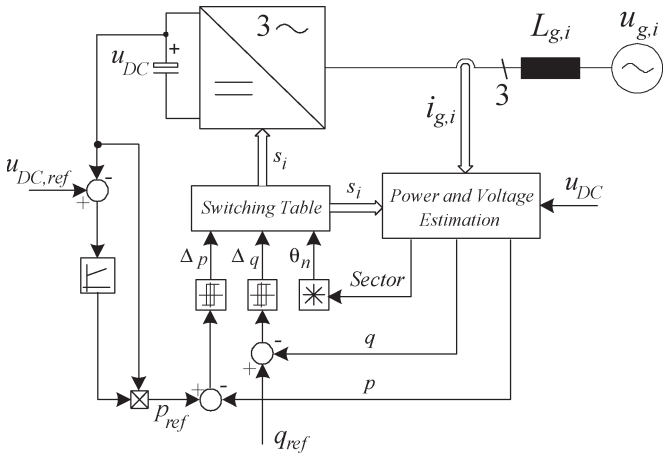

Fig. 1. Block scheme of a conventional DPC.

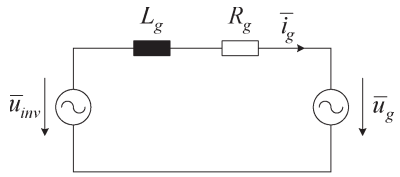

Fig. 2. Equivalent circuit of a grid-connected three-phase VSI with an L filter.

(DTC) for induction machines. In DPC, active and reactive powers replace the torque and flux amplitudes that are used as the controlled output in the DTC. The basic concept consists of selecting the appropriate switching states from a switching table based on the errors, which are limited by a hysteresis band, present in the active and reactive powers as illustrated in Fig. 1.

Two important aspects have to be maintained to guarantee the correct operation of the system: 1) correct selection of the switching states and 2) accurate and fast estimation of the active and reactive powers.

In order to correctly estimate the power and, at the same time, to reduce the number of implemented voltage sensors, Noguchi proposes the use of voltage vector estimation. The implementation of such approach involves the computation of the time derivative of the measured currents. The use of a derivative can increase the noise in the control loop, thus increasing the level of distortion.

Recently, the virtual-flux strategy was proposed [5], which basically assumes that the grid voltage and the ac-side inductors are quantities that are related to a virtual ac motor. By making an analogy with ac motors, R_g and L_g (Fig. 2) represent the stator resistance and the stator leakage inductance, respectively, and the grid voltage u_g represents the machine's electromotive force.

By applying the flux definitions of (1) and the voltage loop equation of (2), the grid virtual flux can be estimated.

$$\overline{\psi}_g = \int \overline{u}_g \cdot dt \tag{1}$$

$$\overline{u}_g = \overline{u}_{\text{inv}} - R_g \cdot \bar{i}_g - L_g \cdot \frac{d\bar{i}_g}{dt}. \tag{2}$$

By neglecting the series resistance of the grid inductor, the grid virtual flux can be calculated as

$$\overline{\psi}_g = \int \overline{u}_{\text{inv}} \cdot dt - L_g \cdot \bar{i}_g. \tag{3}$$

By using the estimated grid virtual flux and the measured currents, the active and reactive powers can be estimated [5] as

$$p = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{g,\beta} - \psi_{g,\beta} \cdot i_{g,\alpha}) \tag{4}$$

$$q = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{g,\alpha} + \psi_{g,\beta} \cdot i_{g,\beta}) \tag{5}$$

assuming the stationary ($\alpha\beta$) transformation of

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} u_R \\ u_S \\ u_T \end{bmatrix}. \tag{6}$$

III. Proposed DPC System

The proposed system adapts the conventional DPC strategy for use with a third-order LCL output filter and to achieve reduced levels of harmonic distortion for a VSI that operates with a low switching frequency. With this approach, the final size of the output filter is reduced through a lower total series inductance, fulfilling the requirement for high-power applications. In order to practically implement this and to try to overcome the resonance challenges that systems incorporating an LCL filter bring, the block diagram that is shown in Fig. 3 shows the concept for the proposed approach. The basic idea of the DPC in controlling the instantaneous active and reactive powers through the appropriate selection of the switching states based on the instantaneous errors between the reference and the estimated values is kept. Some modifications are necessary in order to achieve an individual harmonic control and an active damping while reducing the oscillations that are due to the LCL filter resonances. Unlike the conventional DPC which operates only in the stationary reference frame (SRF), the proposed method applies a synchronous reference frame transformation in some of the outer loops. Typically, this transformation is avoided since it requires angle information, which increases complexity. However, in the proposed method, the angle is available, which is provided by the phase-locked loop (PLL) that is used to guarantee the correct operation even under grid voltage distortion.

Since the switching states are selected via a switching table, there is no modulation index or common control signal within the control loops where the active damping control signal can directly be added. To overcome this limitation, the active damping control, as well as the individual harmonic rejection control, has to be implemented by directly acting on the active and reactive power components. These control signals have to be added to the fundamental references (p_{ref} and q_{ref}). Both control features will be explained in detail in the following sections.

Besides the two measurements that are typically used in the conventional DPC, namely, the dc-link voltage and the converter-side current, the proposed method demands

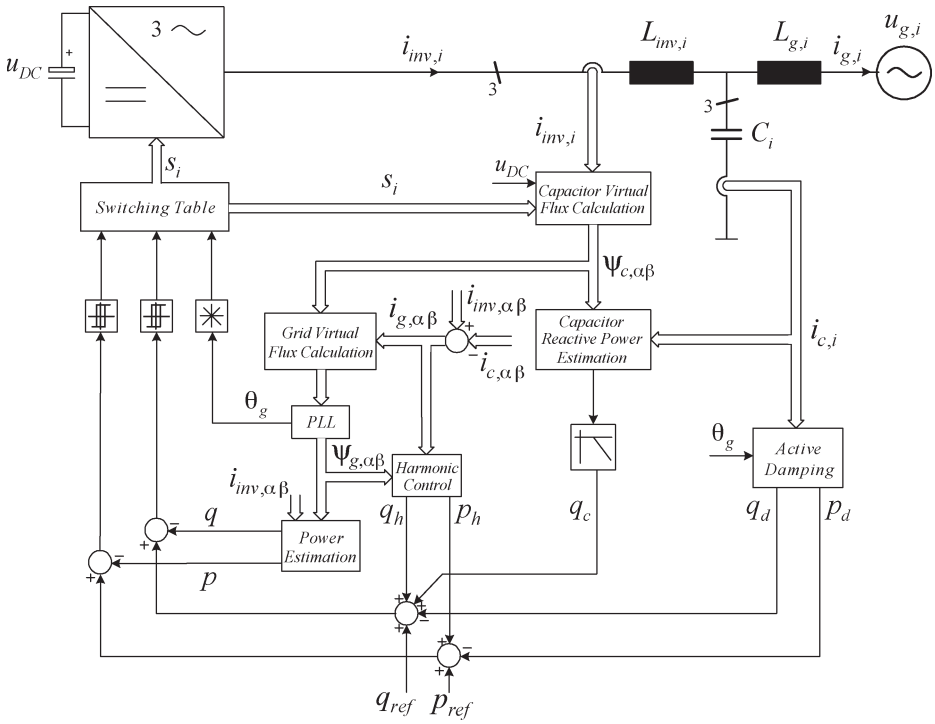

Fig. 3. Block diagram of the proposed DPC system with LCL filters.

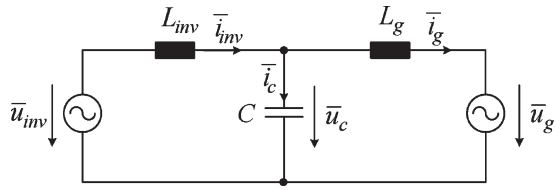

Fig. 4. Equivalent circuit of a grid-connected three-phase VSI with an LCL filter.

additional measurements to implement the extra control loops. The harmonic control loop utilizes the mains current to extract the harmonic information. The active damping controller would typically be required to measure the capacitor voltage; however, to avoid two extra sensors, only the capacitor current is measured since it allows both the capacitor voltage and the mains current to be calculated.

The mains current and, consequently, the mains power are expected to have a very low switching ripple by using a third-order output filter. This low ripple makes the control of the grid-side active and reactive powers very difficult when hysteresis approach is used, as the hysteresis boundaries have to be reduced to minimum. As a solution, the converter-side active and reactive powers must be controlled, and this explains the sensing of the converter-side currents.

A different method for mains virtual-flux estimation from the conventional concept with a series inductor filter is required. An equivalent simplified circuit of the LCL filter is shown in Fig. 4 and is used to derive the virtual-flux estimation method.

First, the capacitor virtual flux is estimated as

$$\overline{\psi}_c = \int \overline{u}_{\rm inv} \cdot dt - L_{\rm inv} \cdot \overline{i}_{\rm inv}. \tag{7}$$

The grid virtual flux can then be estimated based on the capacitor and the grid-side inductor virtual fluxes, which is the product of the grid-side inductance and its current. To avoid using another current sensor, the mains current can be estimated from the converter side and capacitor current measurements

$$\overline{\psi}_g = \overline{\psi}_c - L_g \cdot (\overline{i}_{\rm inv} - \overline{i}_c). \tag{8}$$

In a practical implementation, the integrator that is used to calculate the inverter output flux might saturate due to either the noise or dc offsets that are present in the sensed current or voltage. Therefore, a low-pass filter normally replaces the pure integrator; however, this reduces the system performance since phase and magnitude errors are inherent in the low-pass filter. In order to avoid these errors, phase and magnitude compensations, as presented in [8], are implemented in the flux estimation. The main idea of this method is to provide a low-pass filter behavior at all frequencies, except at the operating frequency (grid voltage frequency), thus avoiding the integration drift problem while at the same time maintaining a good system performance.

The relationship between the α and β components of the actual flux $(\psi_{{\rm inv},\alpha\beta})$ in terms of the α and β components of the estimated flux $(\psi'_{{\rm inv},\alpha\beta})$ is calculated based on the low-pass filter cutoff frequency (w_c) and the operating frequency (w_f)

$$\psi_{{\rm inv},\alpha} = \psi'_{{\rm inv},\alpha} + \psi'_{{\rm inv},\beta}\frac{w_c}{w_f} \tag{9}$$

$$\psi_{{\rm inv},\beta} = \psi'_{{\rm inv},\beta} - \psi'_{{\rm inv},\alpha}\frac{w_c}{w_f}. \tag{10}$$

The complete grid virtual-flux estimation method is shown in the block diagram in Fig. 5.

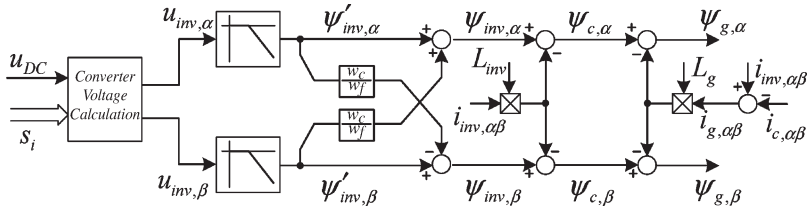

Fig. 5. Detailed grid virtual-flux calculation block diagram.

Another aspect to be considered during the practical implementation is the effect of the dead-time on grid virtual-flux estimation. For low-switching-frequency applications, the dead-time has no significant influence; however, for higher switching frequencies, an adaptive method that is used to compensate the dead time needs to be considered.

By using the same methods as in the conventional DPC, the converter-side active and reactive powers can be estimated by

$$p = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{\mathrm{inv},\beta} - \psi_{g,\beta} \cdot i_{\mathrm{inv},\alpha}) \tag{11}$$

$$q = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{\mathrm{inv},\alpha} + \psi_{g,\beta} \cdot i_{\mathrm{inv},\beta}). \tag{12}$$

Since both the active and reactive powers are controlled on the converter side, the capacitor reactive power must be properly compensated, and this is implemented by adding the estimated capacitor reactive power (13) to the fundamental reactive power reference (q_{ref})

$$q_c = \frac{3}{2}\omega \cdot (\psi_{c,\alpha} \cdot i_{c,\alpha} + \psi_{c,\beta} \cdot i_{c,\beta}). \tag{13}$$

A. Active Damping

One well-known method that is used to provide a reasonable damping of the current oscillations that are caused by the LCL filter resonance is to connect a physical resistor in parallel with the filter capacitor. A main disadvantage of this strategy is that the required damping resistance value that is needed for a satisfactory dynamic performance usually results in very high power losses. It is possible to avoid these additional losses by using an effective damping controller strategy that is realized by emulating this resistor. An active damping strategy can be applied because the resonance frequency of the output filter is usually within the bandwidth of the VSI control loops.

Several methods have been proposed [6], [7] to damp the supply current oscillations and are usually based on quantities such as voltages and/or currents. Most of these methods use the output of the damping controller to modify the modulation index; however, this is not possible with the DPC as the switching states are selected via an optimum switching table and not only by knowing the sectors and the current control loop. To overcome these limitations, a novel active damping strategy that makes use of the active and reactive power control loops is proposed.

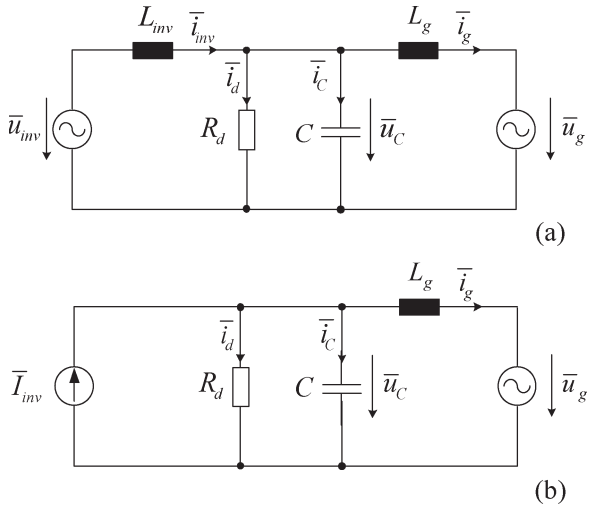

Fig. 6. Equivalent output stage (a) with passive damping and (b) with an LCL filter, considering the inverter plus inverter-side inductor as a current source.

As a first step of the damping analysis, a passive damping concept is reviewed and then is compared with the active damping strategy to determine its effectiveness. To focus on the damping effect that is caused by the resistance that is connected in parallel to the filter capacitor, the grid and converter-side inductor resistances are ignored in this analysis.

As the power is controlled in the inverter-side inductor (L_{inv}) and the controller is relatively fast, both the inverter and the inverter-side inductor can be considered as a current source (I_i), as shown in the simplified equivalent diagram [see Fig. 6(b)]. Therefore, the resonance to be damped occurs only between the grid-side inductor (L_g) and the capacitor (C).

The transfer function between the grid and the inverter currents, considering the passive damping as shown in Fig. 6(b), is given by

$$\frac{i_g(s)}{I_{\mathrm{inv}}(s)} = \frac{\frac{1}{L_g C}}{s^2 + s\frac{1}{R_d C} + \frac{1}{L_g C}}. \tag{14}$$

From (14), the bode diagram for different resistor values is given in Fig. 7.

To illustrate the proposed strategy, a current source that is proportional to the resonance component of the capacitor voltage $(I_d = k_d \cdot \tilde{u}_c)$ replaces the passive damping resistor, as shown in the equivalent circuit in Fig. 8. This controlled current source is used to actively damp any current oscillations due to filter resonance.

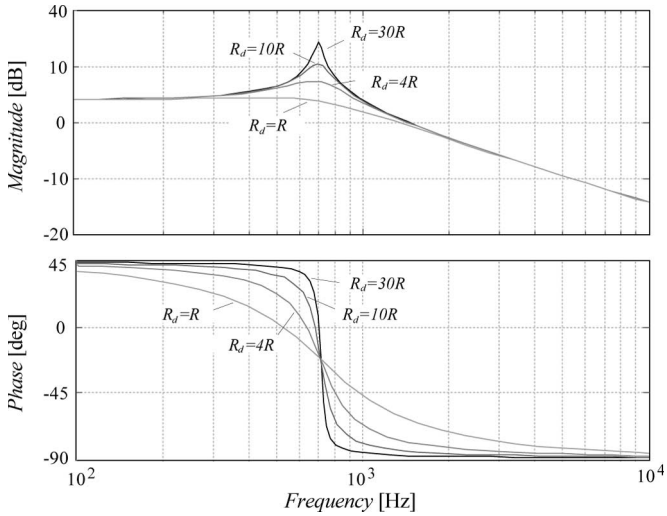

Fig. 7. Bode plot of an LCL filter characteristic with passive damping for different values of a damping resistor.

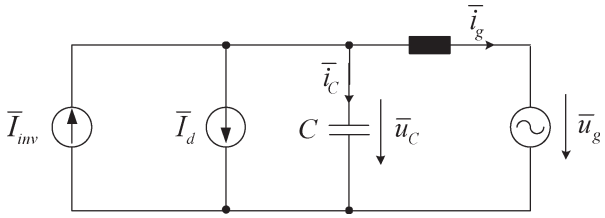

Fig. 8. Equivalent output stage with active damping.

By adding the active damping approach to the output LCL filter equivalent circuit, the transfer function from the grid to the inverter currents is then modified to

$$\frac{i_g(s)}{I_{\text{inv}}(s)} = \frac{\frac{1}{L_g C}}{s^2 + s\frac{k_d}{C} + \frac{1}{L_g C}}. \tag{15}$$

The relationship between the damping factor k_d and the parallel resistor R_d can be found by comparing the transfer function of passive (14) and active (15) dampings and is given by

$$k_d = \frac{1}{R_d}. \tag{16}$$

The undamped natural frequency (17) and the damping factor (18) can be calculated based on the output filter parameters (L_g and C) and the desired damping ratio (ξ)

$$\omega_n = \sqrt{\frac{1}{L_g C}} \tag{17}$$

$$k_d = 2\xi\sqrt{\frac{C}{L_g}}. \tag{18}$$

The active damping scheme is better explained through the block diagram in Fig. 9. The capacitor voltage $(u_{C,\alpha\beta})$ is initially calculated based on the measured capacitor current $(i_{C,\alpha\beta})$. In order to obtain the proportional damping current source $(I_{d,dq})$ value, the resonance component of the capacitor voltage $(\tilde{u}_{C,\alpha\beta})$, which is extracted by eliminating the fundamental frequency component through a notch filter, is transformed to the dq coordinates and is then multiplied by the damping factor (k_d). The capacitor voltage that is needed to calculate power quantities is obtained by converting the SRF capacitor voltage $(u_{C,\alpha\beta})$ to synchronous reference frame components. As the dq transformation is synchronously rotating in the same direction and speed as the capacitor voltage, the fundamental voltage appears as a dc component, and the ac parts (harmonics) are suppressed by a low-pass filter.

In order to obtain power quantities, the capacitor voltage is then multiplied by the complex conjugate of the proportional current source value that is given in the synchronous reference frame

$$p_d = \frac{3}{2}\text{Re}\left\{u_{C,dq} \cdot I^*_{d,dq}\right\} \tag{19}$$

$$q_d = \frac{3}{2}\text{Im}\left\{u_{C,dq} \cdot I^*_{d,dq}\right\}. \tag{20}$$

By solving (19) and (20), the active and reactive power damping components are found as

$$p_d = \frac{3}{2}u_{C,d} \cdot k_d \cdot \tilde{u}_{C,d} \tag{21}$$

$$q_d = -\frac{3}{2}u_{C,d} \cdot k_d \cdot \tilde{u}_{C,q}. \tag{22}$$

The damping components (p_d and q_d) are subtracted from the fundamental active and reactive power references, as shown in Fig. 3, and this provides an effective damping of the filter resonance.

An effect of the active damping control loop is the reduction of the harmonic currents that are present in the LCL filter resonance range. However, the reduction of these harmonic currents causes an increase in the low-order harmonics that are present in the capacitor current and, consequently, causes a reduction in the quality of the output current waveforms. This effect occurs because not only the resonance frequencies are used in the active damping controller but also all the other harmonics in the capacitor current are included into the active and reactive power references. One solution for this is to select a smaller damping factor so that capacitor current amplification is reduced, but the level of damping suffers. Another way to diminish this effect is the use of an active harmonic rejection controller.

B. Harmonics Rejection

In order to reduce the level of current harmonics that are injected into the grid, a method that is used to individually control the harmonics in their respective individual synchronous reference frames is introduced. This concept, as proposed by the study in [9], is implemented to compensate for the nonlinear load harmonics and load unbalance with a shunt active filter based on a dq reference frame PWM current controller. The basic idea behind this approach is the transformation of the three-phase voltage and current into dc quantities by employing

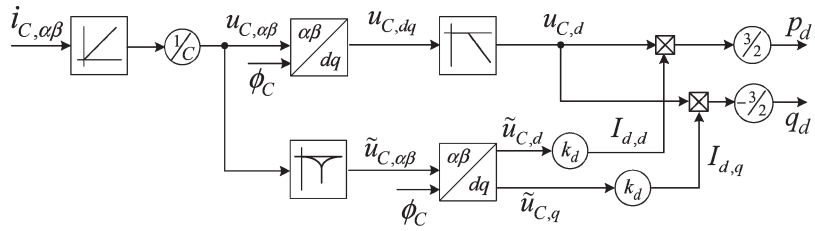

Fig. 9. Active damping block diagram.

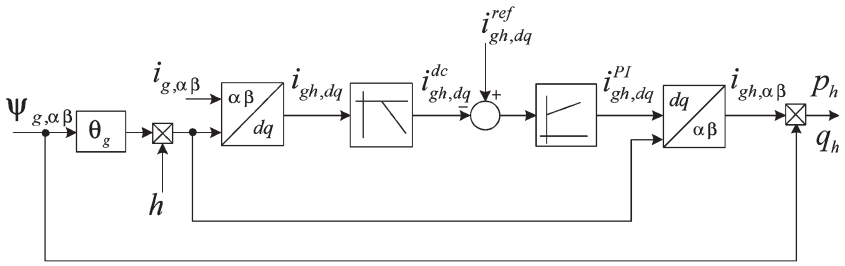

Fig. 10. Closed-loop individual harmonic current control.

the synchronous reference frame transformation, which is based on a synchronously rotating vector with the same direction as the voltages and currents.

Thus, if each harmonic quantity is transformed into its own individual synchronous reference frame, then these quantities appear as dc in their own reference frame, and consequently, a PI controller is sufficient to guarantee a zero steady-state error. All other harmonics will appear as harmonics with a changed order.

The block diagram in Fig. 10 shows the basic idea of such approach. The mains side current in the SRF $(i_{g,\alpha\beta})$ is transformed into an individual synchronous reference frame for the harmonic (h) of interest, as shown by the following:

$$\begin{bmatrix} i_{gh,d} \\ i_{gh,q} \end{bmatrix} = \begin{bmatrix} \cos(h\cdot\theta_g) & \sin(h\cdot\theta_g) \\ -\sin(h\cdot\theta_g) & \cos(h\cdot\theta_g) \end{bmatrix} \cdot \begin{bmatrix} i_{g,\alpha} \\ i_{g,\beta} \end{bmatrix}. \quad (23)$$

For the case where the transformation is done in an SRF, the space phasor relative rotational speed has exactly the same value as the harmonic order, as shown in Fig. 11. On the other hand, if the transformation is based on the dq coordinates, the relative rotation speed is equal to $n-1$, where n is the harmonic space phasor rotational speed. For example, in the case of the fifth harmonic, which has a rotational speed that is five times faster than the fundamental space phasor and in opposite direction, the relative rotational speed is minus six. To avoid inherent possible errors in these transformations, a PLL is implemented to generate the necessary angle for the SRF transformation.

In order to extract the dc component value (individual desired harmonic) from the output transformation, a first-order low-pass filter of (24), with a cutoff frequency that is at least one decade below the harmonic to be compensated, is used. As an alternative, the low-pass filter can be replaced by a moving average filter. This filter produces a perfect dc output in one ac

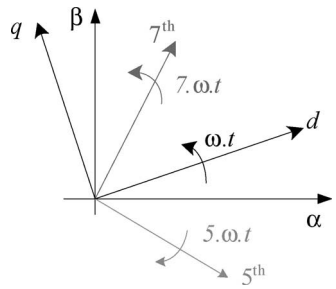

Fig. 11. Fundamental and harmonics phasor diagram.

cycle, whereas a low-pass filter only attenuates the ac quantities but cannot completely eliminate them

$$i^{dc}_{gh,dq} = \frac{1}{1+s\cdot T_1} i_{gh,dq}. \quad (24)$$

The dc quantity is then controlled by using a PI compensator (25), which tries to eliminate the steady-state error

$$i^{\mathrm{PI}}_{gh,dq} = k_p\left(1+\frac{1}{s\cdot T_i}\right)\cdot\left(i^{\mathrm{ref}}_{gh,dq} - i^{\mathrm{dc}}_{gh,dq}\right) \quad (25)$$

and then transformed back to the SRF using

$$\begin{bmatrix} i_{gh,\alpha} \\ i_{gh,\beta} \end{bmatrix} = \begin{bmatrix} \cos(h\cdot\theta_g) & -\sin(h\cdot\theta_g) \\ \sin(h\cdot\theta_g) & \cos(h\cdot\theta_g) \end{bmatrix} \cdot \begin{bmatrix} i^{\mathrm{PI}}_{gh,d} \\ i^{\mathrm{PI}}_{gh,q} \end{bmatrix}. \quad (26)$$

The output of this individual harmonic current controller is multiplied by the virtual grid flux by using (27) and (28) to estimate the individual harmonic active and reactive power controller outputs. These outputs override the fundamental

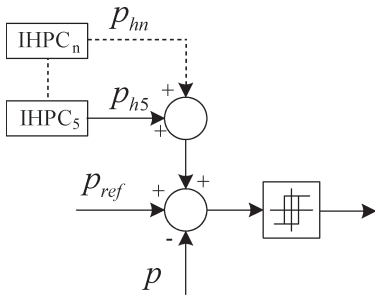

Fig. 12. Overriding harmonic power controllers.

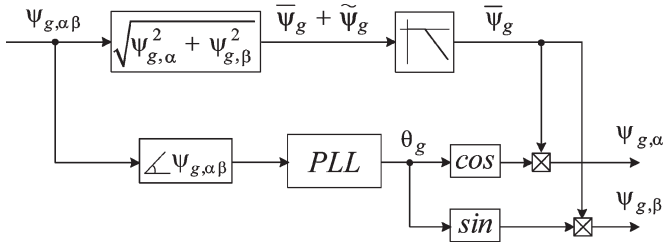

Fig. 13. PLL scheme.

active and reactive power references, as shown in Fig. 12, and effectively diminish the output harmonic current amplitudes

$$p_h = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{gh,\beta} - \psi_{g,\beta} \cdot i_{gh,\alpha}) \tag{27}$$

$$q_h = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{gh,\alpha} + \psi_{g,\beta} \cdot i_{gh,\beta}). \tag{28}$$

When the control of more then one harmonic is desired, the output of each individual harmonic power control (IHPC$_n$) is added to the reference (Fig. 12). The index n represents the harmonic to be controlled (5th, 7th, and 11th).

The number of harmonics to be compensated is limited by the LCL filter bandwidth, which is normally much lower than the sampling frequency that is used by the digital controller. This makes the controller insensitive to the sampling delays.

C. Phase-Locked Loop (PLL)

As the grid voltages are not always purely sinusoidal and balanced, a PLL is used to extract the fundamental phase and frequency. The simplest method, to obtain the phase information, is to detect only the zero crossing points of the utility voltages. However, since the zero crossing points can be detected only at every half-cycle of the mains frequency, the information during the rest of the cycle is missed. One of the most employed PLL methods is based on synchronous reference frame. Under ideal grid conditions, this approach provides satisfactory results; however, in case of a distorted grid voltage with high-order harmonics or under voltage unbalance, the tracking performance is highly dependent on the PLL bandwidth.

A PLL that is based on the virtual-flux stationary components is proposed by the study in [10]. The method compensates for the grid voltage distortion by employing a polar representation, as shown in the block diagram in Fig. 13. A low-pass filter is used to reject the ripple component that is present in the virtual-flux absolute value, while angle synchronization is implemented by a PLL. The compensated radial $(\overline{\psi}_g)$ and angle (θ_g) polar components are transformed back to rectangular coordinates.

IV. Simulation Results

In order to confirm the effectiveness of the proposed system, a MATLAB/Simulink model has been implemented. The steady state and dynamic performance of the proposed system are compared to the conventional DPC without active damping and harmonic rejection control. The electrical parameters for the simulation model are given in Table I.

TABLE I
Electrical Parameters for the Simulation Model

Rated output power	p=6kW
Phase voltage (RMS)	u_g=230V
DC-link voltage	u_{DC}=750V
Average switching frequency	fs=4kHz
Converter side inductance	L_{inv}=7.9mH
Grid side inductance	L_g=3.5mH
Filter Capacitance	C=14.1uF

The current oscillations that are caused by the LCL filter resonance when the conventional DPC is implemented can clearly be seen in steady-state mains current [Fig. 14(a)], as well as in the harmonic spectrum analysis [Fig. 14(b)]. A significant reduction of these oscillations when the proposed active damping is added to the main loop is observed in Fig. 14(c); however, the noise present in the capacitor current is injected to the system, increasing the low-order harmonics as shown in Fig. 14(d). In order to overcome this problem, the individual harmonic rejection that is tuned to the fifth harmonic is implemented. The fifth harmonic component is reduced from 2.1% of the fundamental to around 1.2%, as can be noted in the harmonic spectrum that is shown in Fig. 14(f).

Active damping signals (p_d and q_d) under a normal operation and during resonance are shown in Fig. 15. During the resonance period, the oscillations that are caused by the filter resonance are clearly noted in both signals.

Although the proposed system includes two additional loops compared to the conventional DPC, the main advantage of the DPC, which is a fast dynamic response, is kept. The response to a step of 40% on the converter-side active power reference [Fig. 16(b)] achieves a rise time of 900 μs, and this proves the effectiveness of the proposed approach.

The active damping significantly reduces the transient oscillations that are caused by the filter resonance, as can be seen by comparing the grid power and current of the conventional DPC [Fig. 16(c)–(e)] with the proposed method [Fig. 16(d)–(f)].

Fig. 16 also shows the effective compensation of the filter capacitor reactive power. In order to guarantee a null reactive power on the grid side [Fig. 16(d)], as set by the reference, the reactive power compensation loop forces the inverter to inject the appropriate amount of reactive power.

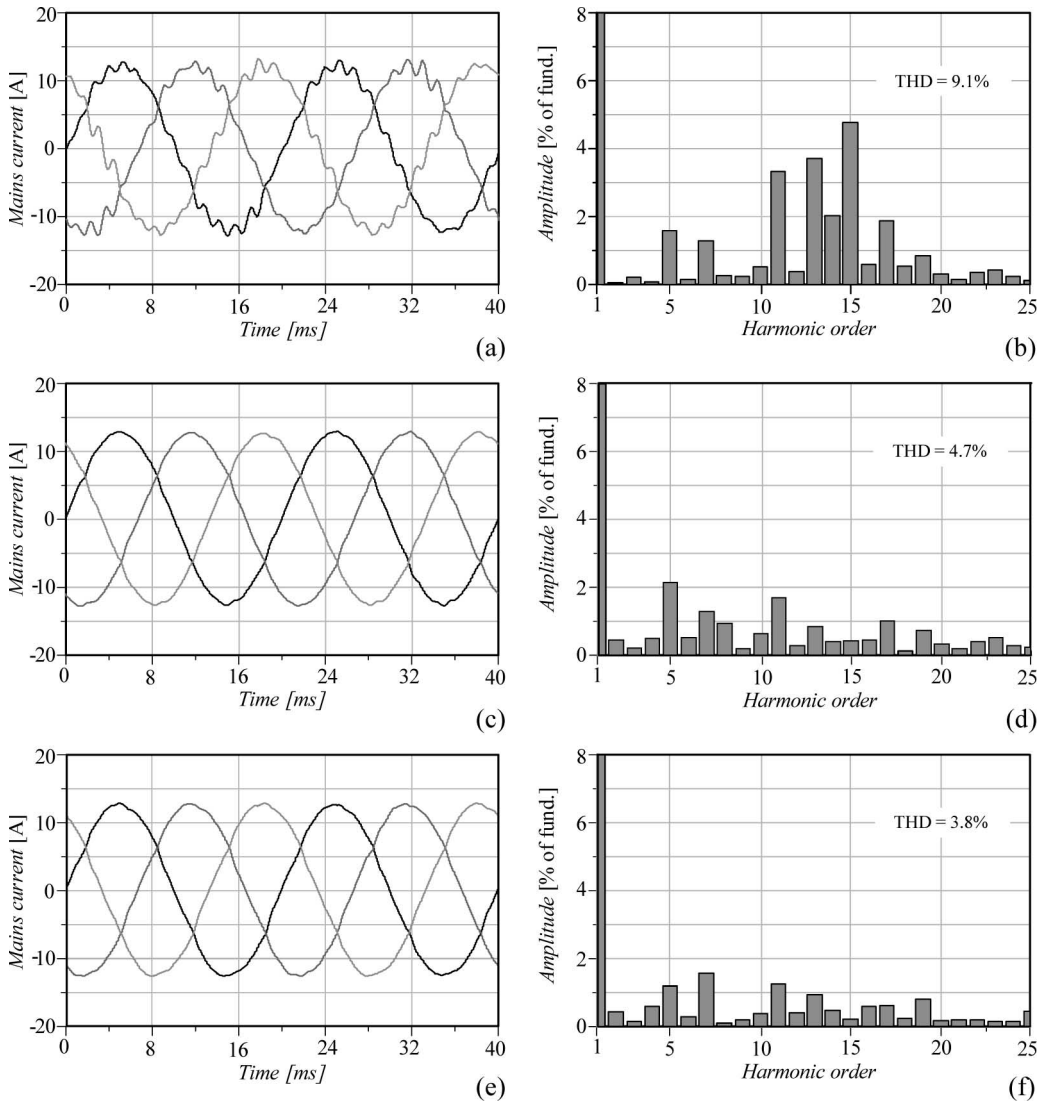

Fig. 14. Simulation results of the mains current and respective harmonic spectrum (a)–(b) of a conventional DPC, (c)–(d) of a system when the active damping approach is added to the main DPC loop, and (e)–(f) of the proposed system, with active damping and harmonic rejection control loops added to the conventional DPC.

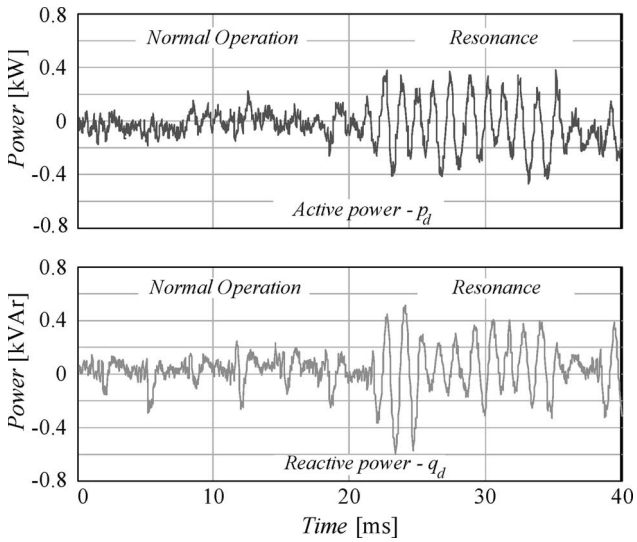

Fig. 15. Active damping signals (p_d and q_d) under normal operation and during resonance.

The values of the converter-side inductor (L_{inv}) and the grid-side inductor (L_g) may vary according to the operation point and aging. A small variation in one of these parameters may cause erroneous virtual-flux estimation, and consequently, an incorrect amount of active and reactive powers is generated by the inverter. To show the influence of these variations in system accuracy, simulations with different inductor values are analyzed. A variation in the range of $\pm 20\%$ of the filter inductances is considered, and the errors on the generated grid active and reactive powers are measured and presented in Fig. 17.

The inverter-side inductor (L_{inv}), with an inductance that is 20% smaller than the designed value, produces an error in the generated active power [Fig. 17(a)] of approximately 0.3%, while the error in the reactive power [Fig. 17(b)], for the same parameter variation, is 1.7%. This difference is explained by the fact that an alteration in the inductance value causes a change mostly on the estimated flux amplitude, while the effect on the phase is minimal.

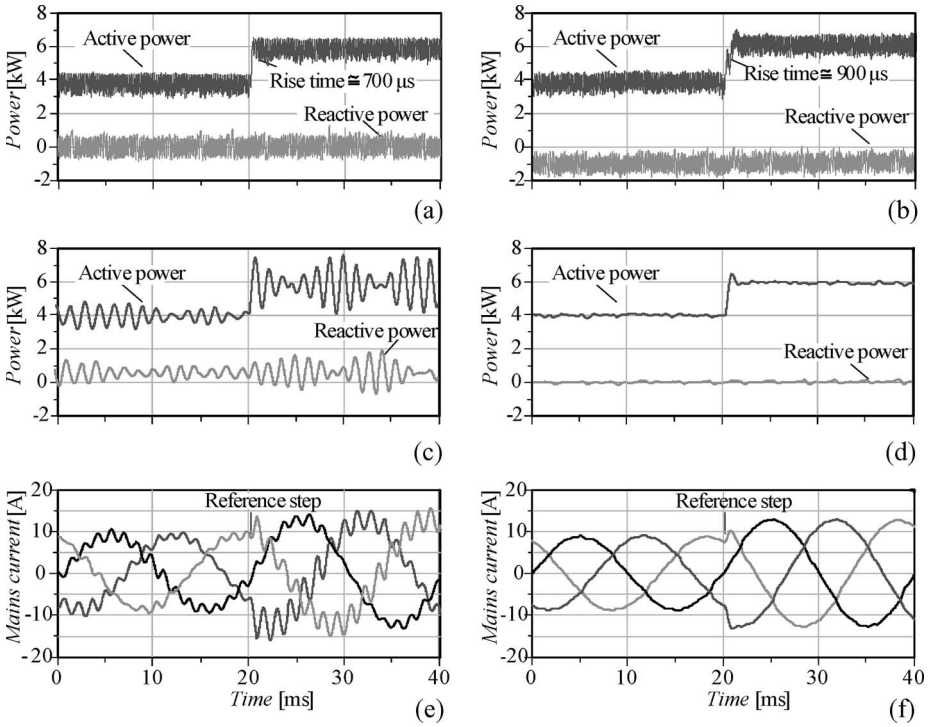

Fig. 16. Simulation time response of a reference step of 40% of the rated power in (a), (c), (e) the conventional DPC and (b), (d), (f) the proposed method. (a), (b) Converter-side active and reactive powers, (c), (d) grid-side active and reactive powers, and (e), (f) the grid current.

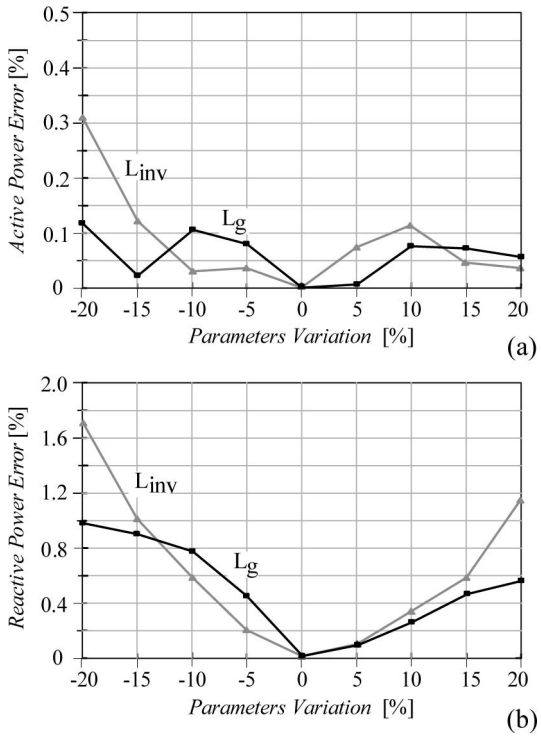

Fig. 17. Accuracy analysis of the active and reactive power estimation method. Error on the generated (a) active and (b) reactive powers that are caused by variations in the output filter parameters ($L_{\rm inv}$ and L_g).

A similar characteristic is observed when the grid-side inductor (L_g) value is changed. However, there is less influence since the grid-side inductance is smaller.

V. Experimental Verification

The experimental evaluation of the proposed virtual flux DPC (VF-DPC) is performed using a scaled lower power prototype that has the same low switching frequency as in a high-power application. The setup consists of a 6-kW inverter, with an averaged switching frequency of around 4 kHz, which is connected to a controlled 400-V 50-Hz three-phase ac power source via an LCL filter ($L_{\rm inv} = 7.9$ mH, $L_g = 3.5$ mH, and $C = 14.1$ μF). The dc power is supplied by two 10-kW 600-V controlled dc power supplies that are connected in series to provide a 750-V dc link. The VF-DPC control is implemented in a fully digital system using an Analog Devices ADSP21991 16-bit 160 MHz DSP. The DSP is interfaced to the inverter via a measurement and interface printed circuit board. Five analog signals (two grid currents, two capacitor currents, and the dc link voltage) are sampled at 140 kHz using the internal 14-bit analog-to-digital converter (ADC). During the ADC conversion time of 725 ns, the algorithm calculates the grid virtual flux based on the switch state and instantaneous dc input voltage, as well as the converter and grid-side inductor fluxes. The DSP selects the switch state based on the grid sector and the error between the calculated instantaneous power and the reference. The active damping and the sector decision are calculated in a separate control loop, with a sampling frequency of 40 kHz. The calculation of the harmonic control, which is adjusted to the fifth harmonic, and the PLL are updated at a rate of 20 kHz.

To limit the influence of possible low-order harmonic components that are present in the capacitor, the damping factor

ξ must be selected so that the capacitor current amplification is low but high enough to provide a sufficient level of damping. By substituting the desired damping ratio $\xi = 0.5$ and the output filter parameters (C and L_g) into (18), the damping constant k_d can be calculated ($k_d = 0.063$).

The effectiveness of the proposed approach with active damping and harmonic elimination can be seen by comparingthe grid current of the conventional VF-DPC [Fig. 18(a)] and the modified scheme [Fig. 18(c)]. The reactive power reference that is set to null is respected since the grid current is in phase with the grid voltage and/or 90° leading the grid virtual flux. A significant reduction of the total harmonic distortion (THD) is also observed [Fig. 18(b)–(d)] and is mainly caused by damping the resonance frequency (around 650 Hz), as well as the reduction of the fifth harmonic component. On the other hand, the seventh harmonic is slightly increased since, in the fifth harmonic control loop, the seventh harmonic appears as an ac component and it is not completely eliminated by the low-pass filter.

A decrease of the resonance disturbance during a step of 40% in the active power reference does not significantly affect the dynamic response, as can be seen by comparing the usual VF-DPC [Fig. 19(a)–(c)] with the proposed approach [Fig. 19(b)–(d)]. The rise time of 800 μs of the conventional system is increased to around 1 ms when the proposed scheme is implemented.

The system performance for unbalanced voltages, with $+10\%$ on phase R and -10% on phase S, is verified. Fig. 20(a) shows the unbalanced grid voltages which generate low-order harmonic distortion in the grid current due to the unbalanced calculated virtual flux [Fig. 20(c)]. A PLL is implemented, which guarantees a balanced virtual flux [Fig. 20(d)] and, consequently, good-quality grid currents [Fig. 20(b)].

Fig. 21 shows the waveforms in which a fifth harmonic voltage component of 5% is intentionally superimposed on the fundamental grid voltage. The presence of the resonance oscillations and the fifth harmonic component is observed [Fig. 21(a) and (b)] in the conventional VF-DPC. At the same time, the resonance oscillation is reduced by adding the active damping, and a significant amplification of the fifth harmonic component is verified [Fig. 21(c) and (d)] since the capacitor voltage and harmonics present are fed back into the power references. To overcome this drawback, the harmonic elimination loop is enabled [Fig. 21(e) and (f)], reducing the fifth harmonic component from 17% to around 1.5% and, consequently, the THD from 18.6% to 5.6%.

VI. Conclusion and Outlook

The adaptation of the conventional DPC to inverter systems, where a third-order LCL filter is required, is presented in this paper. The distortion that is caused by the filter resonance is suppressed through a novel active damping approach that acts together with an individual harmonic rejection controller. Both of these additional controllers are based on power quantities. The effectiveness of the proposed system for high-power applications is proved via simulation results, which show a

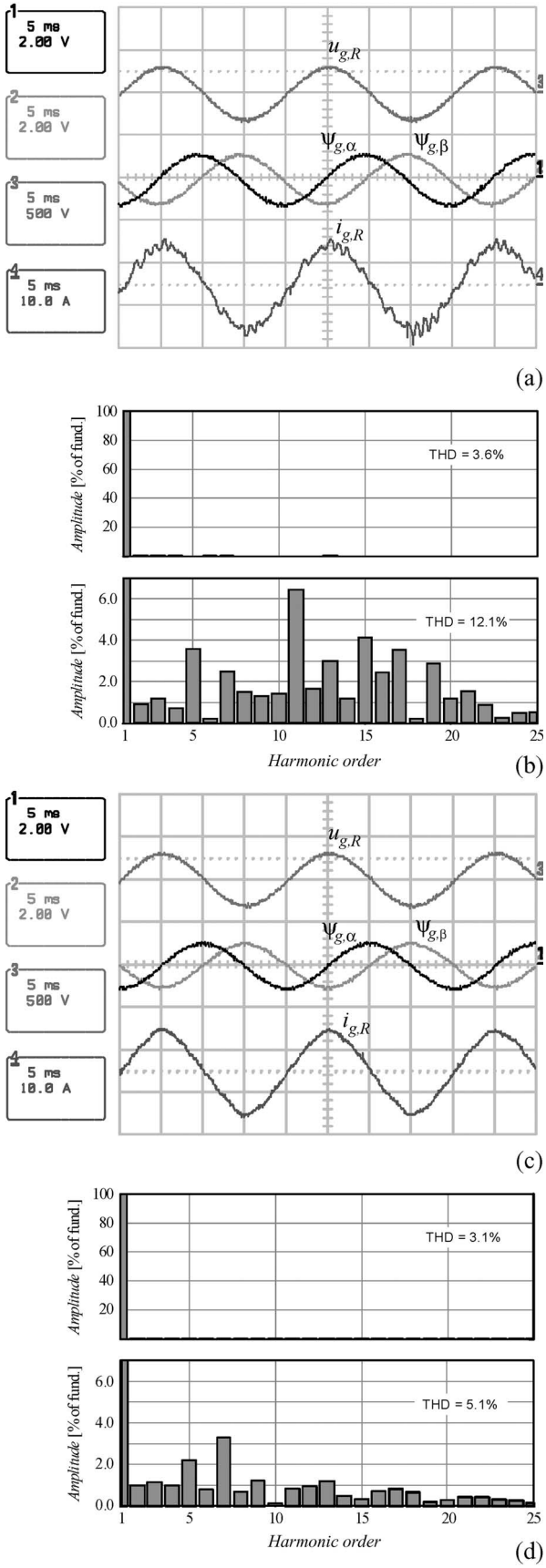

Fig. 18. Experimental result of the grid phase voltage $u_{g,R}$, virtual flux $\psi_{g,\alpha\beta}$, and phase current $i_{g,R}$ (a) for the conventional VF-DPC and (c) the proposed strategy, including the active damping and harmonic control. The voltage and current harmonic spectrums are shown in (b) and (d), respectively.

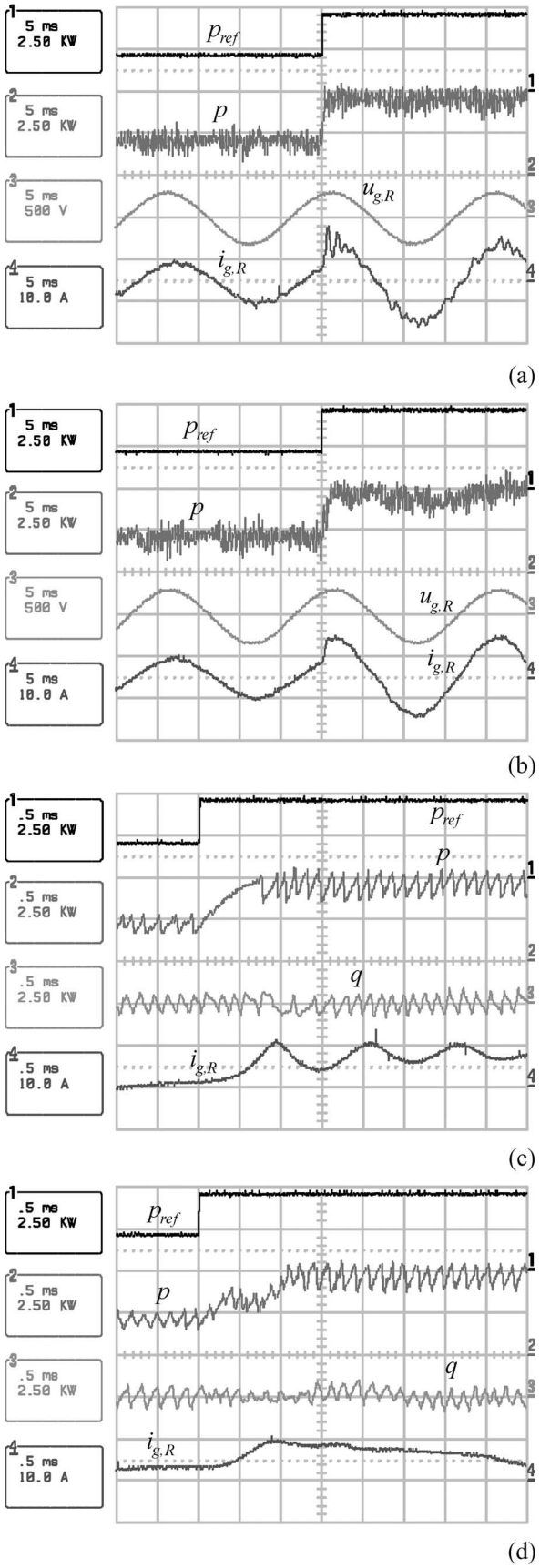

Fig. 19. Experimental results of a step in the active power reference of 40% with (a)–(c) the conventional VF-DPC and (b)–(d) the proposed system. Active power reference $p_{\rm ref}$, actual active and reactive powers p and q, respectively, grid phase voltage $u_{g,R}$, and current $i_{g,R}$.

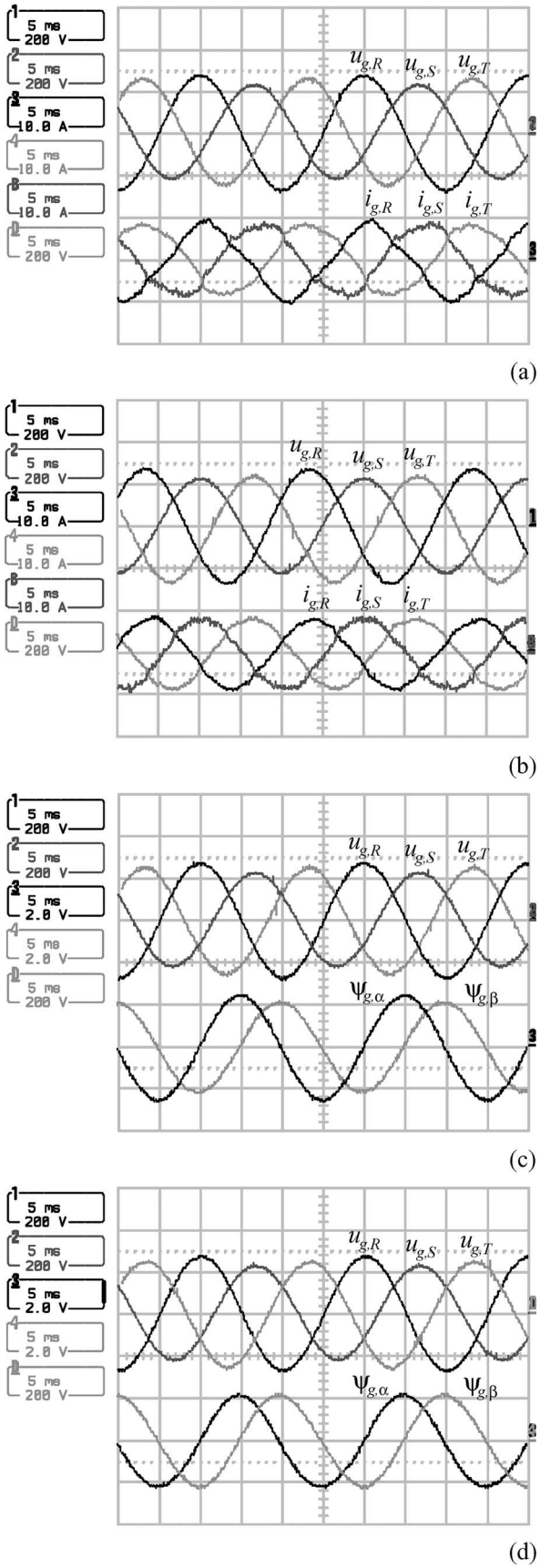

Fig. 20. Experimental results under the unbalanced grid voltage (phase R with $+10\%$, phase S with -10%, and phase T with 230 V rms). Grid phases current $i_{g,i}$ and grid virtual flux $\psi_{g,\alpha\beta}$ (a)–(c) without PLL and (b)–(d) with PLL, respectively.

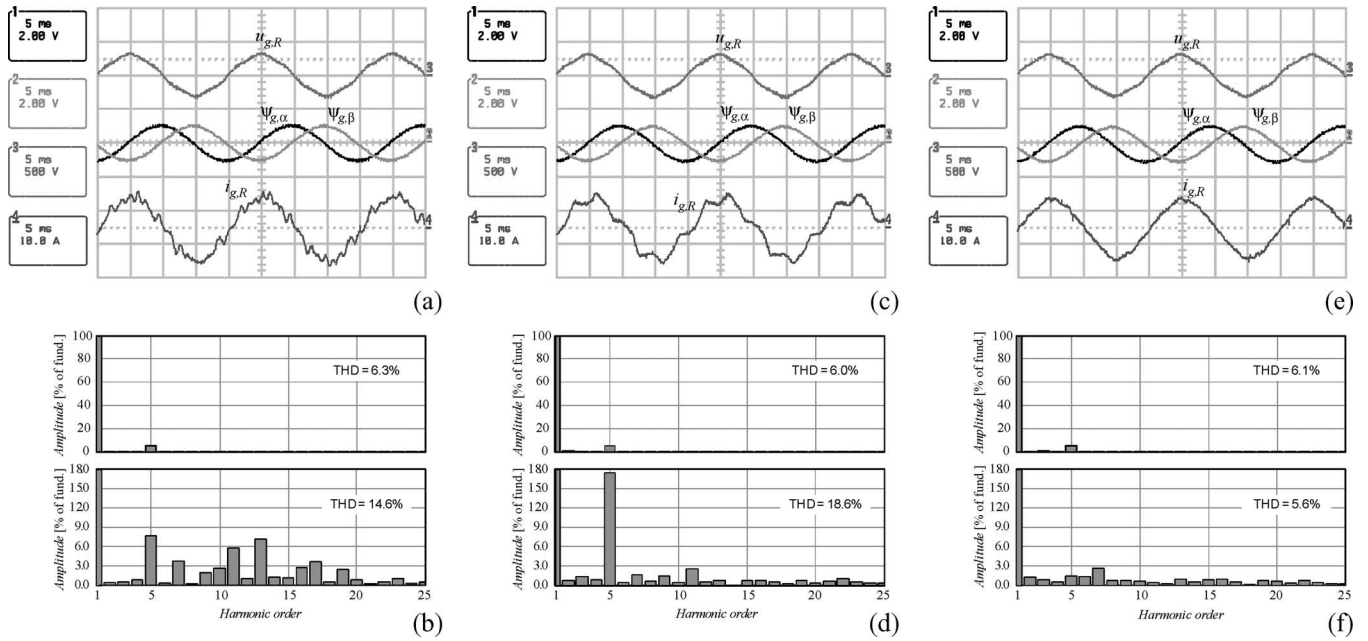

Fig. 21. Experimental results when 5% of the fifth harmonic is superposed the fundamental grid voltage. Grid phase voltage $u_{g,R}$, virtual flux $\psi_{g,\alpha\beta}$ and phase current, and respective voltage and current spectrum (a), (b) with the conventional VF-DPC, (c), (d) by adding the active damping, and (e), (f) by enabling the fifth harmonic control.

significant improvement in the steady state and transient behavior when compared to a conventional DPC. The same behavior is experimentally verified.The fast dynamic response to a reference step is not affected by the inclusion of the additional control loops. A good performance is guaranteed even under unbalanced and distorted grid voltages.

REFERENCES

[1] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron*, vol. 18, no. 3, pp. 888–895, May 2003.

[2] M. Liserre, A. D. Aquila, and F. Blaabjerg, "Design and control of a three-phase active rectifier under non-ideal operation conditions," in *Conf. Rec. IEEE IAS Annu. Meeting*, 2002, vol. 2, pp. 1181–1188.

[3] R. Wu, S. B. Dewan, and G. R. Slemon, "Analysis of a PWM AC to DC voltage source converter under the predicted current control with a fixed switching frequency," *IEEE Trans. Ind. Appl.*, vol. 27, no. 4, pp. 756–763, Jul./Aug. 1991.

[4] T. Noguchi, H. Tomiki, S. Kondo, and I. Takahashi, "Direct power control of PWM converter without power-source voltage sensors," *IEEE Trans. Ind. Appl.*, vol. 34, no. 3, pp. 473–479, May/Jun. 1998.

[5] M. Malinowski, M. P. Kazmierkowski, S. Hansen, F. Blaabjerg, and G. D. Marques, "Virtual-flux-based direct power control of three-phase PWM rectifiers," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1019–1027, Jul./Aug. 2001.

[6] V. Blasko and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 542–550, Mar./Apr. 1997.

[7] P. A. Dahono, "A control method to damp oscillation in the input LC filter of AC–DC PWM converters," in *Proc. IEEE PESC*, Jun. 2002, vol. 4, pp. 1630–1635.

[8] N. R. N. Idris and A. H. M. Yatim, "An improved stator flux estimation in steady-state operation for direct torque control of induction machines," *IEEE Trans. Ind. Appl.*, vol. 38, no. 1, pp. 110–116, Jan./Feb. 2002.

[9] S. Ponnaluri and A. Brickwedde, "Overriding individual harmonic current control with fast dynamics for active filtering," in *Proc. IEEE PESC*, 2001, pp. 1596–1601.

[10] M. Malinowski, G. D. Marques, M. Cichowlas, and M. P. Kazmierkowski, "New direct power control of three-phase PWM boost rectifiers under distorted and imbalanced line voltages conditions," in *Proc. IEEE ISIE*, 2003, vol. 2, pp. 831–835.

Leonardo Augusto Serpa (S'05) received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 2002 and 2004, respectively. He is currently working toward the Ph.D. degree at the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland.

Between July and December 2001, he was an internship student with the Center for Power Electronics Systems, VA. His research interests include control strategies of grid-connected inverter systems and multilevel converters.

Mr. Serpa is a member of the Brazilian Power Electronics Society.

Srinivas Ponnaluri was born in Guntur, India, on August 31, 1970. He received the B.E. degree in electrical engineering from Ravishankar University, Raipur, India, the M.E. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 1994, and the Ph.D. degree on design and control of grid-side converters with uninterruptible power system (UPS) features from the Technical University of Aachen, Aachen, Germany, in 2006.

Since 1994, he has been with the ABB Automation Power Electronics Division, Turgi, Switzerland, where he is currently a Senior Engineer. He is working mainly in the area of converters for railways distributed generation, UPS, and multilevel converters for future applications. He has approximately 15 years of experience in the industry. He is the holder of several patents and has authored several publications. He specializes in topologies, system design, simulation, and control of power-electronics-based equipment.

Peter Mantovanelli Barbosa (SM'06) received the Ph.D. degree from Polytechnic Institute and State University, Blacksburg, Virginia, in 2002.

He is currently leading the Power Electronics and System Applications Group, ABB Corporate Research, Baden, Switzerland.

Dr. Barbosa is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS.

Johann Walter Kolar (SM'89–M'91–SM'04) received the Ph.D. degree (*summa cum laude*) from the University of Technology Vienna, Vienna, Austria.

Since 1984, he has been teaching and working in research, in close collaboration with international industry, in the fields of high-performance drives, process technology, and uninterruptible power supplies. He has proposed numerous novel converter topologies, e.g., the Vienna Rectifier and the three-phase ac–ac sparse matrix converter concept. He has published over 250 scientific papers in international journals and conference proceedings and has filed more than 50 patents. He was appointed as a Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zurich, on February 1, 2001, where he is currently working. The focus of his current research is on ac–ac and ac–dc converter topologies, with low effects on the mains, e.g., for power supply of telecommunication systems, more-electric-aircraft, and distributed power systems in connection with fuel cells. Other main areas of interest include the realization of ultracompact intelligent converter modules that are employing the latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multidomain/multiscale modeling and simulation, pulsed power, bearingless motors, and power microelectromechanical systems.

Dr. Kolar is a member of the Institute of Electrical Engineers of Japan (IEEJ) and of the technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and since 2001, he has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he has been an Associate Editor of the *Journal of Power Electronics* of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*. He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003.