Virtual-Flux Direct Power Control for Mains Connected Three-Level NPC Inverter Systems

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***Abstract* - This paper proposes a control strategy which extends the Virtual-Flux Direct Power Control traditionally employed for the conventional two-level VSI to a three-level NPC inverter. This topology generates a higher number of output voltage levels, increasing the flexibility for selecting an appropriate voltage vector. The mid-point potential is controlled according to the direction of the mid-point current and the sign of the mid-point voltage deviation. The method is adapted to be used with an LCL output filter, where some undesirable characteristics, such as filter resonance, have to be compensated. Further investigation concerning the dependency of the mid-point voltage with the current phase-shift is given. Theoretical analysis is presented and the performance of the proposed method is verified by simulation.**

***Index Terms*—Direct Power Control, Grid Connected, Three-Level NPC.**

I. INTRODUCTION

For high power systems the use of direct power control (DPC) is spreading in the last few years due to the advantages, such as a fast dynamics and simplicity, when compared with other methods. For instance the voltage oriented control method guarantees a high static performance via an internal current control loop but suffers from a low dynamic performance and is affected by the stability requirements of the feedback loop [1]. Predictive control [2] gives optimal performances, in terms of both response time and accuracy; however it involves considerable calculation effort and requires a good knowledge of load parameters.

The basic idea of the DPC approach is the direct control of active and reactive power without any internal control loop or PWM modulator. The switching states are selected via a switching table and the states are chosen based on the instantaneous error between the estimation and the desired active and reactive power.

Traditionally, the DPC was investigated for low power applications [3] where normally the standard two-level topology is employed. However, high voltage applied to the semiconductors limits the use of this topology for high power and high voltage applications, an area in which multilevel inverters are emerging.

Since its introduction in 1981 [4], the three-level neutral-point-clamped (NPC) voltage source inverter (Fig. 1) has demonstrated some advantages over the conventional two-level inverter. It has been applied in medium and high power applications due to the inherent advantages, namely: voltage across the switches is clamped to half of the dc-link, produces low output voltage and current harmonic distortion and reduces the dv/dt stress on the load. However, the NPC-VSI has a problem that excessive high voltages may be applied to switching devices, when the floating neutral point potential varies from the mid-potential of the dc-link voltage.

Therefore, to take full advantage of this topology the mid-point of the dc-link must remain clamped at one half of the complete dc-link voltage. The possibility of influencing the mid-point potential is based on the existence of redundant switch states concerning the voltage space vector generated at the output of the inverter [5]. The redundant switching states are characterized by opposite loading of the mid-point current [6]. Therefore, this allows the control of the mid-point potential without any influence on the output voltage.

When using a three-level inverter, the selection of the output voltage vectors becomes more complex due to higher number of available inverter states, however it provides more flexibility for choosing an appropriate voltage vector.

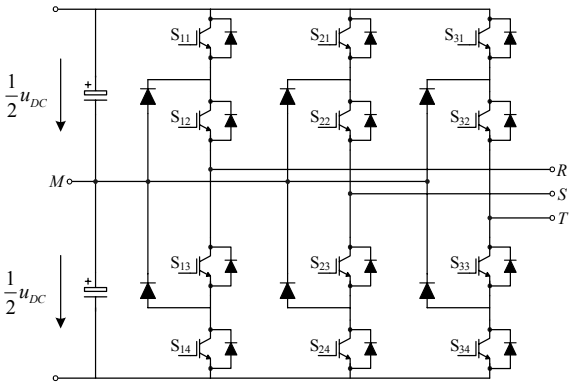

Fig. 1. Three-Phase Three-Level NPC Voltage Source Inverter.

For high power applications a third order output filter that can achieve reduced levels of harmonic distortion at lower switching frequencies and with less total inductance is usually employed. However, systems incorporating LCL filters require extra control effort in order to compensate undesirable characteristics such as the filter resonance.

This paper presents a sensorless direct power control scheme, employing a three-level NPC inverter connected to the grid. The proposed scheme includes a special method to avoid a dc-link capacitor voltage unbalance. In Section II the basic concept of direct power control is discussed and the calculation of active and reactive power estimation is given. In order to adapt the standard DPC to be used with three-level inverter, a strategy to increase the number of utilized space vectors as well as a method for balancing the mid-point potential is presented in Section III. The basis of controlling the potential of the mid-point *M* is given by the knowledge of the mid-point current i_M and the mid-point voltage deviation. The proposed approach is proved by simulation in Section IV. Section V adapts the virtual-flux direct power control (VF-DPC) for a system with third order LCL filter. Finally, Section VI verifies the extended method by simulation.

II. Principle of Direct Power Control

The basic principle of the Direct Power Control (DPC) was proposed by Noguchi [3] and is based on the well know Direct Torque Control (DTC) for induction machines. In the DPC, the active and reactive powers replace the torque and flux amplitude used as the controlled output in the DTC. The basic concept consists of selecting the appropriate switching states from a switching table based on the errors, which are limited by a hysteresis band, present in the active and reactive powers as illustrated in Fig. 2.

In order to correctly estimate the power and at the same time reduce the numbers of implemented voltage sensors, Noguchi proposes the use of voltage vector estimation. The implementation of such approach involves the computation of the time derivative of the measured currents. The use of a derivative can increase the noise in the control loop, thus increasing the level of distortion.

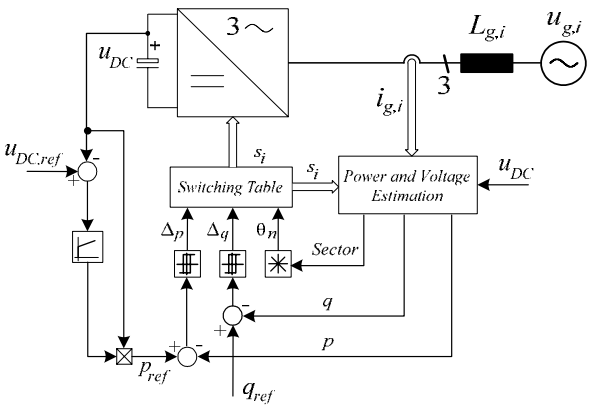

Fig. 2. Block diagram of conventional Direct Power Control.

Recently the Virtual Flux strategy was proposed [7], which assumes basically that the grid voltage and the ac-side inductors are quantities that are related to a virtual ac motor. Making an analogy with ac motors, R_g and L_g (Fig. 3) represent the stator resistance and the stator leakage inductance respectively and the grid voltage $\bar{u}_g$, represents the machine's electro-motive force.

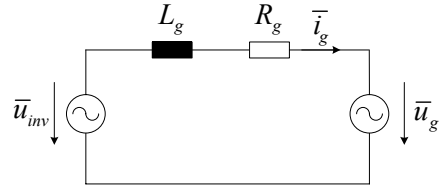

Fig. 3. Equivalent circuit of a grid connected three-phase VSI with L filter.

Appling the flux definitions of (1) and the voltage loop equation of (2), the grid virtual flux can be estimated.

$$\bar{\psi}_g = \int \bar{u}_g \cdot dt \tag{1}$$

$$\bar{u}_g = \bar{u}_{inv} - R_g \cdot \bar{i}_g - L_g \cdot \frac{d\bar{i}_g}{dt} \tag{2}$$

Neglecting the series resistance of the line inductor, the line virtual flux can be calculated based on the measured line current $\bar{i}_g$ and the inverter voltage $\bar{u}_{inv}$

$$\bar{\psi}_g = \int \bar{u}_{inv} \cdot dt - L_g \cdot \bar{i}_g \tag{3}$$

where the inverter output voltage in the stationary coordinate system can be calculated based on the dc-link voltage and the converter switching states.

Based on the grid virtual flux and current the active and the reactive power, as developed in [7], can be estimated as

$$p = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{g,\beta} - \psi_{g,\beta} \cdot i_{g,\alpha}) \tag{4}$$

$$q = \frac{3}{2}\omega \cdot (\psi_{g,\alpha} \cdot i_{g,\alpha} + \psi_{g,\beta} \cdot i_{g,\beta}) \tag{5}$$

where the stationary ($\alpha\beta$) transformation is according to

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} u_R \\ u_S \\ u_T \end{bmatrix}. \tag{6}$$

III. VF-DPC for Three-Level NPC Inverter

In the Neutral-Point Clamped inverter presented in Fig. 1, each phase can produce three distinct levels by connecting the output either to the positive ($u_{DC}/2$), negative ($-u_{DC}/2$) or null (0) potential. In a three-phase system it results in $3^3 = 27$ output voltage vectors.

The output voltage space vector can be classified into four categories according to its magnitude, namely: zero space vector V_0 which corresponds to three

configurations that produces null output voltage, half vectors (V_1, V_2, V_3, V_4, V_5 and V_6) that create a voltage space vector with amplitude equal to $u_{DC}/3$, medium vectors (V_8, V_{10}, V_{12}, V_{14}, V_{16} and V_{18}) with an amplitude of $\sqrt{3}\cdot u_{DC}/3$ and the full voltage vectors (V_7, V_9, V_{11}, V_{13}, V_{15} and V_{17}) that generate a space vector with amplitude equal to $2\cdot u_{DC}/3$.

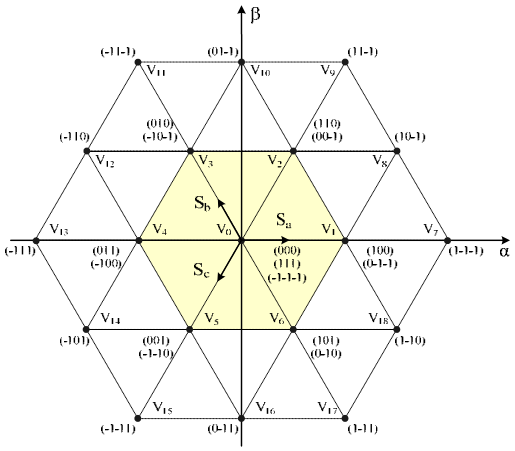

Fig. 4. Space vector diagram of three-level inverter.

Although in a three-level inverter there are 27 possible states, some of them apply the same voltage vector. There are two possible configurations for each small vector and three for the zero vectors. Therefore, 19 different vectors V_0 to V_{18} are available as shown in Fig. 4.

The voltage vectors are identified for example by (1 0 0) or (1 0 -1), where each column represents one phase (*R*, *S* and *T*) and the numbers 1, 0 and -1 indicate the phase connection to the positive, neutral and negative point of the dc-link, respectively.

The proposed VF-DPC scheme (Fig. 5) to be employed with three-level NPC inverter is a natural extension of the classical VF-DPC [7][8] used previously for two-level systems. Some modification must be done in order to minimize the output voltage harmonic distortion and to assure the balance of the mid-point voltage by appropriate selection of the redundant vectors.

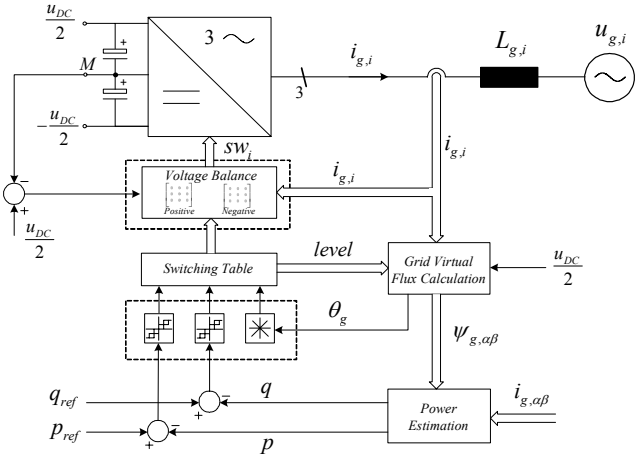

Fig. 5. Block scheme of the VF-Direct Power Control for three-level NPC inverter.

Fig. 5 shows that the main idea of the VF-DPC is maintained. The inverter switching states are appropriately selected by a switching table according to the instantaneous error between references and estimated values of active and reactive power. However, to permit more flexibility in the vector selection, a single band hysteresis is replaced by a double band strategy and to achieve a proper mid-point balancing, a method to decide on the correct redundant vector is employed.

A. Voltage Vector Selection

With 27 possible choices for space vector selection, the Switching Table in three-level inverters becomes more complex comparing with two-level inverters, however it allows much more possibilities for appropriate voltage vector selection to satisfy the commutation condition.

In order to utilize this benefit, a double band hysteresis method is applied as shown in Fig. 6.

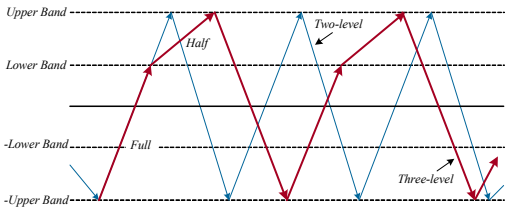

Fig. 6. Active or reactive power error variation in two and three-level inverters.

When active/reactive power error comes down to negative upper band, a full voltage vector is chosen. A half vector replaces the full vector when the error reaches the positive lower band, resulting in a lower slope of the active or reactive power. If the error increases beyond the positive upper band, a full voltage vector is applied to decrease the error or increase the instantaneous active or reactive power.

As consequence of selecting more voltage space vectors in the three-level inverter DPC, the harmonic content in the output voltage and current can be reduced.

B. Mid-Point Balance

The mid-point balance is not influenced by all the vectors. Large vectors do no affect the mid-point balance, since the phase currents are connected to either the positive or negative potential. Medium vectors connect one of the phase currents to the mid-point making the *M* potential dependent on the load conditions. They are the most important source of mid-point potential unbalance. As mentioned before, small vectors come in pair, as shown, for example, by the vector V_1 in Fig. 7. These states apply equivalent voltages to the output; however the orientation of the mid-point current differs. In one state, the current flows out of *M*, effectively discharging the lower capacitor of the dc-link while charging the upper capacitor. In the opposite state, the current flows into the mid-point, charging the lower capacitor and consequently discharging the upper capacitor.

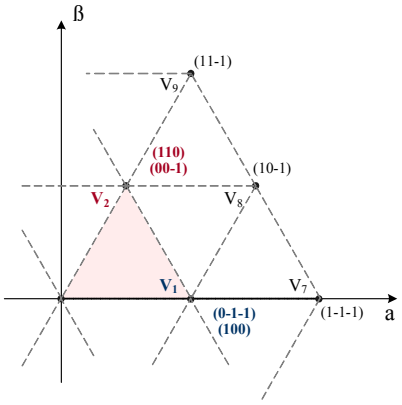

Fig. 7. Redundant vectors presented in the voltage space vectors of a three-level inverter.

An illustration of the effect caused by redundant switching states (0 -1 -1) and (1 0 0) of the space vector V_1 in the mid-point current can be seen in Fig. 8. Although the line-to-line voltages produced by both switching states are identical ($u_{RS}=u_{DC}/2$, $u_{ST}=0$ and $u_{TR}=-u_{DC}/2$), the mid-current generated are in opposite direction.

Assuming positive current in the phase *R* and negative current in the phases *S* and *T*, the mid-point current flows out of the mid-point when the state (0 -1 -1) is selected (Fig. 8(a)). In this case the upper capacitor is charged and the lower capacitor is discharged. An opposite effect on the capacitors voltages is observed when the state (1 0 0) is choose, since the mid-point current now flows into the mid-point, as shown in Fig. 8(b).

The presence of these redundant vectors creates a degree of freedom for controlling the mid-point potential by knowing i_M and the mid-point voltage deviation.

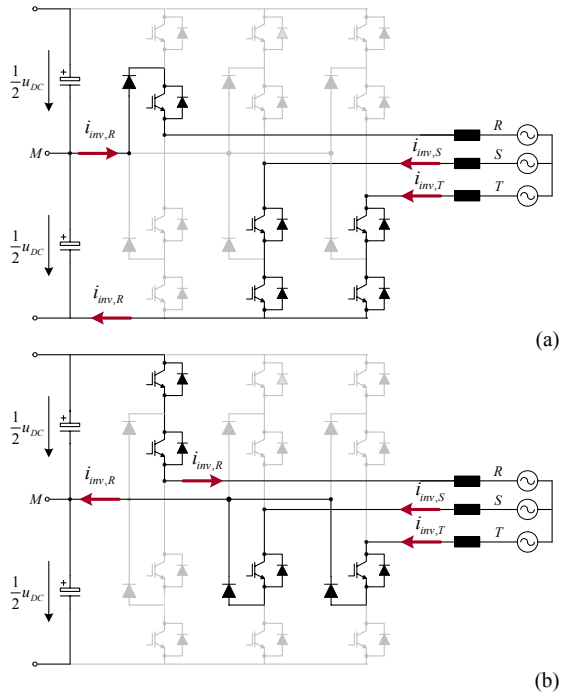

Fig. 8. Influence caused by the redundant vector in the mid-point current (a) positive small vector (0 -1 -1) and (b) negative small vector (1 0 0).

The deviation is measured by the difference between the voltage reference and the voltage across the lower capacitor, as shown in (7).

$$\Delta u_{C_l} = u_{C_l,ref} - u_{C_l} \tag{7}$$

Each phase has influence on the mid-point current i_M only when the respective phase is connected to the mid-point potential.

Therefore, i_M can be calculated based on the measured phase currents and the state of each phase:

$$i_M = mp_R \cdot i_{inv,R} + mp_S \cdot i_{inv,S} + mp_T \cdot i_{inv,T} \tag{8}$$

where mp_i is equal to 1 if the phase $i=R,S,T$ is connected to the mid-point potential, and 0 when the phase is connected either to the positive or negative potential.

Based on the direction of the generated i_M and the lower capacitor voltage deviation (Δu_{C_l}), the controller selects the appropriate redundant state, as shown in Fig. 9.

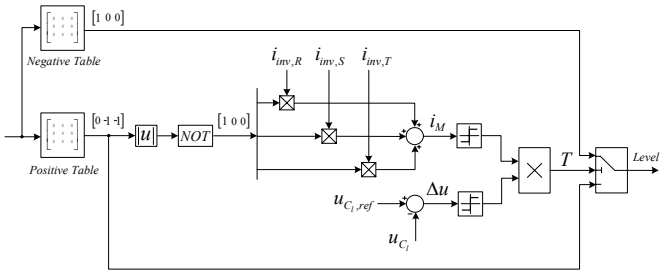

Fig. 9. Block diagram of the Mid-Point voltage control.

The switching table is divided into a positive and a negative part, which contain the same structure except the small vectors (redundant) that are allocated according to the effect on the mid-point current. A small vector that produces a positive i_M will be referred as a positive small vector and the one which generates a negative i_M, will be called as a negative small vector.

Initially, the vector to be applied to the NPC inverter is selected by the positive switching table, according to the hysteresis and sector indication. By knowing the state to be applied and the instantaneous measured phase currents, the resulting i_M is predicted using (8). If the predicted i_M would increases even more the mid-point potential deviation, the opposite redundant vector is selected by switching to the negative switching table.

For example, the hysteresis and sector indicate the small vector V_1 as the appropriate choice. A priori the positive small state (0 -1 -1) is selected by the positive switching table. As a result, according to (8), the mid-point current is identical to the current in phase *R*, since only this phase is directly connected to the mid-point *M*.

Assuming a positive current in phase *R* and a positive capacitor voltage deviation ($\Delta u_{Cl} > 0$), if the chosen state (0 -1 -1) is applied to the NPC inverter, a resulting positive $i_M = i_{inv,R}$ would discharge the lower capacitor, consequently increasing the deviation. In this case the

opposite negative small vector (1 0 0), which generates a negative current, $i_M = -i_{inv,R}$, must be employed to charge the lower capacitor and reduce the voltage deviation.

The logic decision to switch among the positive and negative table is summarized in TABLE I. If both i_M and Δu_{Cl} have the same signal, either positive (1) or negative (-1), the negative switching table is selected ($T=1$), otherwise the state choose by the positive table is maintained ($T=-1$). This logic can be simply implemented by multiplying i_M by Δu_{Cl}, as presented in Fig. 9.

TABLE I

LOGIC DECISION AMONG POSITIVE AND NEGATIVE TABLE.

i_M	Δu_{Cl}	T
-1	-1	1
-1	1	-1
1	-1	-1
1	1	1

IV. SIMULATION RESULTS

In order to verify the effectiveness of the proposed VF-DPC for three-level NPC inverter, simulations have been performed. The output inductance of 18mH links between the inverter and the grid (400V / 3-phase). The inverter, designed to operate with an average switching frequency of 2.5kHz, is supplied by an 800V DC power source.

The estimated grid virtual-flux ($\Psi_{g,\alpha\beta}$), lagging in 90° the grid phase voltage, is showed in Fig. 10(a). The virtual-flux is used to calculate the instantaneous active and reactive power applied to control the grid current illustrated in Fig. 10(b). The grid current is in phase with the grid voltage, since the reactive power reference is set to zero.

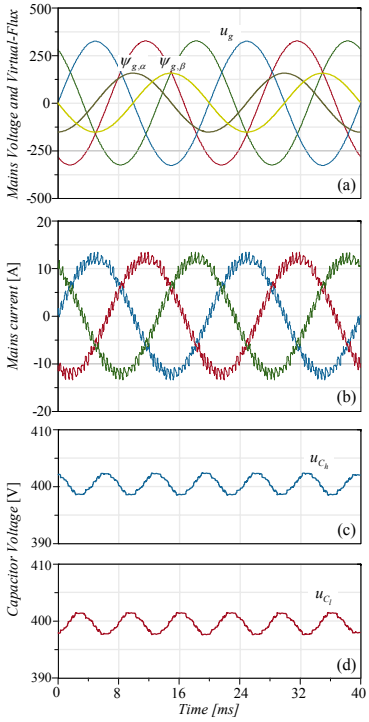

Fig. 10. Simulation results of the proposed VF-DPC with L filter. Grid voltage and estimated virtual-flux (a), resulting grid current (b) and voltage across the upper and lower dc-link capacitors (c)-(d).

Fig. 10(c),(d) show the voltage across the upper and lower dc-link capacitors clamped at one half of the complete dc-link voltage. It proves the efficacy of the proposed mid-point voltage control strategy, which uses the benefits of redundant vector.

V. VF-DPC FOR HIGH POWER APPLICATION

The proposed DPC system can be adapted to be used with a third order LCL output filter and therefore achieve reduced levels of harmonic distortion for a VSI operating with a low switching frequency. The LCL filter attenuates the switching ripple substantially and the overall size of the LCL filter is reduced compared to only an L filter. However, systems incorporating LCL filter requires extra control effort in order to compensate some undesirable characteristics such as the filter resonance. The modified VF-DPC showed in Fig. 11 maintains the core of the conventional approach and incorporates outer control loops which damp the filter resonance, reject the influence of grid voltage harmonics [8][9] and compensate for the reactive power of the capacitor, since the active and reactive power are controlled on the inverter side.

Since the switching states are selected via a switching table, there is no modulation index or common control signal within the control loops where outer loops control signal can be directly added. To overcome this limitation the active damping control, as well as the individual harmonic rejection control have to be implemented by acting directly on the active and reactive power components. These control signals have to be added to the fundamental references (p_{ref} and q_{ref}).

The active damping strategy can be applied effectively because the resonance frequency of the output filter is usually inside the bandwidth of the inverter control loops. The active damping is achieved by emulating a resistor in parallel with the filter capacitor by creating a current source proportional to the capacitor voltage resonance component.

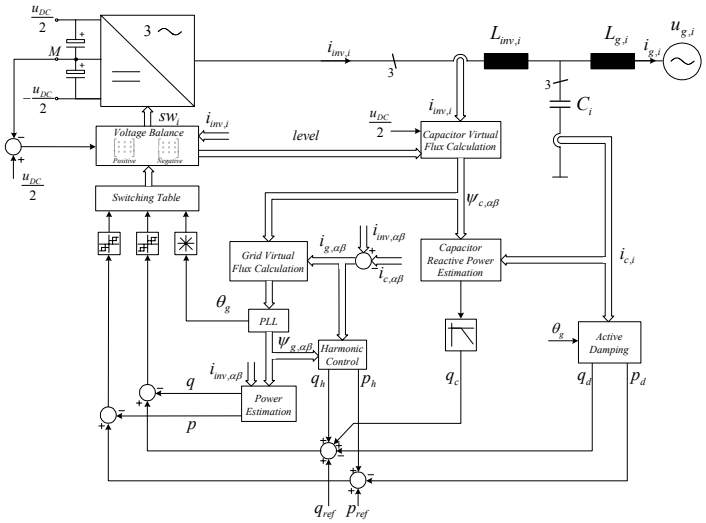

Fig. 11. Block diagram of the extend VF-DPC with active damping, harmonic control, phase-locked loop and reactive power compensation.

The harmonic control block proposed in [8][9] regulates the harmonics individually in their respective individual synchronous reference frame. Each harmonic quantity to be controlled is transformed into its own individual synchronous reference frame. The corresponding harmonic quantities appear as dc in their own reference frame, consequently a PI control is enough to guarantee zero steady state error.

VI. Simulation Results for the Extended Approach

To confirm the efficacy of the extended VF-DPC with an LCL output filter, simulations have been carried out. The setup consists of a 6kW NPC inverter, with an averaged switching frequency of around 2.5kHz, connected to a controlled 400V - 50Hz 3-phase AC power source via an LCL filter (L_{inv}=17mH, L_g=5.6mH and C=18μF).

The oscillation caused by the filter resonance is reduced when the active damping loop is added to the conventional approach, as can be seen comparing the grid current (Fig. 12(a),(d)) and the respective harmonic spectrum (Fig. 12(b),(e)) for the conventional and extended method. The mid-point balance is guaranteed even when the outer control loops are added to the conventional DPC as shown in Fig. 12 (c),(f).

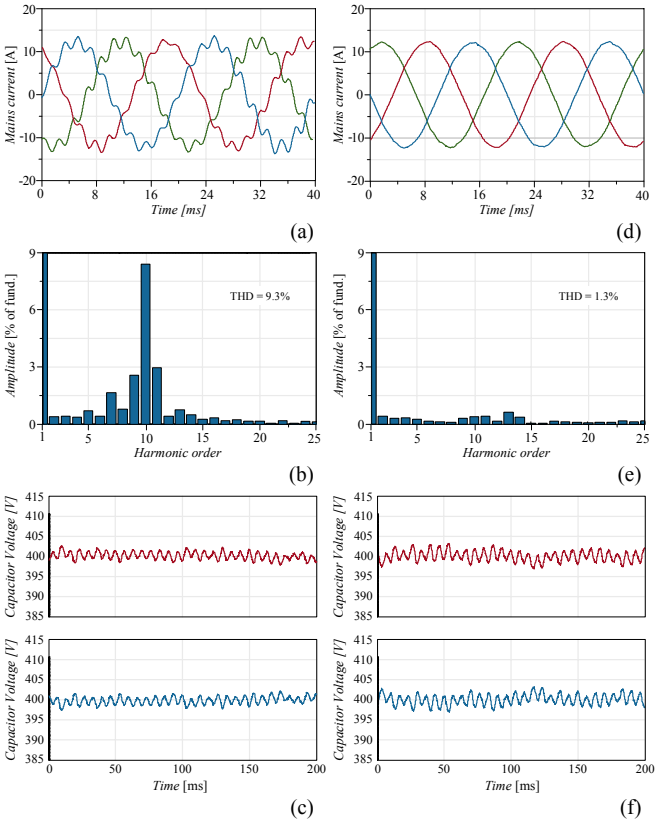

Fig. 12. Simulation results of mains current, respective harmonic spectrum and voltages across the dc-link capacitors (a), (b) and (c) provided by conventional DPC (d), (e) and (f) when the active damping approach and harmonic rejection control loops are added to the main DPC.

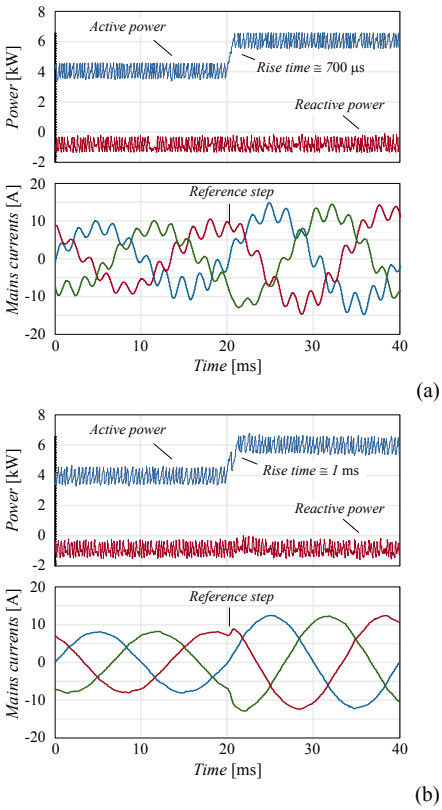

Fig. 13. Simulated time response of the proposed system to a reference step (a) and the extended method with active damping and harmonic control (b).

Although the rise time is increased by 300μs, the extended method, Fig. 13(b), reduces significantly the resonance during a step of 35% on the active power reference.

Fig. 14 shows simulation results in which 5% of the fifth harmonic component is superposed on the fundamental grid voltage. The effect caused on the grid current by the 5th harmonic is now added to the oscillations due to the filter resonance, resulting in a high total harmonic distortion (THD=11.9%) as shown in the spectrum analysis of Fig. 14(b). By enabling the active damping and harmonic control loops both the resonance oscillation and fifth harmonic component effects are suppressed as can be observed in the grid current presented in Fig. 14(c) and proved by the harmonic spectrum shown in Fig. 14(d). The THD is reduced from 11.9% to around 1.8%.

The dependency of the mid-point voltage control with the grid current phase-shift is also verified by simulation. Fig. 15 shows the voltage across the dc-link capacitors for three different operation points. Initially, the system is performed with a cosφ=0^o, which assures a proper mid-point balance control. By forcing, at 100ms, the grid current to lag in 45^o the grid voltage, the oscillations on the capacitors voltage are increased; however the efficacy of the mid-point voltage control remains valid. Similar behaviors on the capacitors voltage are observed at 200ms when the phase-shift between voltage and current is increased to 90^o.

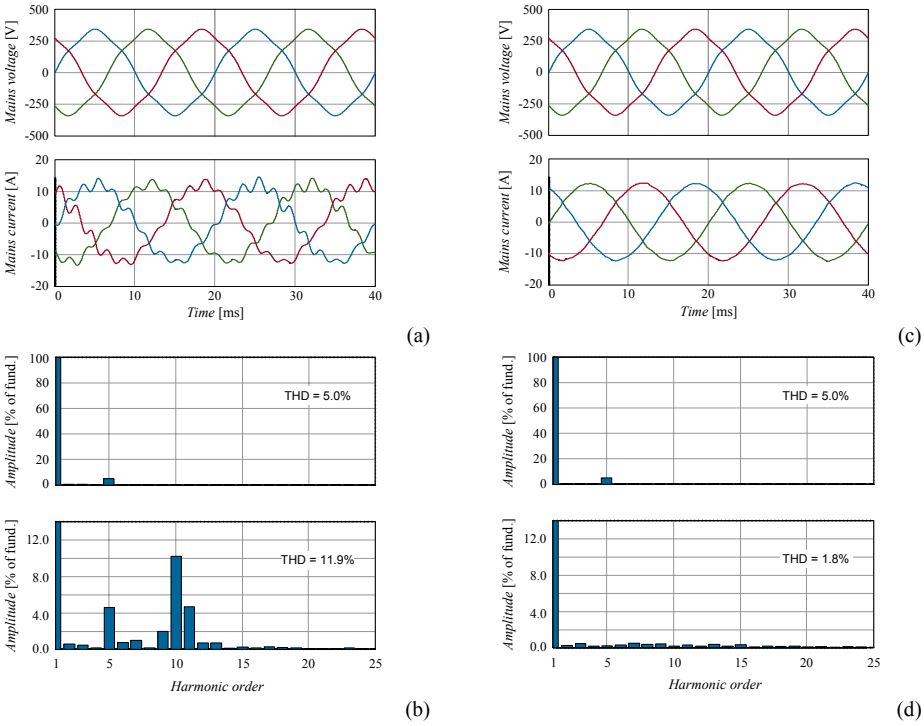

Fig. 14. Simulation results when 5% of the 5th harmonic is superposed the fundamental grid voltage. Grid phase voltage, current and respective harmonic spectrum for the conventional approach (a)-(b) and for the proposed scheme with active damping and harmonic control (c)-(d).

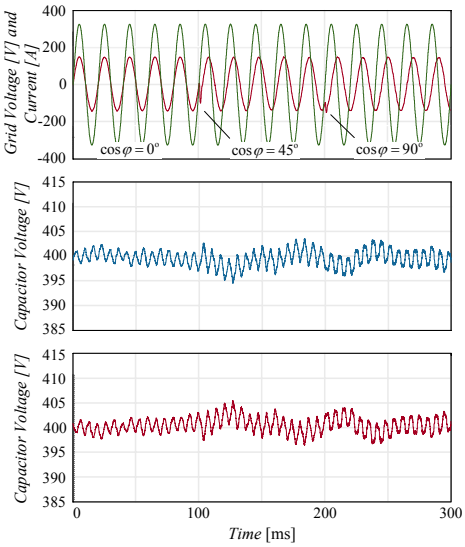

Fig. 15. Dependency analysis of the mid-point voltage with the current phase-shift. The grid current is multiplied by a factor of 10.

VII. Conclusion

An extension of the conventional DPC to be used with a three-level NPC inverter has been presented in this paper. Different hysteresis strategy as well a mid-point potential control are incorporated to the conventional DPC in order to utilize the full advantages of three-level topology. The method is also adapted to be used with a third order LCL filter by adding active damping and harmonic control strategies. Both static and dynamic behaviors were investigated by simulation, as well the efficacy of the mid-point voltage control for different grid voltage and current phase-shift.

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