Five-Level Virtual-Flux Direct Power Control for the Active Neutral-Point Clamped Multilevel Inverter

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***Abstract*—Although multilevel inverters present numerous advantages such as high quality waveform, low switching losses, high voltage capability and low electromagnetic compatibility concerns, some drawbacks are evident. They require a higher number of semiconductors and either multiple isolated dc sources or a bank of series connected capacitors. Consequently, the control complexity increases considerably, since more switching devices normally result in a higher number of possible combinations and the balance of the capacitors has to be guaranteed. But on the other hand, multilevel inverters create an extra degree of freedom due to existing redundant voltage vectors, which produce the same output phase voltage level but with diverse effect on the dc-link and floating capacitors. Among the existing control techniques the Virtual-Flux Direct Power Control (VF-DPC) has showed to be very suitable for grid connected systems since it controls the active and reactive powers directly without any internal current control loop or PWM modulator. However, in order to adapt the VF-DPC for multilevel systems, specifically for the recently proposed five-level Active Neutral-Point Clamped converter, additional features must be included and/or modified in the inner main control loop. In order to allow the controller to select a higher number of available voltage vectors, the active and reactive power hysteresis strategies are modified. Additionally, a method to balance the dc-link and floating capacitor voltages by applying available redundant states is implemented, based on the actual condition of the voltage across the lower dc-link and floating capacitors, as well output phase currents direction. The proposed five-level VF-DPC has been implemented using a $6kW$ five-level prototype and has shown good static and dynamic performance.**

I. Introduction

Important improvements concerning voltage and current ratings have been achieved over the last decade for fast semiconductors like IGBTs. This permits the utilization of these devices in high power and high voltage applications, employing either the conventional two-level topology or the industry standard three-level NPC converter. However, the use of fast switching devices under high voltage may generate high dv/dt to the load. Additionally, the switching losses are increased significantly, reducing the overall efficiency.

In order to bring the stress on the switching components back to acceptable values, a new branch of multilevel converter is quickly emerging, namely five-level topologies. Furthermore, due to the ability of generating a higher number of output voltage levels, this group of multilevel converters can further reduce the voltage and current harmonic contents when compared against three-level topologies.

Traditionally, five-level structures are obtained as natural extension of existing three-level topologies, such as the Neutral-Point Clamped (NPC) [1] and Floating-Capacitors (FC) [2] converters. Additional semiconductors and energy storage elements are included into the classical three-level topologies to produce extra levels. However, both topologies reveal technical difficulties which complicate their application by the industry. A higher number of clamping diodes and flying capacitors is required considering all components with the same voltage rating [3].

Another important aspect to be considered is the complexity to balance the dc-link capacitor voltages of the NPC, and flying capacitors of the FC. In the five-level NPC the dc-link is subdivided into four equal voltage levels by using a split bank with four capacitors instead of only two capacitors as for the three-level approach. The number of flying capacitors is also significantly increased for the five-level converter, demanding a dedicated control technique.

Both difficulties are avoided in the Cascaded H-Bridge multilevel topology, which is characterized by series connection of single-phase H-bridge converters. However, the use of this strategy is limited in some applications due to the necessity of isolated dc power sources.

Recently, a new multilevel topology has been introduced [4] to overcome some of the above mentioned limitations while achieving all the advantages of multilevel converters. The five-level active neutral-point clamped (ANPC) inverter combines characteristics of the neutral-point clamped and floating-capacitor inverters.

However, at the same time the five-level ANPC inverter brings numerous benefits, it also demands especial and dedicated control strategies. If the balance of the capacitor voltages are not guaranteed, a group of switching devices experience a higher voltage applied across their terminals and extra distortion may occurs in the load voltages and currents. Additionally, the controller shall allow the inverter to switch between different voltage levels in order to take advantage of the higher number of voltage vectors available in a five-level structure. Therefore, existing control techniques, namely voltage oriented control, hysteresis, direct

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power control, etc., have to be adapted in order to fulfill these requirements.

Among these control methods the Direct Power Control (DPC) has become more widely used over the last few years in grid connected systems due to the advantage of controlling the active and reactive powers directly without any internal current control loop or PWM modulator. It has been originally presented and analyzed for the conventional two-level inverter [5] [6] [7]. Later on, a natural extension of the DPC for the three-level NPC inverter was proposed [8] by modifying the classical two-level hysteresis voltage vector decision block and by including a strategy for choosing an appropriate redundant voltage vector for balancing the dc-link capacitor voltages.

This paper proposes a five-level Virtual-Flux Direct Power Control scheme to be used with the Active Neutral-Point Clamped inverter. The concept maintain the same main idea of controlling the active and reactive powers directly through hysteresis comparators and a switching table, however additional blocks are included to balance the voltage across the dc-link and floating capacitors. In addition, the hysteresis method is adapted to allow the inverter to switch between multiples voltage levels.

II. Five-Level Active Neutral-Point Clamped

The active neutral-point clamped (ANPC) inverter presented by one-phase leg in Fig. 1 produces five distinct output voltage levels by combining the three-level characteristic of the input stage (*Cell 1*) with the two-level of the output parts (*Cell 2* and *Cell 3*). Moreover, unlike classical five-level topologies, the ANPC inverter splits the dc-link into only two capacitors and requires only a single floating capacitor for each phase. Consequently, it reduces costs, volume and control complexity.

Five output voltage levels are achieved from eight distinct switching combinations, indicated by the combination of the switching functions of S_1, S_3 and S_5 in Table I. One can note that the switches S_5 and S_7 are operated in the same way and complementarily to S_6 and S_8.

The list of switching combinations also shows the presence of redundant states, which generate the same output voltage level referred to the dc-link mid-point M. The voltage level $-\frac{u_{dc}}{4}$ is generated either by the switching state u_2 or u_3. Nevertheless, they cause an opposite effect on the floating capacitor voltage, due to the different combination of the switches. For a positive output phase current for example, while state u_2 discharges, u_3 charges de floating capacitor.

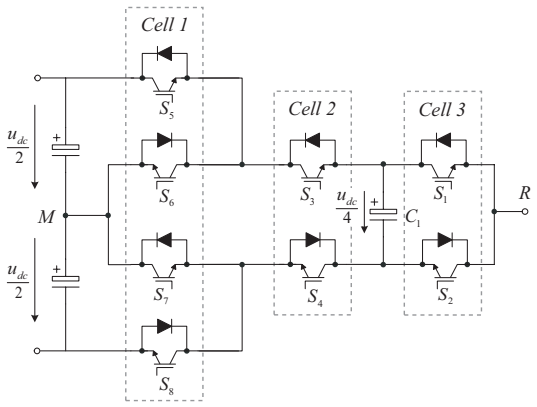


Fig. 1: One phase-leg of a five-level active-neutral point converter.

TABLE I: 5-Level ANPC Inverter Output Voltage Levels and Respective Switching States

Cell 1				*Cell 2*		*Cell 3*		Phase Voltage	Switching State
S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1		
1	0	1	0	1	0	1	0	$-\frac{u_{dc}}{2}$	u_1
1	0	1	0	1	0	0	1	$-\frac{u_{dc}}{4}$	u_2
1	0	1	0	0	1	1	0	$-\frac{u_{dc}}{4}$	u_3
1	0	1	0	0	1	0	1	0	u_4
0	1	0	1	1	0	1	0	0	u_5
0	1	0	1	1	0	0	1	$\frac{u_{dc}}{4}$	u_6
0	1	0	1	0	1	1	0	$\frac{u_{dc}}{4}$	u_7
0	1	0	1	0	1	0	1	$\frac{u_{dc}}{2}$	u_8

A similar behavior is observed on the level $\frac{u_{dc}}{4}$ produced by the states u_6 and u_7. Depending on the direction of the output phase current, these states have the ability to charge or discharge the floating capacitor.

Besides that, the redundant combinations have also different impact on the mid-point potential, depending on the switching state of the input stage. For building an output voltage equal to $-\frac{u_{dc}}{4}$, the input stage can be connected either to the negative potential $-\frac{u_{dc}}{4}$ (u_2) or directly to M (u_3). For the voltage level equal to $\frac{u_{dc}}{4}$, the switching state u_6 results in mid-point current flow, while u_7 is connected to the positive potential.

Therefore, this analysis clearly shows a degree of freedom to balance the floating capacitor of each phase individually by properly selecting the switching states according to the direction of the output current and the state of the floating capacitor voltage. The influence of each phase on the mid-point potential can also be regulated using redundant states to create or avoid a link between the output and M.

For a three-phase system, this flexibility of controlling the output, mid-point and floating-capacitor voltages raises considerably, but on the other hand the complexity increases proportionally. The number of vectors increases from 18 of the three-level structure to 61 available for the five-level topology. Furthermore, due to the presence of redundant vectors, the number of switching states raises to 125 possibilities as shown in the space vector diagram of Fig. 2. To generate the zero voltage vector U_0, for example, there are five distinct vectors and for the vectors U_1 to U_6 there exist four possibilities. The vectors are labeled according to the voltage level of each phase (R S T) where the output voltage levels $-\frac{u_{dc}}{2}$, $-\frac{u_{dc}}{4}$, 0, $\frac{u_{dc}}{4}$ and $\frac{u_{dc}}{2}$ are numbered from -2 to 2, respectively.

In the specific case of the five-level ANPC, the number of possible states is further increased to 343, due to redundant states for the levels -1 $\left(\frac{u_{dc}}{4}\right)$, 0 and 1 $\left(\frac{u_{dc}}{4}\right)$ as described in Table I. The voltage vector U_{19}, for example, traditionally consisting of two redundant vectors (2 -1 -1) and (1 -2 -2) is extended to six distinct states (Table II) concerning mid-point and floating-capacitor balancing capability. The sequence $-1-1$ in the first redundant vector (2 -1 -1) can be realized with four different combinations of the states u_2 and

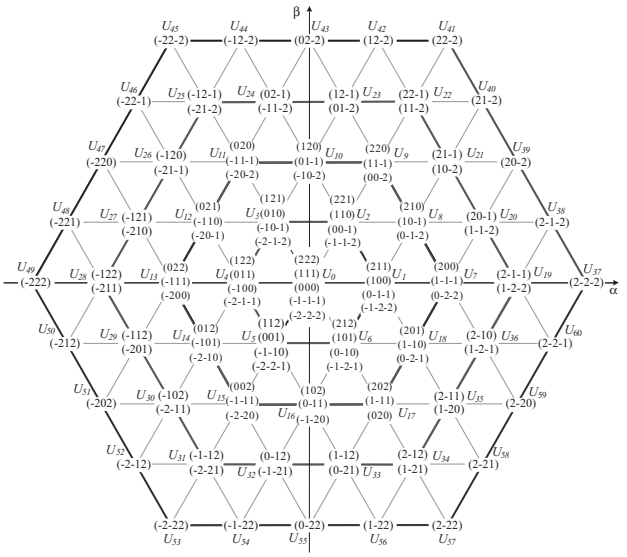


Fig. 2: Five-level space vector diagram.

u_3, and the level 1 in the second redundant vector (1 -2 -2) with the states u_6 and u_7. Hence, multiple combinations for effecting the floating-capacitor and mid-point potential can be achieved while applying the same line-to-line voltage.

TABLEII: VOLTAGE VECTORψ $U19$ - SWITCHING STATES

				State		
				R	S	T
U_{19}	2	-1	-1	u_8	u_2	u_2
	2	-1	-1	u_8	u_2	u_3
	2	-1	-1	u_8	u_3	u_2
	2	-1	-1	u_8	u_3	u_3
	1	-2	-2	u_6	u_1	u_1
	1	-2	-2	u_7	u_1	u_1

Nevertheless, in order to take advantage of all this flexibility, the controller needs to find a proper combination of switching states and/or voltage vectors to regulate the instantaneous active and reactive power and switching states to balance the mid-point potential and floating-capacitor voltages.

Therefore, some concepts previously developed for the conventional two-level VF-Direct Power Control have to be reviewed and at the same time new strategies introduced.

III. 5-LEVEL VIRTUAL-FLUX DIRECT POWER CONTROL

The basic concept of choosing a switching state via a switching table according to the error between the actual and desired active and reactive power references is maintained on the proposed five-level VF-DPC illustrated in Fig. 3. However, to permit more flexibility in the vector selection, the single band hysteresis employed on the conventional two-level VF-DPC is replaced by a four bands strategy and to achieve a proper mid-point and floating capacitor balancing, a method to decide on the correct redundant switching state is employed. Depending on the space vector selected by the switching table, the voltage balance strategy will choose the proper state according to the mid-point and floating capacitor voltages deviation and load current direction. Additionally, to improve the accuracy of selecting a correct voltage vector, the space vector plane is divided into 24 sectors instead of 12 used previously.

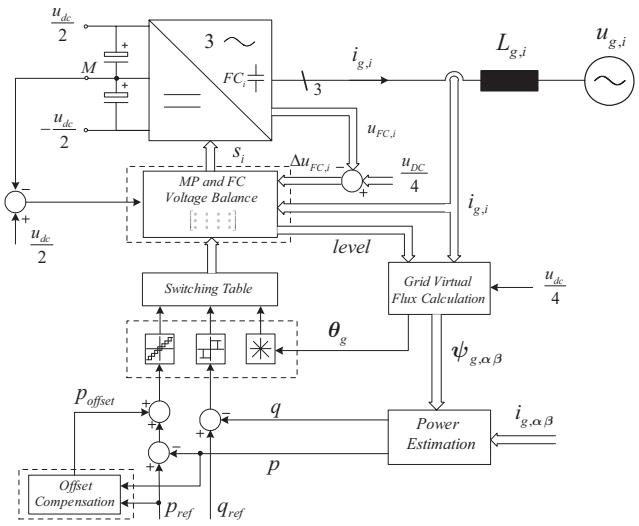


Fig. 3: Virtual-Flux Direct Power Control for the five-level ANPC inverter.

A. Sector Decision

For five-level systems, vectors existing in an $\frac{\pi}{6}$-wide interval may result in considerable distinct effects on the instantaneous active and reactive power. The vector which would be the best choice for the first $\frac{\pi}{12}$ of a $\frac{\pi}{6}$-sector, might not be optimum for the second $\frac{\pi}{12}$ half when considering voltage vectors of highest magnitude (S_{37} to S_{60}).

A more precise voltage selection is achieved by splitting the space vector plane into 24 sectors of $\frac{\pi}{12}$ each, starting with *Sector 1* in an interval $\left(-\frac{2\pi}{3}, -\frac{7\pi}{12}\right]$, as illustrated in Fig. 4. The consecutive sectors are allocated sequentially in counterclockwise direction according to

$$(n-9)\frac{\pi}{12} \leq \text{sector n} < (n-8)\frac{\pi}{12} \quad \text{where } n = 1, 2, \ldots 24. \tag{1}$$

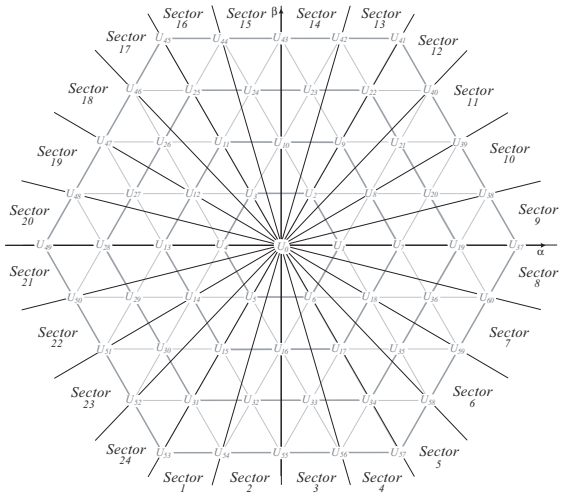


Fig. 4: $\alpha\beta$ plane divided into 24 sectors.

B. Vector Selection

A higher number of levels available amplifies the flexibility of choosing an optimum voltage vector, and consequently a more precise control of both active and reactive powers can be obtained. However, the complexity is further increased.

The strategy to select an appropriate voltage vector for the five-level ANPC is a natural extension of the method employed with the two-level approach. The basic concept of adjusting the angle between inverter and grid virtual-flux vectors to regulate the active power, and the magnitude of the inverter virtual-flux vector to control the reactive power (Fig. 5) is again utilized. However, three extra voltage levels existing in the space vector plane increase the degree of freedom to control both variables, especially the active power.

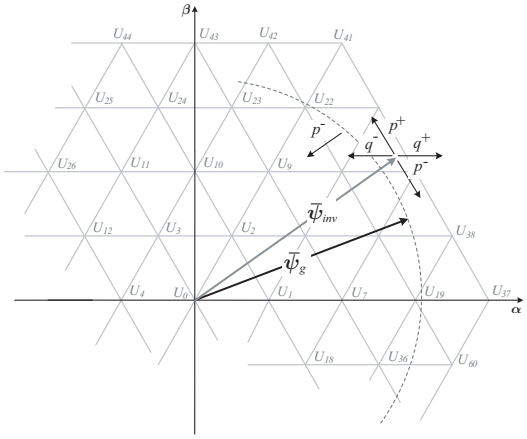


Fig. 5: Influence of the voltage vectors on the instantaneous active and reactive powers.

To take advantage of this fact, the hysteresis strategy is modified (Fig. 6) by adding three extra boundaries (u_{p2}, u_{p3} and u_{p4}) to the one used for the two-level method. Each level of the hysteresis control (u_{p1} to u_{p4}) is directly referred to one level of the space vector plane (inner to outer hexagons).

According to the position of the grid voltage vector (or virtual-flux vector) and the inverter operating point, the active power error is maintained within two consecutive boundaries, allowing to select only neighboring vectors. Assuming the grid voltage vector rotating between the two outer hexagons, depending to the inverter modulation index,

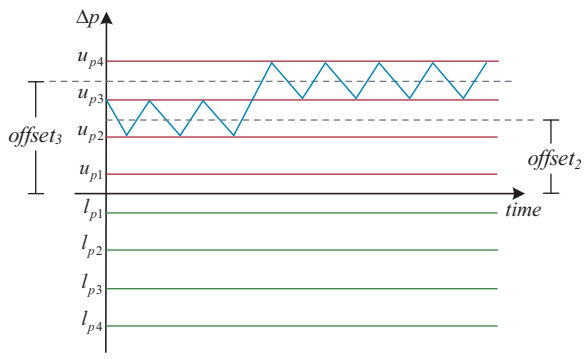


Fig. 6: Active power hysteresis strategy used by VF-DPC for the five-level ANPC inverter.

Δp might be conserved e.g. within two outer hysteresis boundaries (u_{p3} and u_{p4}). When the error reaches the upper limit (u_{p4}) an appropriate vector of the outer hexagon (U_{37} to U_{60}) is selected to increase the instantaneous active power, reversing the direction of Δp. When the active power error crosses u_{p3}, a voltage vector of the next inner level (U_{19} to U_{36}) is chosen to reduce the instantaneous active power. These decisions are evidently also dependent on the state of the sector decision block and the reactive power requirement.

To correct the undesirable offset produced by the active power hysteresis strategy, a feedforward offset compensation block is added to the active power reference as shown in the Fig. 3. The magnitude of the offset to be compensated (e.g. $offset_2$ and $offset_3$ in Fig. 6) is dependent on the inverter operating point. The controller verifies the actual position of Δp based on the inverter modulation index and injects a constant value proportional to the respective hysteresis limits u_{pi}, according to

$$p_{pre} = u_{pi} + \frac{u_{pi+1} - u_{pi}}{2} \qquad \text{where } i = 1, 2, 3. \tag{2}$$

In terms of reactive power control, a good performance which limits ΔU by selecting only neighbor vectors is achieved when a single band hysteresis with zero cross detection method is used (Fig. 7). The zero detection is applied to select an intermediate vector which does not cause a big influence on the reactive power however, creates a link between two another vectors without resulting in a high ΔU.

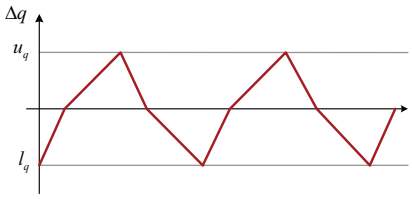


Fig. 7: Reactive power hysteresis strategy.

C. Mid-Point and Floating Capacitors Balance

Despite the traditional necessity of balancing the mid-point potential in multilevel inverters, the five-level ANPC demands extra control effort to regulate the voltage of the floating capacitors. However, the number of redundant vectors is significantly increased and additional redundant states are created for phase voltage levels $-\frac{u_{dc}}{4}$ (-1), 0 and $\frac{u_{dc}}{4}$ (1). These redundant vectors and states are characterized by applying the same line-to-line voltages while affecting differently the mid-point and floating capacitor voltages.

An example of the influence of redundant vectors and states on the mid-point and floating capacitor voltage is given in Table III for the voltage vector U_{19}.

One can note that due to the existence of two redundant states (u_2 and u_3) for level -1 and another two states (u_6 and u_7) for level 1, the two redundant voltage vectors (2 -1 -1) and (1 -2 -2) can be generated using six distinct switching states. Each state results in a different combination of mid-point and floating capacitor currents.

In terms of mid-point current, there exist four possibilities to influence the mid-point potential as function of the output

TABLEIII: REDUNDANT SWITCHING STATES OF VOLTAGE VECTOR U19 AND RESULTING i_M AND $i_{FC,RST}$ (POSITIVE i_M REPRESENTS CURRENT FLOWING OUT OF M AND POSITIVE $i_{FC,i}$, CURRENT CHARGING THE FLOATING CAPACITOR).

	Vector			States			i_M	$i_{FC,R}$	$i_{FC,S}$	$i_{FC,T}$
				R	*S*	*T*				
U_{19}	2	-1	-1	u_8	u_2	u_2	0	0	-i_S	-i_T
	2	-1	-1	u_8	u_2	u_3	i_T	0	-i_S	i_T
	2	-1	-1	u_8	u_3	u_2	i_S	0	i_S	-i_T
	2	-1	-1	u_8	u_3	u_3	-i_R	0	i_S	i_T
	1	-2	-2	u_6	u_1	u_1	i_R	-i_R	0	0
	1	-2	-2	u_7	u_1	u_1	0	i_R	0	0

phase currents. Moreover, there are two alternatives for each phase to charge or discharge the respective floating capacitor. Therefore, a degree of freedom exists to select the appropriate switching state to regulate the voltage of mid-point and the voltages of the floating capacitors.

Nevertheless, although there is a wide diversity of switching states, not all necessities might be covered. If for example, for vector U_{19} the floating capacitors of phases S and T need to be charged and the lower dc-link capacitor discharged, despite the last combination (u_7 u_1 u_1) which does not cause any influence on these variables, the remaining states would increase the deviation in at least one capacitor voltage. Therefore, in order to achieve a wider control range, hysteresis limits are used on the mid-point and floating capacitor voltage deviations. Instead of requesting a change of the switching state each time the voltage of a control variable is higher or lower then the respective reference, the hysteresis provides some flexibility for controlling a variable while the remaining variables do not cross any boundary.

The mid-point and floating capacitor control block presented in Fig. 8 is basically divided into two parts. The first block performs the selection of an appropriate voltage vector from the switching table to control instantaneous active and reactive powers. Out of this vector, the second block extracts from a table the correct switching state to balance the mid-point and the floating capacitors based on the conditions of the lower dc-link capacitor (u_{C_l}), floating capacitors ($u_{FC,RST}$) and the direction of output phase currents ($i_{inv,RST}$).

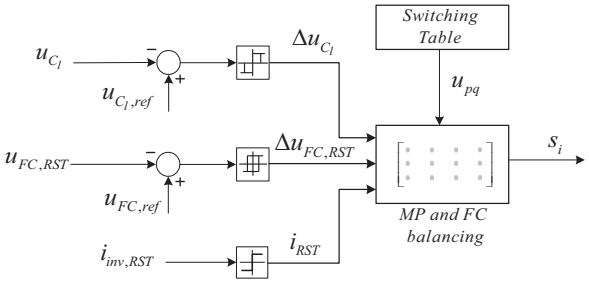


Fig. 8: Mid-point and floating capacitors balance strategy.

A hysteresis with zero crossing detection is used to allow a voltage ripple on the dc-link capacitor. When the error of the dc-link voltage reaches the upper boundary, the hysteresis output changes to 1 which indicates that the lower capacitor should be charged. If the error is below the lower limit, an output equal to -1 informs that the lower capacitor has to be discharged. When the error crosses the zero line, a digit 0 informs the controller that either a state which charges or discharges the lower dc-link capacitor may be applied. This gives sufficient margin for controlling the floating capacitors also for a voltage vector with reduced number of states. For the floating capacitors, classical hysteresis controls are employed, providing 1 if the error reaches the upper band and -1 for the lower band. Additionally, the directions of the output phase currents are measured, giving 1 for positive and 0 for negative current.

This information is to select from a predefined table the correct switching state with respect to the power condition established by the switching table and allows to regulate the mid-point potential and the voltage of the floating capacitors.

IV. EXPERIMENTAL VERIFICATION

The performance of the proposed VF-DPC to be used with the five-level ANPC inverter is verified through experimentation. The $6kW$ ANPC inverter (Fig. 9) supplied by two 10kW dc power sources connected in series to obtain 800V is connected via a $10mH$ L filter to a controlled $400V$, $50Hz$, 3-phase AC power source. The average switching frequency is adjusted to $2.5kHz$ to emulate high power systems. The VF-DPC control is implemented digitally using an Analog Devices ADSP21991 16-bit $160MHz$ DSP. In a control loop with $90kHz$ sampling frequency two output p hases are measured using the internal 14-bit ADC. During the conversion time of $725ns$, the grid virtual-flux is calculated based on the actual switching state and measured voltage across the lower dc-link capacitor. At the same sampling rate, the algorithm estimates the instantaneous active and reactive power and compares the actual power values with the references to select an optimum voltage vector from the switching table. The three floating capacitor voltages are measured using three channels of the internal ADC and are compared to the desired values. The errors are used together with the current directions and the dc-link voltage status to select the correct switching state from one of the original vectors table.

An accurate estimation of the grid-virtual fluxes $\psi_{g,\alpha\beta}$ in terms of magnitude and phase is fundamental to correctly

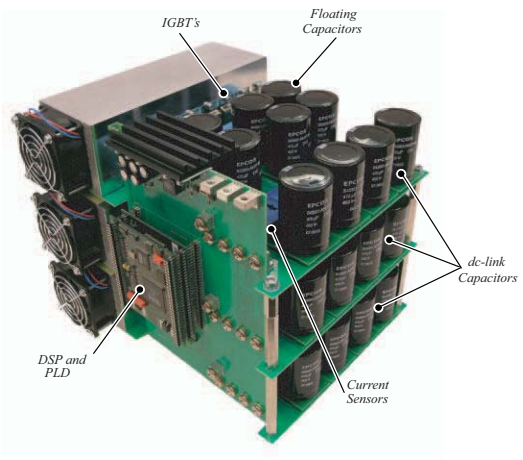


Fig. 9: Photo of the three-phase five-level ANPC prototype.

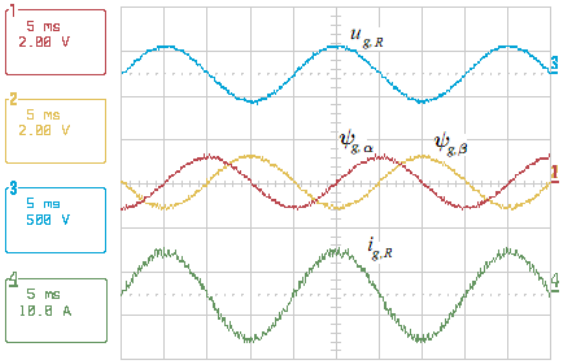


Fig. 10: Experimental analysis of the five-level VF-DPC concerning grid phase voltage $u_{g,R}$, virtual-flux $\psi_{g,\alpha\beta}$ and phase current $i_{g,R}$.

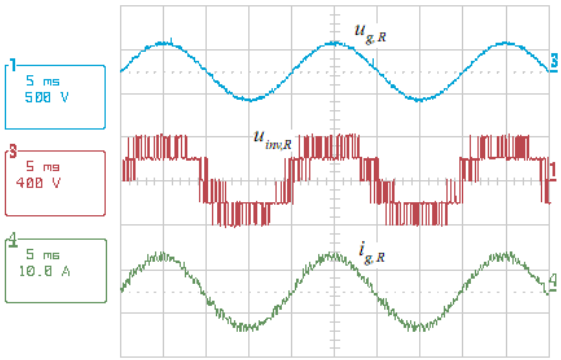


Fig. 12: Experimental results of the inverter output voltage $u_{inv,R}$ refereed to the dc-link mid-point M, phase voltage $u_{g,R}$ and resulting grid phase current $i_{g,R}$.

generate the desired phase current $i_{g,R}$ as shown in Fig. 10. Furthermore, the grid virtual-flux has important influence on the correct estimation of the instantaneous active p and reactive q powers, which are the control variables used by the VF-DPC. In Fig. 11 the active power is set to the rated value $6kW$ and the reactive to 0 in order to obtain the load current $i_{g,R}$ in phase to the grid voltage $u_{g,R}$.

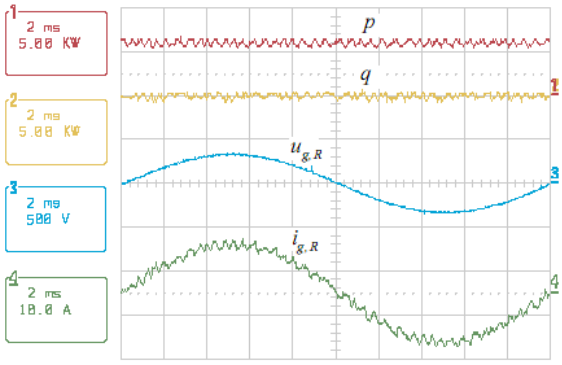


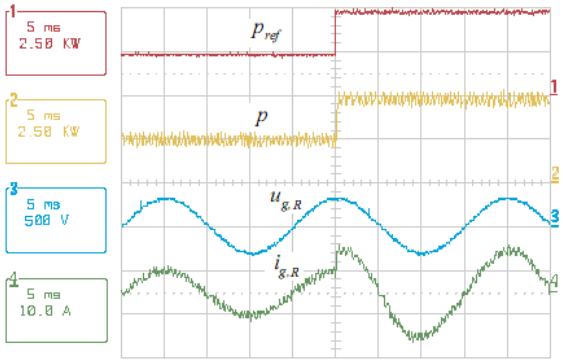
Fig. 11: Experimental analysis of the five-level VF-DPC showing instantaneous active p, reactive q powers, grid phase voltage $u_{g,R}$, and phase current $i_{g,R}$.

The hysteresis strategy and the switching table build the core of the direct power control technique. For multilevel systems, these blocks are significantly modified in order to allow the inverter two switch between n levels. For the five-level ANPC, a hysteresis method with four levels is used to generate five distinct output voltage levels $u_{inv,R}$ referred to the dc-link mid-point M as shown in Fig. 12. Additionally, the switching table and the hysteresis control have to work in synchronism to switch only between consecutive levels, reducing Δu.

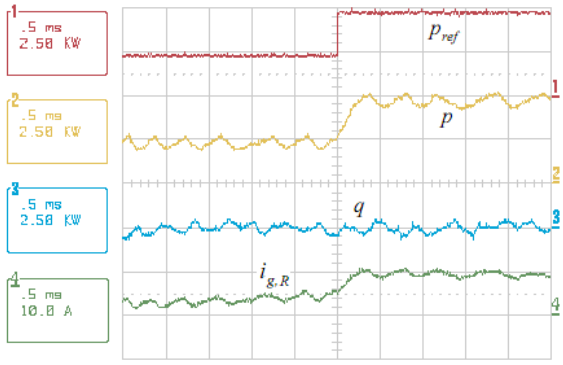
The dynamic response has also been experimentally tested, in order to prove that although some blocks of the classic VF-DPC have been adapted to operate with five-level system, the fast transient response is not affected. A step of the active power reference p_{ref} from 40% to 80% of the rated value is shown in Fig. 13. The grid current and consequently the estimated active power almost immediately follows the change on the reference. A closer look at the rise time (Fig. 13(b)) shows the instantaneous active power reaching the new reference value in approximately $400\mu s$. Moreover, the reactive power is practically not affected by the change of the active power.

Good static and dynamic performances showed by the experimental results are only possible with the five-level ANPC if the dc-link and floating capacitors are correctly balanced. Otherwise, any unbalance in one of these capacitors besides creating undesirable harmonics in the output current, results in an excessive high voltage applied to a group of switching devices.

The proposed VF-DPC regulates the voltage across the lower dc-link capacitor u_{C_l} (and consequently the upper capacitor u_{C_u}) to half of the total dc-link voltage $400V$ (Fig. 14), by properly manipulating existing redundant voltage vectors and switching states. Additional tables con-



(a) Time scale - 5ms



(b) Time scale - $500\mu s$

Fig. 13: Experimental results of a positive step of 40% in the active power reference presented in (a) 5 ms time scale and (b) $500\mu s$ time scale. Active power reference p_{ref}, actual active power p, grid phase voltage $u_{g,R}$ and current $i_{g,R}$.

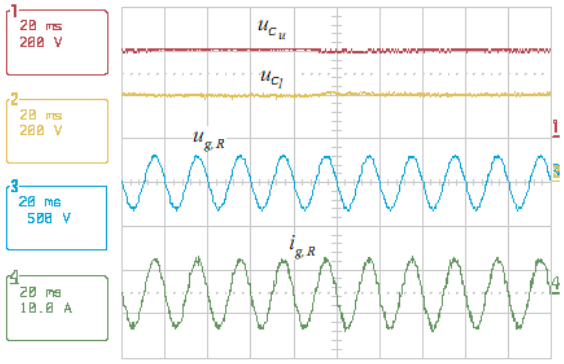


Fig. 14: Experimental results of the voltage across the upper u_{C_u} and lower u_{C_l} dc-link capacitors.

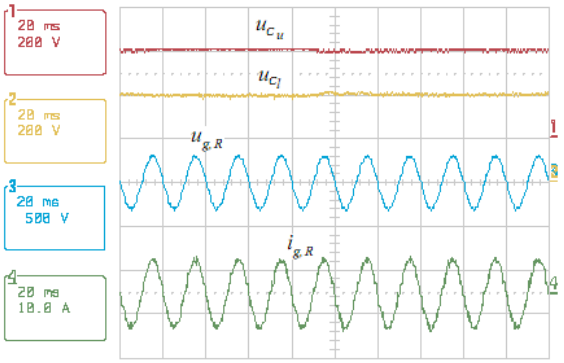


Fig. 15: Experimental results of the voltage across the floating capacitors.

taining the switching states organized according to their ability to charge or discharge the capacitors assist to find the optimum state. The deviation of the lower dc-link capacitor voltage is measured and a hysteresis control defines the next step of the dc-link controller.

The regulation of the floating capacitors is achieved as an extension of the dc-link voltage control method. Besides the deviation of the dc-link capacitors, the control analyzes the states of the floating capacitor of the three phases to decide on the next switching state. By selecting the correct redundant switching state the voltages of the three floating capacitors are controlled to $\frac{u_{dc}}{4}$ $(200V)$ as shown in Fig. 15.

V. Conclusion

At the same time the five-level ANPC demands complex technique to control its variables, it provides extra degree of freedom to the controller due to higher number of switching possibilities. Five distinct voltage levels may be generated by applying eight switching combinations, therefore it is clear the existence of redundant states. However, to take advantage of this flexibility the classical current controllers have to be properly adapted. The VF-DPC previously presented for two-level systems and later extended to be used with the industry standard three-level NPC requires additional modifications, mainly on the voltage vector decision block. Extra levels have to be added to the active power hysteresis control to allow the controller to switch among five voltage levels. To increase the accuracy of the vector decision, the space vector plane is divided into 24 sectors instead of 12 of the classical approach. Additionally, the five-level VF-DPC must be able to regulate the voltage across the dc-link and floating capacitors. This demands a dedicated strategy to select the correct switching state based on the status of the dc-link and floating capacitors as well as the direction of the output phase currents. The static and dynamic performance of the proposed five-level VF-DPC has been experimentally verified using a $6kW$ five-level ANPC inverter prototype connected to a 400V 3-phase AC power source via a first order L filter.

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