Design and Experimental Verification of a Novel 1.2kW 480V_{AC}/24V_{DC} Two-Switch Three-Phase DCM Flyback-Type Unity Power Factor Rectifier

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Abstract-The basic principle of operation of a novel three-phase two-switch unity power factor flyback rectifier is analyzed and a system control concept is proposed. The stresses on the power components are calculated in an analytical form and used for designing a converter with an input voltage range of 480V±10% and 24V/50A DC output. The theoretical considerations are verified by an experimental analysis of a laboratory prototype of the system.

I. INTRODUCTION

The extending automation of manufacturing processes results in a rising power demand of industrial control systems. Thereby, typical output voltage/current values of switched-mode power supplies supplying the control electronics are 24V/30A or 24V/50A. The power supplies in most cases are connected to the 400V or 480V three-phase mains. As compared to a single-phase supply this does allow to reduce the effort for smoothing of the output voltage of the rectifier input stage of the power supplies and does provide a redundancy in case of a mains phase loss.

For installation of the power supplies in switchboards and distributed junction boxes low power losses and/or a high efficiency η>90% as well as a compact design exceeding a power density (including the heatsink) of $\rho > 200W/dm^3$ ($3W/in^3$) for natural convection are required. A topology being employed for the realization of such systems is, e.g., the two transistor flyback converter shown in **Fig.1**(a). There, in contrast to a forward converter only one single inductive component has to be provided, i.e., the current limiting inductor and the transformer are integrated in a single magnetic device and the maximum blocking voltage stress is limited by the amplitude of the mains line-to-line voltage what results in relatively low overall realization effort.

Keeping in mind the more stringent regulations concerning the effects on the mains in the course of the development of a new generation of control system power supplies one now has to pose the question if besides increasing the output power a power factor correction could be incorporated into the system without a main degradation of the efficiency and power density. There, due to the relatively low output power single-stage topologies are of special interest which show a complexity comparable to conventional systems. (The output voltage ripple with twice the mains frequency occurring for single-stage power conversion in case of an asymmetric mains and/or failure of a mains phase is not critical for control electronics power supplies because of the high allowable output voltage ripple of typically <2%).

In [1] a three-phase single-switch discontinuous conduction mode (DCM) AC/DC flyback converter has been propose which does show a sinusoidal shape of the input current for constant duty cycle of the power transistor over the mains period, i.e. shows a very low complexity of power and control circuit. However, due to the relatively high blocking voltage stress of the switch the concept is not applicable in the case at hand. As shown in [2], the maximum transistor blocking voltage can be reduced to values lower than twice the mains phase voltage amplitude in case two switches are employed ([3], cf. Fig.1(b)) which are connected to an artificial mains neutral point *N'*, i.e. the neutral point of the star connection of the input filter capacitors C_F . Accordingly, the realization of power transistors S_+ and S_- could be by power MOSFETs with 1000V blocking capability also for application of the system in a 480V mains what does make the concept applicable for the realization of a power supply for industrial control systems.

In **section 2** of this paper the basic function of the three-phase two-switch unity power factor flyback converter is analyzed. In **section 3** the stresses on the power components are calculated in an analytical form. The system control is treated in **section 4** There, in addition to the output voltage control loop a control loop limiting the average value of the output current and/or the maximum output power and a control loop suppressing the occurrence of zero sequence components of the input capacitor voltages is provided. In **section 5** experimental results gained from a laboratory prototype of the system are shown.

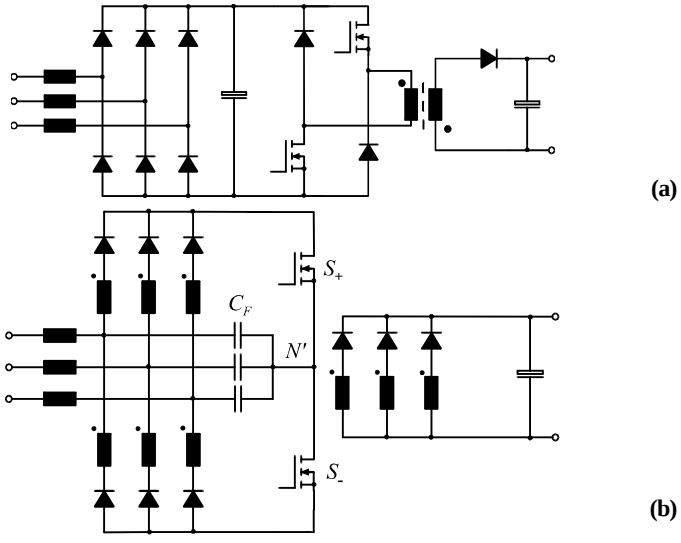


Fig.1: Converter topologies for the power supply of industrial automation systems from the three-phase mains; **(a)**: conventional two-stage two-switch flyback converter, **(b)**: proposed three-phase two-switch unity power factor DCM flyback converter [3].

II. PRINCIPLE OF OPERATION

For equal potentials of the artificial neutral point *N'* and of the actual mains neutral point *N*, the system behavior is identical to three independent single-phase flyback converters. For a positive filter capacitor phase voltage $u_{U,i}>0$ ($i=R,S,T$) the primary partial winding $N_{1+,i}$ and for negative filter capacitor phase voltages $u_{U,i}<0$ the primary partial winding $N_{1-,i}$ is active. The system shows a relatively low realization effort and/or relatively high silicon utilization [4] as compared to a three-phase arrangement of three individual single-phase units [5] because the power transistors S_+ and S_- are shared by all three phases and because only two diodes have to be provided per phase on the primary.

For constant duty cycle δ and operation of the system in discontinuous conduction mode (DCM) the primary current shows a triangular shape within each pulse period T_P. There the local peak value is defined by

$$\hat{i}_{U,i} = \frac{T_P \cdot \delta^2}{2L} \cdot u_{U,i} \qquad (1)$$

($\delta = \delta_+ = \delta_-$, $i_{U,i}=i_{U,i+}$ for $u_{U,i}>0$, $i_{U,i}=i_{U,i-}$ for $u_{U,i}<0$). Accordingly, the mains phase currents $i_{N,i}$ which result after low-pass filtering of the primary currents (cf. $L_F C_F$ in **Fig.2**) which corresponds to a local averaging of $i_{U,i+}$ and/or $i_{U,i-}$ will show an input voltage proportional shape (automatic resistive behavior, [6]).

The rectifier system therefore behaves like a symmetric ohmic load, i.e. for equal duty cycles $\delta_+ = \delta_- = \delta$ the artificial neutral point *N'* and the actual mains neutral point *N* will show equal potentials. However, a difference between the effective duty cycles δ_+ and δ_- (as caused e.g. by different delay times of the gate drive circuits or different switching times of the power transistors S_+ and S_-) or a high ripple of the capacitor voltage would result in low frequency component of the potential of *N'* with reference to *N*. This in turn would increase the blocking voltage stress on the power transistors S_+ and S_-. Therefore, one has to provide an active control of the potential of *N'* (cf. Fig.6). Furthermore, a proper safety margin should be considered for the dimensioning of the power transistors concerning the blocking capability.

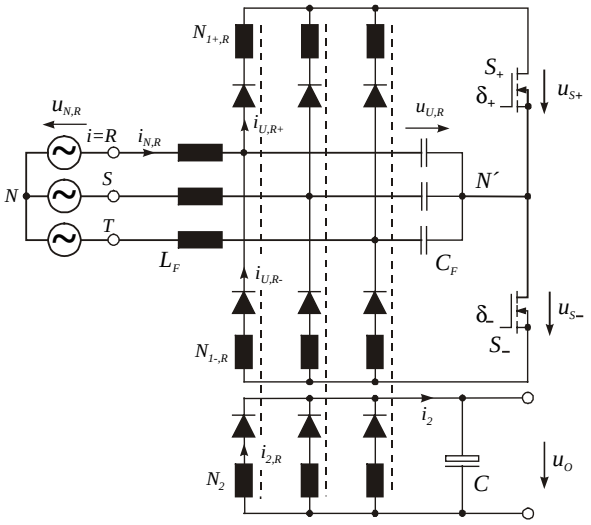


Fig.2: Basic structure of the power circuit of a three-phase two-switch discontinuous conduction mode flyback unity power factor rectifier.

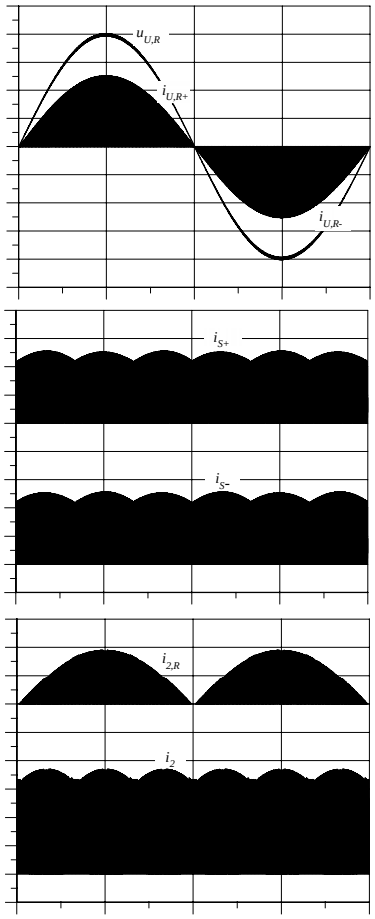


Fig.3: Time behavior of the primary partial input phase currents $i_{U,R+}$ and $i_{U,R-}$ and of the corresponding filter capacitor voltage $u_{U,R}$ (cf. **(a)**, 5A/div, 100V/div) of the currents i_{S+} and i_{S-} in the power transistors S_+ and S_- (cf. **(b)**, 5A/div), of an output phase current $i_{2,R}$ and of the total output current i_2 (cf. **(c)**, 75A/div). Simulation parameters: U_N=282V, U_O=24V, P_O=1.2kW, f_P=30kHz.

Results of a simulation of the time behavior of characteristic primary and secondary side currents within a mains period using CASPOC [7] are compiled in **Fig.3.**

III. SYSTEM DESIGN AND STRESSES OF THE COMPONENTS

A. Dimensioning of the Components

For the dimensioning of the phase transformers the following criteria have to be considered.

1) Transfer of the rated power: The rated system input power can be calculated by

$$P_I = \frac{P_O}{\eta} = \frac{L}{2} \cdot \sum_i \hat{I}_{U,i}^2(t) \cdot f_P = \frac{3}{4} \hat{I}_U^2 \cdot L \cdot f_P \,. \qquad (2)$$

Equation (2) shows that the primary inductance *L* has to be chosen as large as possible in order to minimize the peak value of the input currents $\hat{I}_U$ and/or switch stress and the input filter size.

2) Blocking Voltage Stress on S_+ and S_- : Considering the maximum blocking capability (1000V) of the power MOSFETs and a margin for overvoltage protection of 200V, the blocking

TABLE I:
CALCULATION OF THE CURRENT STRESS OF THE POWER COMPONENTS

Component	**Primary Diodes**	**Secondary Diodes**	**Switches**	**Transformer**		**Output Cap.**	**Filter Cap.**
Value	I_{Dp}	I_{Ds}	I_S	I_{N1}	I_{N2}	I_C	I_{CF}
AVG	$I_N \cdot \frac{\sqrt{2}}{\pi}$	$\frac{P_O}{3 \cdot U_O}$	$I_N \cdot \frac{3\sqrt{2}}{\pi}$	$I_N \cdot \frac{\sqrt{2}}{\pi}$	$\frac{P_O}{3 \cdot U_O}$		
RMS	$\sqrt{\frac{2}{3\delta_N}} \cdot I_N$	$\sqrt{\frac{32 \cdot L \cdot f_P \cdot N_1}{9\pi \cdot \delta_N^3 \cdot U_O \cdot N_2} \cdot \left(\sqrt{2} \cdot I_N\right)^3}$	$I_N \cdot \sqrt{\frac{4}{\delta_N} \cdot \left(\frac{1}{3} + \frac{\sqrt{3}}{2\pi}\right)}$	$\sqrt{\frac{2}{3\delta_N}} \cdot I_N$	$\sqrt{\frac{32 \cdot L \cdot f_P \cdot N_1}{9\pi \cdot \delta_N^3 \cdot U_O \cdot N_2} \cdot \left(\sqrt{2} \cdot I_N\right)^3}$	$I_O \cdot \sqrt{\left(\frac{\sqrt{2} \cdot \delta_N \cdot U'_O}{3 \cdot I_N \cdot L \cdot f_P} - 1\right)}$	$I_N \cdot \sqrt{\frac{4}{3\delta_N} - 1}$

voltage stress on the switches S_+ and S_- should be limited advantageously to

$$U_{S,\max} = \hat{U}_N + U_O' = 800\text{V} . \quad (3)$$

Accordingly, the voltage occurring across the transformer primary during demagnetization has to be limited to

$$U'_O = \frac{N_1}{N_2} \cdot U_O \le U_{S,\max} - \hat{U}_N \quad (4)$$

($N_1=N_{1+}=N_{1-}$) by proper selection of the transformer turns ratio.

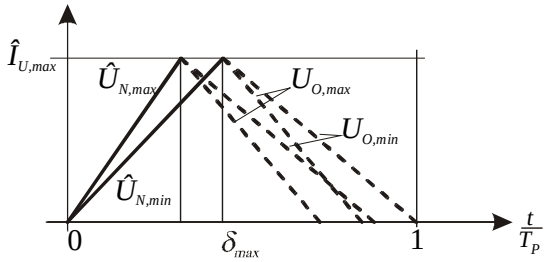


Fig.4: Magnetization of a phase transformer.

3) System Operation in discontinuous conduction mode (DCM): In order to ensure a complete demagnetization of the phase transformers within each pulse period (cf. **Fig. 4**) for minimum mains voltage and minimum output voltage at given output power one has to limit the duty cycle $\delta=\delta_+=\delta_-$ to

$$\delta_{\max} \le \frac{U'_{O,\min}}{\hat{U}_{N,\min} + U'_{O,\min}} . \quad (5)$$

($\hat{U}_{N,\min}$ denotes the amplitude of the minimum mains phase voltage, $U'_{O,\min}$ denotes the minimum output voltage referred to the primary).

B. *Stresses on the power components*

The current stress (rms average value) of the power components are compiled in **Tab.1**. Thereby, the rms value of the output capacitor current is estimated by replacing the superposition of the secondary currents of the phases by a single triangular shaped current pulse of same pulse width and same peak value

$$\hat{I}_2 = 2\hat{I}_U \frac{N_1}{N_2} \frac{\sqrt{3}}{2} . \quad (6)$$

The blocking voltage stress on the secondary side diodes D_S is defined by

$$\hat{U}_{Ds,r} = U_{O,\max} + \frac{N_2}{N_1} \cdot \hat{U}_U . \quad (7)$$

The maximum input voltage ripple can be estimated by

$$\Delta U_{U,i} = \sqrt{2} I_{N,i} \left(\frac{\delta^2}{2} - 2\delta - 2\right) \frac{1}{C_F f_P} . \quad (8)$$

C. *Flyback transformer*

For limiting the overvoltages caused by the transformer stray inductance a snubber network (cf. **Fig.5**(a)) has to be employed.

According to (2) a high output power related to a high peak value of the input current and therefore to a small inductance L. On the other hand, for given current density the winding area which in a first rough approximation directly determines the transformer stray inductance (whether interleaving of primary and secondary is employed or not) is proportional to the output power. In consequence, the stray factor σ of a high power flyback transformer is increasing with the square of the output power

$$\frac{L_\sigma}{L} = \sigma \propto P^2 . \quad (9)$$

According to (10) this would cause high overvoltage limitation losses P_{snub} and/or result in a low efficiency ($P_{snub}/P \propto \sigma$) of high power DCM flyback converters in case a dissipative overvoltage limitation is employed (Fig.5(a)).

A possible solution to this problem are loss-less clamping circuits or an auxiliary DC/DC converter (Fig.5(b)) feeding the overvoltage limitation energy to the secondary. A detailed analysis of the different concepts applicable will be presented in a future paper.

Due to the transformed output voltage U_O' the power transfered into a overvoltage clamp results to

$$P_{snub,i} = \left(\frac{U_{snub}}{U_{snub} - U'_O}\right) \frac{L_\sigma \cdot I_{N,i}^2}{\delta^2} \cdot f_P . \quad (10)$$

(U_{snub} denotes the voltage of the overvoltage limitation capacitor C_{snub} which has to be determined under consideration of the blocking capability of the switches S_+ and S_- and of the peak value of the mains phase voltage.)

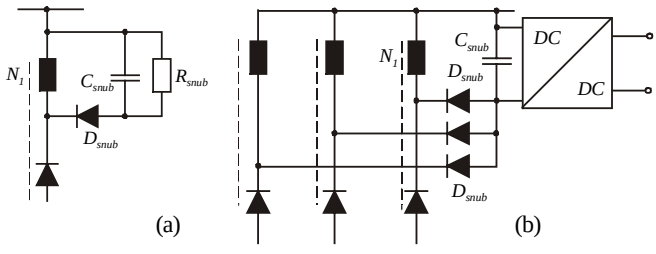


Fig. 5: DRC-overvoltage clamp connected across each partial primary winding of the flyback-transformers **(a)** and transfer of the overvoltage limitation energy to the system output by an auxiliary DC/DC converter **(b).**

IV. Control Concept and Dynamic Analysis

As shown in **Fig.6** the system control is by an output voltage controller or by an output current controller. During regular operation the output voltage controller is active. If the average value of the output current exceeds a given limit (e.g., in case of a short circuit of the load), the output voltage controller is inhibited and the output current controller takes over.

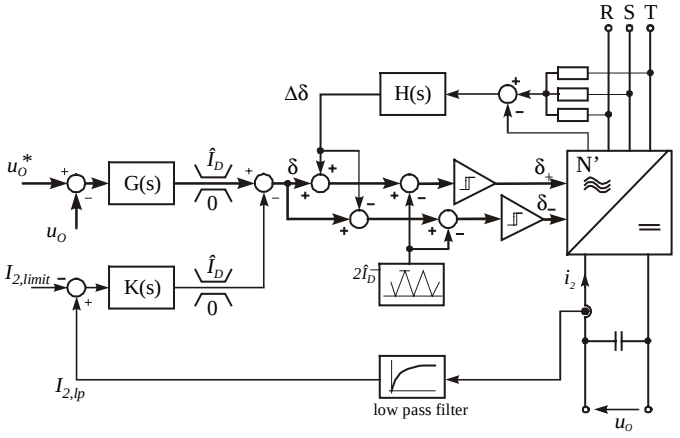


Fig.6: Control structure of the three-phase two-switch DCM flyback unity power factor rectifier.

Furthermore, as described in section 2, a control of the voltage potential $u_{N'}$ of the artificial neutral *N'* is provided. The reference value $u_{N'}^{*}$ is determined using a star connection of equal resistors connected to the system mains terminals.

The control oriented analysis of the three-phase system can be based on an equivalent DC/DC-flyback converter [5]. There, for characterizing the dynamic system behavior by transfer functions the nonlinear differential equations derived by state-space averaging (c.f. **Fig.7**)have to be linearized around an operating point. Accordingly, we define for the system quantities (i=R,S,T):

$$\delta = \Delta + \Delta\delta \tag{11}$$

$$u_{U,i} = U_{N,i,0} + \Delta u_i \tag{12}$$

$$u_O' = \tfrac{N_1}{N_2}\left(U_O + \Delta u_O\right) = U_O' + \Delta u_O' \tag{13}$$

$$i_{O,i}' = \tfrac{N_2}{N_1}\left(I_{O,i} + \Delta i_{O,i}\right) = I_{O,i}' + \Delta i_{O,i}' \tag{14}$$

A. Output voltage controller G(s)

As mentioned above at regular operation the converter operates in DCM with an output voltage controller in order to control the output voltage to a constant value. As shown in **Fig.8** converter input behavior is equivalent to a star connection of equal resistors R_i.

$$R_i = \frac{2Lf}{\Delta^2}. \tag{15}$$

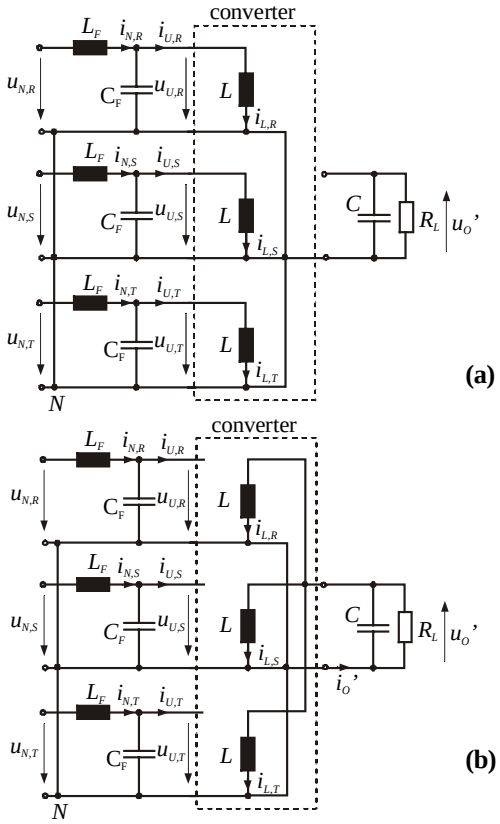
At the secondary side the current $i_{O,i}$ is determined by

$$i_{O,i}' = \frac{u_{U,i}^2 \cdot \delta^2}{u_O' \cdot 2 \cdot L \cdot f_P}. \tag{16}$$

The system behavior is characterized by the transfer function

$$\frac{\Delta u_O'}{\Delta\delta} = U(s) = \frac{\sum_j U_{N,j}^2 \cdot \Delta}{U_O' \cdot LC \cdot f_P} \cdot \frac{s^2 - s \cdot \frac{1}{R_i C_F} + 1}{\left(s + \frac{2}{R_L C}\right) \cdot \left(s^2 + s \cdot \frac{1}{R_i C_F} + \frac{1}{L_F C_F}\right)} \tag{17}$$

In order not to distort the input current for two-phase operation the crossover frequency of the output voltage controller has to be set to values known from the single phase PFC [8] (10..20Hz). Therefore, the parameter T_N of the PI-type controller (18) has been chosen as 16ms. The resulting root locus diagram given in schematic form in **Fig.9**(a).



(a)

(b)

Fig.7: Circuit topologies during on- **(a)** and off-states **(b)** of the switches S_+ and S_-.

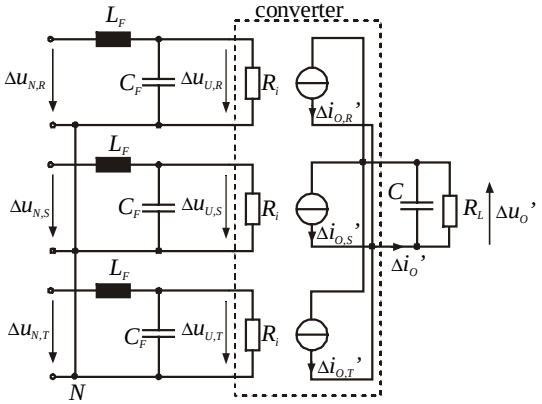


Fig.8: Small signal model of the flyback-converter in discontinuous conduction mode (DCM). (voltages $u_{U,i}$ assumed to be free of zero-sequence components).

$$G(s) = K_P + K_I \frac{1}{s} = K_P\left(1 + \frac{1}{sT_N}\right) = \frac{K_P}{T_N}\frac{1+sT_N}{s} \qquad (18)$$

For the laboratory prototype given in section V instability would occur at a controller gain of $K_P \geq K_{P,max}=0.88$.

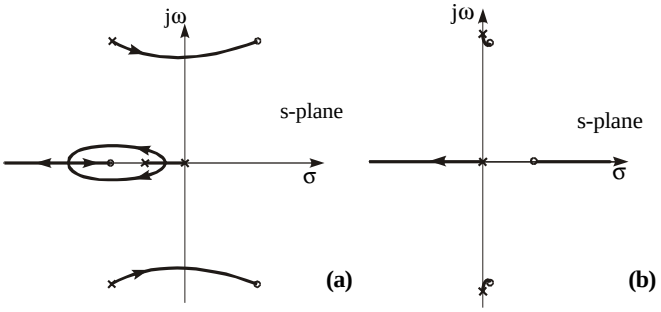


Fig.9 Root locus diagram of the output voltage control loop ($G(s)\cdot U(s)$) at discontinuous conduction mode **(a)** and of the output current control loop ($K(s)\cdot V(s)$) at continuous conduction mode **(b)**. The output voltage control loop is stable for $K_P<K_{P,max}$. The current control loop is not stable in case parasitic losses are neglected.

B. Output current controller K(s)

In case of an overload or output short circuit the converter operates in continuous conduction mode (CCM). Then, the output voltage controller is inhibited and the output current controller is active. In this case the converter does not show resistive input behavior. Assuming a short circuit on the output terminals ($U_O' = 0$) we receive the system transfer function

$$\frac{\Delta i_2}{\Delta\delta} = V(s) = \frac{(1-\Delta)\cdot\left(\sum_j |U_j| + 3U_{20}\right)\cdot\left(L_F C_F s^2 + 1\right) - \sum_j |I_j|\cdot s\cdot\left(L_F C_F L s^2 + \Delta L_F + L\right)}{L_F C_F L\cdot s\cdot\left(s^2 + \frac{L_F\Delta^2 + L}{L_F C_F L}\right)} . \qquad (19)$$

The root locus diagram for using a P-type controller, $K(s) = K_C$, is depicted in Fig.9(b). The current control loop is not stable independent of the controller gain for ideal components. Considering the main (current dependent) parasitic losses of the system by a resistor R_{LF} =0.2Ω connected in series with the filter inductance L_F a stabilization of the control loop could be achieved (for the laboratory prototype given in section V).

C. Balance controller H(s)

As already mentioned a difference of the average values of the currents i_{S+} and i_{S-} will result in a zero sequence component of the filter capacitor voltages (cf. **Fig.10**). Therefore, a simple P-type controller, $R(s) = K_B$, can be employed for controlling the potential of *N'*.

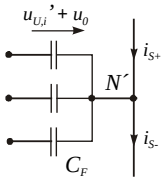


Fig.10: Occurrence of a zero sequence component $u_0 = {}^1/_3\Sigma\, u_{U,i}$ of the filter capacitor voltages $u_{U,i} = u_{U,i}' + u_0$ due to a difference of the (local) average values $i_{S+,avg}$, $i_{S-,avg}$ of the switch currents i_{S+}, i_{S-} ; $du_0/dt = 1/C_F$ ($i_{S-,avg} - i_{S+,avg}$).

Because the difference between the average values of the currents i_{S+} and i_{S-} is very small, only a very slow changing of the potential of *N'* will occur. Therefore a very low gain of the balance controller which has no influence on the control loop stability can be employed.

V. EXPERIMENTAL INVESTIGATION

The experimental analysis was on a laboratory prototype of the converter with the following specifications:

Input phase voltage:	U_N = 248....306V_{rms}
Output voltage:	U_O = 22....28V
Rated output power:	P_O = 1.2 kW (24V/50A)
Switching frequency:	f_P = 45 kHz
Efficiency:	η ≥ 87%

(the specified range for the rms value of the mains phase voltage corresponds to a line-to-line voltage range of 480V_{rms}±10%). The main system parameters have been selected as

$$\begin{aligned} U_O' &= 365\text{V} \\ \frac{N_1}{N_2} &= 12.4 \\ \delta_{max} &< 0.45. \end{aligned} \qquad (20)$$

Each transformer employs a magnetic core of type ETD59/N87 (ETD59/31/22, A_L=191nH, A_E=368mm^2, V=51200mm^3, air gap: s=4mm). With a number of turns N_1=37 of 60*0.1 litz wire, the primary inductance is L_1=261µH and the primary DC winding resistance is R_{N1}=266mΩ. For a secondary winding we have N_2=3 turns of copper foil 3*40*0.01mm which results in a DC winding resistance of R_{N2}=1.6mΩ. Primary and secondary windings are interleaved as shown in **Fig.11**, the resulting stray inductance is $L_\sigma \approx 7\mu$H.

The maximum admissible duty cycle for DCM is δ_{max} = 0.42. At nominal input phase voltage (U_N=277V_{rms}) nominal output voltage (U_0=24V) the duty cycle results to δ_N=0.376.

The peak value of the transformer flux is

$$\hat{B} = \frac{\sqrt{2}\cdot U_N\cdot\delta_N}{N_1\cdot A_E}\cdot\frac{1}{f_P} = 240\text{mT}. \qquad (21)$$

The rms value of the main current results to

$$I_N = \frac{P_O}{\eta\cdot 3\cdot U_N} = 1.66\text{ A}, \qquad (22)$$

and the maximum peak value of the input current is equal to

$$\hat{I}_{U,i} = I_N\cdot\sqrt{2}\cdot\frac{2}{\delta_N} = 12.5\text{A}. \qquad (23)$$

The current stress of the power components compiled in **Tab.2** have been calculated using the equations given in Tab.1.

Figure 12 shows the input capacitor voltage $u_{U,R}$ and input current $i_{N,R}$ of the rectifier at 400V line-to-line input and 24V/20A output. There, the power factor is λ=0.985 and the total harmonic distortion of the input current is THD_I =7.4%.

TABLE II:
CURRENT STRESS ON THE POWER COMPONENTS FOR RATED INPUT AND OUTPUT VOLTAGE AND RATED OUTPUT POWER

Component	Primary Diodes	Secondary Diodes	Switches	Transformer		Output Cap.	Filter Cap.
	I_{Dp} [A]	I_{Ds} [A]	I_S [A]	I_{N1} [A]	I_{N2} [A]	I_C [A]	I_{CF} [A]
AVG	0.75	16.7	2.24	0.75	16.7		
RMS	2.21	40.7	4.22	2.21	40.7	76.6	2.65

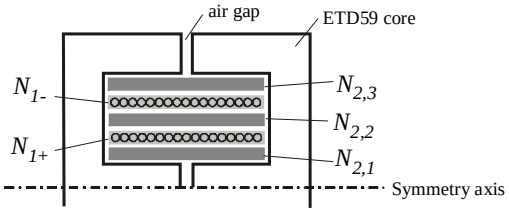


Fig.11: Arrangement of the windings of the flyback transformer. The secondary winding N_2 is split up in $N_{2,1}$, $N_{2,2}$ and $N_{2,3}$, which are connected in parallel in order to minimize the stray inductance[9].

Local time behavior of switch voltage and current is shown for power transistor S_+ in **Fig.13**. The transistor blocking voltage stress is limited to ≈850V.

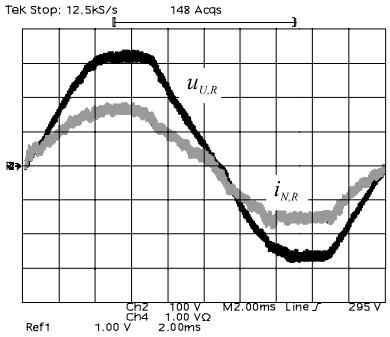


Fig.12: Measured input current (1A/div) and input voltage (100V/div) @ 24V/20A output and 400V line-to-line input.

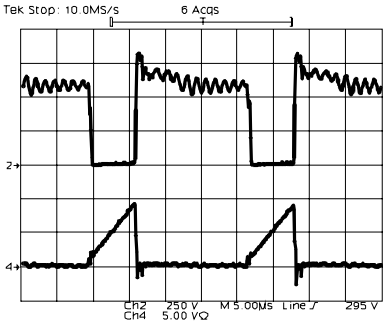


Fig.13: Local time behavior of switch voltage and current; upper trace: u_{S+} (250V/div), lower trace: i_{S+} (5A/div).

VI. CONCLUSIONS

In this paper the design and experimental verification of a novel 1.2kW three-phase flyback-type unity power factor rectifier has been presented. The rectifier does employ two switches with a blocking capability of 1000V and can be used with mains voltages up to 530V. The total harmonic distortion of the input current of a first laboratory system is lower than 7.4% and/or the power factor is higher than 98.5% in an output power range of 0...500W @ $400V_{rms}$ line-to-line input and $24V_{DC}$ output.

The continuation o the research will focus on the optimization of the design of high power flyback phase transformers which are the key component for achieving a high system efficiency. There, besides interleaving of the primary and secondary windings, concepts for splitting up a single high power transformer into several transformers of lower power (and therefore lower stray coefficient, cf. (9)) connected in series or in parallel will be considered.

Furthermore, the parallel connection of several three-phase systems will be investigated in order to lower the input filtering effort and the current stress on the output capacitors.

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