Implementation of a Novel Control Concept for Reliable Operation of a VIENNA Rectifier under Heavily Unbalanced Mains Voltage Conditions

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***Abstract* – The practical realization of a novel concept for output voltage control and mains voltage proportional guidance of the input currents of a three-phase/switch/level PWM (VIENNA) rectifier system being connected to a heavily unbalanced mains is presented. The control is investigated experimentally for a wide input voltage range 6.5kW prototype of the VIENNA rectifier.**

I. INTRODUCTION

High power telecommunications power supply modules usually show a two-stage topology, i.e., a front-end three-phase power factor corrector (e.g., a three-phase/switch/level PWM VIENNA rectifier) and a DC/DC converter output stage. There, according to the required high reliability of the power supply the PWM rectifier system should continue to operate also in case of a mains failure, i.e. for a transition from a symmetric to a heavily unbalanced mains voltage condition.

In [1] a control concept has been presented which does allow operation also in case only two phases of the mains are present. However, there a detection of the phase loss is required and a change-over of the control structure has to be performed in case of a phase loss, which could cause problems for some mains failure conditions. A control concept which does operate at a general unbalance of the mains phase voltages, i.e. mains phase voltages showing different amplitudes and/or a deviation from the symmetric 120° phase displacement without a change-over has been proposed in [2],[3].

In this paper the practical implementation and the dynamic behavior of the phase-oriented control proposed in [2] for a three-phase PWM (VIENNA) rectifier (cf. **Fig.1**) is presented. The control concept does ensures a mains voltage proportional guidance of the input phase currents for any unbalance of the mains phase voltages and does tolerate a phase loss. A short review of the control structure is given in **section 2**. In **section 3** a practical low-cost implementation of the control concept is described in detail. The realization effort and the estimated costs for a production of the control in higher quantities are shown in **section 4**. The experimental investigation of the stationary and dynamic behavior of the control is given in **section 5** in connection with a 6.5kW prototype of the VIENNA rectifier.

II. CONTROL STRUCTURE

As shown in **Fig.2** the control concept of the VIENNA rectifier consists of an inner input current control loop (controller $G(s)$) which is realized as a ramp comparison current controller (average current mode controller) for each phase and an outer output voltage loop (controller $H(s)$). Furthermore, the balance of the partial output voltages is controlled by a controller $R(s)$ defining a zero sequence component i_0 of the input current reference values. For the inner current control loop a mains voltage pre-control signal m_i [4] which does contain a zero sequence quantity u_0 for extending the modulation limit is used. Providing mains voltage pre-control signals m_i (which can be derived directly from the measured mains phase voltages) a high quality input current shape and/or a low current control error can be achieved with a purely P-type current controller.

Due to the missing connection of the rectifier system to the mains neutral N the mains currents $i_{N,i}$ cannot contain a zero sequence component. Therefore, also for unbalanced mains (where a significant zero sequence component of the actual mains phase voltages $u_{N,i}$, measured with reference to the neutral N does occur) only the positive and negative sequence system of the input voltages $u_{N,i}$ has to be used for the derivation of the input current reference values and for the input voltage precontrol. This can be achieved by referring the measurement of the mains voltages to an artificial neutral point N'. In this case a zero sequence component $u_{N,0}=u_{N,R}+u_{N,S}+u_{N,T}$ of the mains voltages $u_{N,i}$ does not appear in the measured voltages $u_{N,i}$'.

The input current reference values $i_{N,i}$* are derived in the following way:

- The input conductivity reference value g* is calculated by interpreting the output voltage controller output as output power demand p* according to (1). ($U_{N,i}$´ denotes the rms value of the mains phase voltage $u_{N,i}$)
- The input conductivity is limited in order to keep the peak value of the input currents lower than a maximum value $\hat{I}_{N,max}$, cf. (2).
- The reference values of the input currents $i_{N,i}$* are derived by multiplying the input conductivity g* with the measured input voltages $u_{N,i}$' , cf. (3)

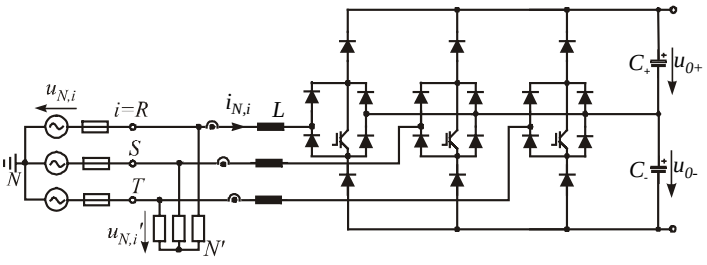

Fig.1: Power stage of the three-phase/switch/level PWM (VIENNA) rectifier. Artificial neutral point N' formed by star connection of equal resistors.

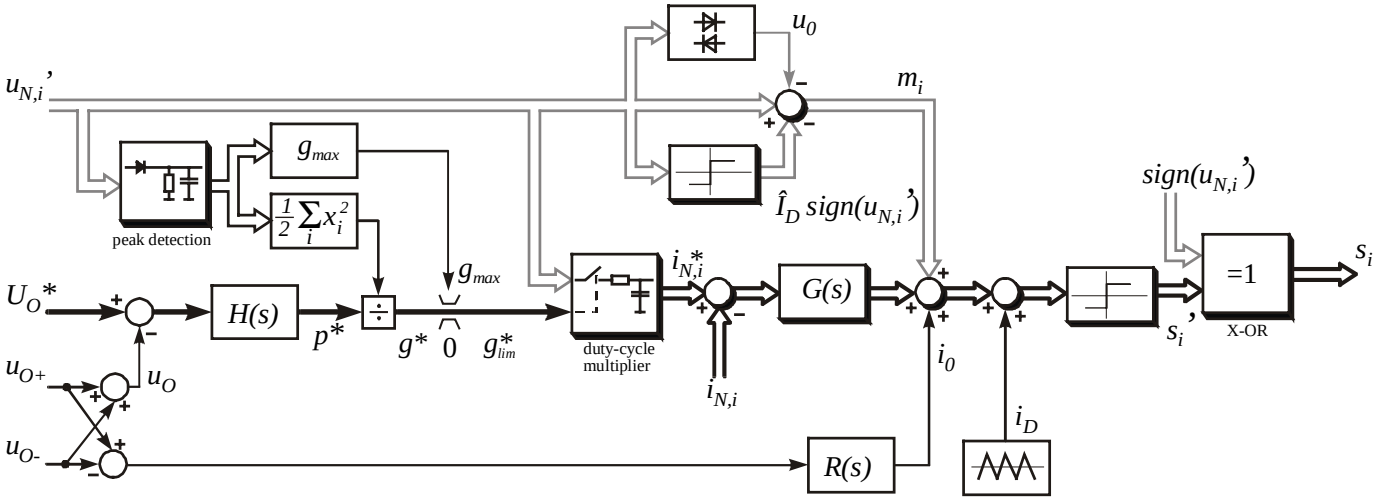

Fig.2: Control structure of a VIENNA Rectifier tolerating heavily unbalanced mains voltage conditions; current controller *G(s)*, output voltage controller *H(s)*, partial output voltage balancing controller *R(s)*. Connections being equal for all phases are combined in double lines; $x_i = \hat{U}'_{N,i}$.

$$g^* = \frac{p^*}{U'^2_{N,R} + U'^2_{N,S} + U'^2_{N,T}} \tag{1}$$

$$g^*_{\lim} < g_{\max} = \frac{\hat{I}_{N,\max}}{\max[\hat{U}'_{N,i}]} \tag{2}$$

$$i^*_{N,i} = g^*_{\lim} \cdot u'_{N,i} \tag{3}$$

Remark: The derivation of the current reference values corresponding to (1)-(3) is not only required for the VIENNA rectifier. Also other three-phase rectifier concepts which should reliably operate under heavily unbalanced mains conditions or in a wide input voltage range have to perform (1)-(3) in a similar manner.

A detailed theoretical description of the control structure shown in Fig.2 is given in [5] and [6] and shall, therefore, be omitted here for the sake of brevity.

III. Practical Implementation

For a practical realization one has to consider, that after disconnection or reconnection of a mains phase, a stepwise change of the input power of the rectifier system does occur because the input conductivity reference *g** is changed only with low dynamics by the output voltage controller. This could result in an output voltage surge or in an input overcurrent condition. Therefore, in addition to the control concept show in Fig.2 an overcurrent protection has to be employed which does reduces the input conductivity reference immediately if the input current or output voltage exceeds a given maximum admissible level *I-limit* and/or U_O*-limit* (cf. Fig.5).

In order to achieve a good power factor the input current control bandwidth is selected as $20.f_N$=1kHz (f_N denotes the mains frequency). The output voltage control bandwidth has to be set to low values as known from single-phase power factor correction (10...20 Hz) [7]. This is due to the pulsation of the rectifier output power with twice the mains frequency in case of unbalanced mains voltage conditions or for two-phase operation which results in a corresponding low-frequency output voltage ripple and would lead to a low-frequency distortion of the input current shape (deviation from the sinusoidal and/or mains voltage proportional shape) for high output voltage controller gain and/or bandwidth.

A high output voltage control error which could occur in case of load steps due to low controller gain/bandwidth there is prevented by a step-wise increase of the controller gain for high magnitudes of the control error. The selected bandwidths of the different tasks to be performed by the rectifier control (cf. Fig.2) are compiled in **Tab.1** (f_S denotes the switching frequency; f_M denotes the mains frequency).

TABLE I:
SIGNAL BANDWIDTHS REQUIRED FOR THE CONTROLLER FUNCTIONS

no.	function	min. bandwidth
1	triangle generator	~10·f_S
2	comparator, X-OR-gates	~10·f_S
3	pre-control signal derivation	10·3·f_M
4	current controller	20·f_M
5	overcurrent protection	20·f_M
6	multiplier (3)	20·f_M
7	limitation g_{max} (2)	f_M
8	calculation of g^* (1)	3·f_M
9	output voltage controller	10Hz
10	Partial output voltage balancing controller	2Hz

As shown in Tab.1, the controller tasks can be divided in fast functions (bandwidth >1kHz) and slow functions (bandwidth <1kHz). The main calculations (1),(2) have to be performed only with low bandwidth and therefore can be realized advantageously in digital form using a low cost µC. Functions requiring a high bandwidth are realized in analog technique. A detailed description of the tasks of the microcontroller and of the analog circuitry is given in the following.

A. Microcontroller

The microcontroller (µC) employed for performing the relatively slow control and supervisory tasks is of type ATMEL AT90S8535. This µC does provide among many other functions an eight channel 10bit analog to digital converter (ADC), a dual 8, 9 or 10bit PWM, and two additional timers with a processor speed of eight MIPS (mega instructions per second).

In the case at hand the functions realized by the µC are

- the total output voltage control and
- the partial output voltage symmetry control,
- the calculation of the input conductivity reference including the conductivity limit calculation as well as
- the input voltage supervisory in order to manage the automatic start and stop of the rectifier and
- the signalization of failures.

1) AD-conversion/Calculations/Control: The maximum possible sampling frequency of the ADC is determined by the ADC clock frequency which must not exceed 200kHz for a maximum admissible inaccuracy of 2LSB and the fixed number of 14 clock cycles. The resulting maximum sample frequency with an 8MHz clock is 8.9kHz for one channel. For using seven channels (positive and negative output rail voltages, three mains phase voltages, reference voltage and optionally the load current) the sampling frequency drops to 1.3kHz (784µs). So the crossover frequency of the controller and the deadtime for the input voltage and the load current feedforward (not implemented in the case at hand) are typically two times the sampling frequency and/or half of the sampling time (approximately 400µs). **Fig.3** shows the realization of the control and feedforward tasks in graphical form. The time intensive calculations (PI-type output voltage control, multiplications, divisions) are done after the ADC interrupt after fetching the conversion values, i.e. (1) is calculated piecewise during conversion of channel 3, 4, 5, 6 and 0.

2) Startup and light loads: In parallel to this relatively fast task a slow timer with an 8ms interrupt period is implemented. In this slow task the highest two instantaneous phase voltage values are added in order to provide a basis for the automatic start and stop function of the PFC. The PFC enters the soft start mode if the sum of the two highest input phase voltages is in a predefined voltage window (according to the line-to-line voltage $U_{N,l\text{-}l}$ = 300 ... 480V (assuming a symmetric input line-to-line voltage conditions) and if the output voltage is higher or equal to a value which would result from three-phase diode bridge rectification. The soft-start mode is succeeded by normal operation as soon as the output voltage reaches the output voltage reference value. The rectifier is disabled if the input voltage is out of the allowed input voltage window of $U_{N,l\text{-}l}$ = 250 ... 530V. Also the conductance limit calculation according to (2) and a burst mode for operation at light loads is done during this 8ms interrupt routine.

3) Failure management: In case no interrupt routine (ADC or 8ms timer) is running, the µC is polling over the input failure pins and a manual stop button input pin in order to signalize a fault condition by turning on a LEDs and/or to stop the unit in case of a failure. This stop is only for backup purposes, because any failure does disable the power transistor drive signals immediately by hardware. In the case at hand a manual reset of the unit and of the µC is required after a fault condition has occurred.

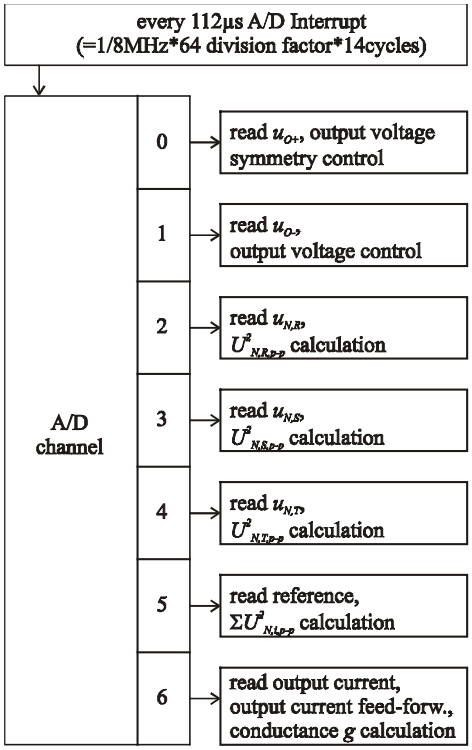

Fig.3: Program structure of the ADC interrupt routine which performs the control and feedforward tasks. After reading the digitized value the A/D conversion channel is switched-over to the next channel and the A/D conversion is initiated again.

B. Analog Part

1) Signal measurement: The control concept shown in Fig.2 requires the sensing of the input voltages $u_{N,i}$', of the partial output voltages u_{0+}, u_{0-} and of the input currents $i_{N,i}$. The input voltages $u_{N,i}$' are measured with reference to an artificial mains neutral N', which is formed by a star connection of 3 equal resistors and three capacitors connected in parallel (for each phase 220kΩ//22nF).

The signal ground of the control board is connected to the artificial neutral N' which - different to e.g. the output voltage center point - does not show a switching frequency common mode voltage with reference to safety ground (earth). The input voltages therefore can be measured by using simple voltage dividers (1:53). Sensing of the output voltages is by a differential amplifier (10.3mV/V). The input current sensing by compensating DC current transducers (0.43V/A).

2) Pre-control generator: According to (4) the input voltage pre-control signal m_i is formed by combining

- the input voltage $u_{N,i}$',
- the square wave function $sign(u_{N,i}')$ and
- the zero sequence component u_0.

This can easily be realized in analog technique (U_O denotes the output voltage of the rectifier, M denotes the pulse width modulation index and $\hat{I}_D$ denotes the amplitude of the triangular carrier of the pulse width modulator

$$m_i = \hat{I}_D \cdot \left(M \cdot \frac{2 \cdot u_{N,i}'}{U_O^*} - sign(u_{N,i}') + M \cdot \frac{2 \cdot u_0}{U_O^*} \right) . \qquad (4)$$

The zero sequence component u_0 which is used do extend the maximum modulation limit and furthermore does reduce the 3rd harmonic of the center point current can be derived using [4]

$$u_O = \frac{1}{2} \cdot \left(\max(u_{N,i}') + \min(u_{N,i}') \right). \qquad (5)$$

3) Derivation of the current references: The input current references are calculated according to (3) by multiplying the limited input reference conductivity with the measured input voltages $u_{N,i}$'. Using the on-chip PWM generator of the µC a simple duty cycle multiplier [8] can be realized which does show considerably lower realization costs as resulting for a conventional multiplier realization (D/A converter in connection with an analog multiplier). According to the switching frequency of the PWM generator of f_P=15kHz and with respect to a bandwidth of the multiplication of at least 1kHz the time constants of the two stage filter of the duty-cycle multiplier have been chosen as $\tau_1 = R_1 \cdot C_1$ =50µs and $\tau_2 = R_2 \cdot C_2$ =120µs (cf. **Fig.4**).

For achieving a sinusoidal shape of the input current reference the duty cycle multiplier has to show a linear transfer characteristic $u_I = \Delta \cdot u_U$ (for a constant duty cycle Δ). In the case at hand equal time constants are employed for charging and discharging of the filter capacitor C_1.

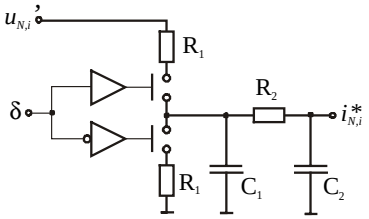

Fig.4: Practical realization of the duty-cycle multiplier.

4) Ramp comparison current control: The output of the P-type current controller *G(s)*, the mains voltage pre-control signal m_i and the output i_0 of the controller balancing the partial output voltages are added and compared with the triangular carrier signal i_D with switching frequency f_P and amplitude $\hat{I}_D$. In each phase the resulting switching signal s_i' is inverted according to the sign $sign(u_{N,i}')$ of the corresponding input phase voltage $u_{N,i}'$ using an X-OR gate. The output signal of the X-OR gate is buffered and wired to the gate drive opotcoupler. In the case at hand the current controller gain K_I is set to unity and the amplitude of the carrier signal is $\hat{I}_D$=7.4V.

5) Overload protection after input phase reconnection: As already mentioned a input overcurrent and/or output overvoltage could occur after reconnection of a missing mains phase. In order to limit input current and output voltage to maximum admissible levels in this case the input conductivity has to be reduced immediately. Due to the representation of input conductivity reference by a PWM-signal in connection with the duty-cycle multiplier a fast reduction can be achieved by suppressing every second pulse of the PWM signal (cf. **Fig.5**). Thereby, the input conductivity reference and/or the input current reference values are reduced by a factor of 2.

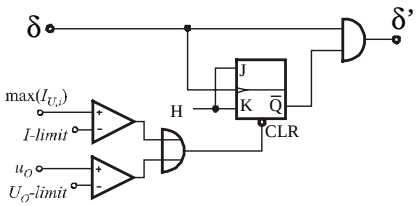

Fig.5: Reduction of the input conductivity reference value in case of an input overcurrent or output overvoltage condition. The input current limit (*I-limit*) is set to 20A, the output voltage limit (U_O-*limit*)is set to 700V.

IV. Realization Effort

The control hardware is realized in surface mount technology (SMT) on a two layer printed circuit board (PCB) with overall dimensions of 16cm x 8 cm (6.3in x 3.15in). The main components and their estimated costs (for purchasing in higher quantities) are compiled in **Tab.II**. In Fig.6 a photography of the control board is shown. Semiconductors and ICs are placed only on the top layer, resistors and capacitors are mounted on both sides.

TABLE II:
QUANTITY OF THE MAIN COMPONENTS AND ESTIMATED COSTS

Quantity	Part	Costs[€]	Total [€]
1	PCB (2 layers)	5.0	5.0
1	AT90S8535 (µC)	4.7	4.7
10	TL084	0.30	3.0
3	DG212/211	0.50	1.5
110	Capacitors (1206)	0.012	1.32
270	Resistors (1206)	0.004	1.08
70	Diodes	0.01	0.7
3	LM339	0.22	0.66
3	74xx	0.22	0.66
2	LM319	0.30	0.6
			19.22

Fig.6: Control board of the VIENNA Rectifier in comparison with a TO247–type power semiconductor package. The overall dimensions of the control board are 16cm x 8 cm (6.3in x 3.15in).

V. Experimental Results

The experimental results given in the following are derived in connection with a prototype of the VIENNA Rectifier with the following operating parameters:

- rated input power P = 6.5kW
- mains voltage U_N = $400V_{l\text{-}l}$+/-20% (320...480V)
- max. input current $\hat{I}_{N,max}$ = 16.6A
- output voltage U_0 = 670V
- switching frequency f_s = 25kHz.

A. Control signals

1) Derivation of the pre-control signals: As shown in (5) the zero sequence component u_0 of the input voltage pre-control signals m_i can be derived directly from the measured mains phase voltages $u_{N,i}$'. **Figure 7** shows the measured input phase voltages and the resulting zero sequence component u_0 within a mains period.

The formation of the input voltage pre-control signals m_i corresponding to (4) is shown in **Fig.8**.

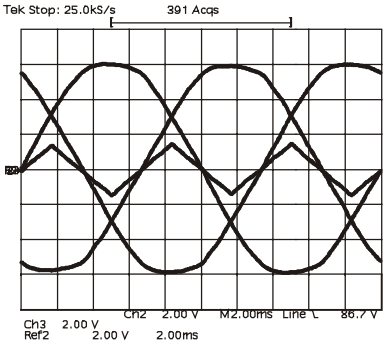

Fig.7: Zero sequence component u_0 of the input voltage pre-control signals m_i derived from the measured input phase voltages $u_{N,i}$'.

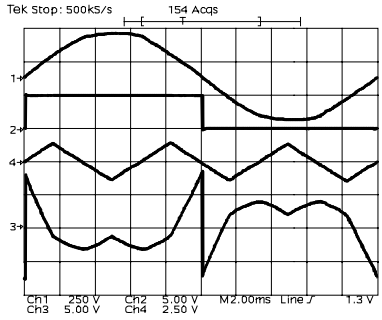

Fig.8: Formation of the input voltage precontrol signal m_i. Shown are the input phase voltage $u_{N,R}$' (CH1), the resulting input voltage precontrol signal m_R (CH3) and the zero sequence component u_0 (CH4).

2) Reduction of the input conductivity: The reduction of the input conductivity reference in case a mains phase current does exceed *I-limit* as, e.g. could occur for reconnection of a missing mains phase is shown in **Fig.9**.

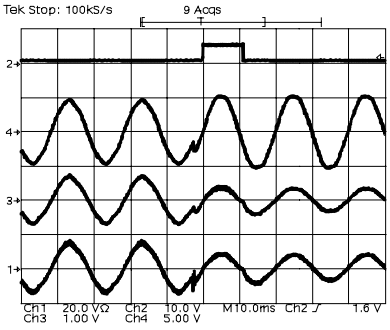

Fig.9: Limitation of the rectifier input currents in case of reconnection of a missing mains phase. Shown are the limitation active signal (CH2 at 10V/div), the measured input phase voltage $u_{N,S}$ (CH4 at 5V/div), the input current reference value $i_{N,S}$* (CH3 at 1V/div) and the resulting input current $i_{N,S}$ (CH1 at 20A/div) for reconnection of phase *R*.

Due to the reconnection of phase *R* a step-like change of the phase of the measured input phase voltages does occurs. As shown in Fig.9 the input conductivity is limited approximately 4ms after the reconnection of phase *R* because of the rising output voltage/input current. After 12ms the reduction of the input conductivity is released and the µC has calculated the suitable input conductivity reference value for three-phase condition and the amplitude of the input currents remains constant.

B. Mains behavior

1) Balanced mains: The behavior of the rectifier for balanced mains is shown in **Fig.10**. There, a power factor of λ=1.0 and a total harmonic distortion of the input currents of max. *THD(I)* =3.8% has been verified by measurements.

After disconnection of phase *R* the *THD(I)* of the remaining input currents does slightly increase to 4.0%.

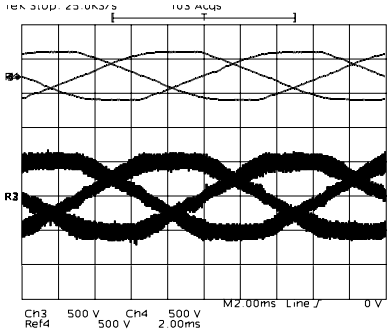

Fig.10 Measured input phase voltages $u_{N,i}$' (500V/div) and mains phase currents $i_{N,i}$ (7.5A/div).

2) Disconnection of phase R (tripping of a fuse): For two-phase operation a pulsation of the output power/voltage with twice the mains frequency does occurs. Thereby, the output voltage ripple is determined by the capacitance of the series connection of the output capacitors C_+ and C_-. In the case at hand output capacitors C_+=C_-=4*470µF are employed. There, the peak-to-peak value of the output voltage ripple at 320V input voltage and 3kW output power is 25V.

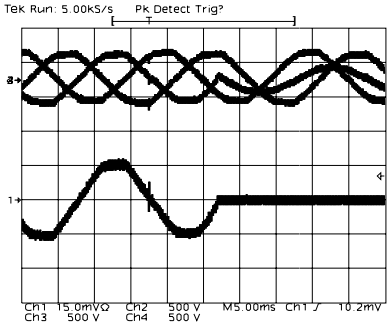

Fig.11: Measured input phase voltages $u_{N,i}$' (500V/div) and input current $i_{N,R}$ (7.5A/div) for disconnection of phase *R*.

The time behavior of the measured mains phase voltages and of the mains phase current $i_{N,R}$ are shown in **Figs. 11** and **12** for disconnection and reconnection of phase *R*. As expected an input current surge does occurs after reconnection of the

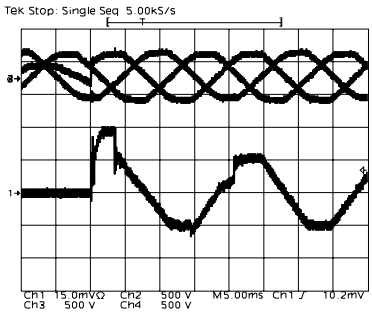

Fig.12: Measured input phase voltages $u_{N,i}$' (500V/div) and input current $i_{N,R}$ (7.5 A/div) for reconnection of phase *R* (return to symmetric mains condition).

missing phase. Within one mains period after reconnection the output voltage controller has calculated the correct value of the input conductivity for the balanced mains condition and the input current amplitude remains constant.

Also for a short circuit between two mains phases (disconnection of phase *R* and connection to phase *S*) or for an input phase earth fault (disconnection of phase *R* and connection to the mains neutral *N*) the system behavior is very much comparable to entering into two-phase operation. Therefore, a more detailed discussion should be omitted here in the sake of brevity.

VII. CONCLUSIONS

In this paper the practical implementation of a novel control concept for the VIENNA rectifier operating under heavily unbalanced mains voltages condition has been discussed.

In order to achieve an economic solution, the control concept is realized by a low cost µC performing the low frequency tasks in combination with an analog circuit performing the high frequency tasks, like ramp comparison mains current control. Thereby, the mains current reference values are derived from the measured mains voltages by duty-cycle multipliers which are controlled by the µC PWM generator.

As the experimental analysis verifies the control concept shows a high performance for three-phase and two-phase operation. Considering further the low realization costs the control is well suited for application in an industrial product, e.g. in a high power telecommunications power supply module.

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