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Analytical Modeling and Comparison of EMI Pre-Filter Noise Emissions of Three-Phase Voltage and Current DC-Link Converters

Daifei Zhang, Michael Leibl, Jonas Mühlethaler, Jonas Huber, and Johann W. Kolar

***Abstract*—Three-phase power-factor-correction (PFC) rectifiers or motor drive inverters can be realized using two dual converter topologies featuring either a voltage DC-link (voltage source) or a current DC-link (current source). This paper presents a generic comparison of the pre-filter differential-mode (DM) and common-mode (CM) electromagnetic interference (EMI) noise emissions of these two topologies (considering only the switching stage), which serve as indicators for the required EMI filter attenuation and, hence, EMI filter realization effort. In contrast to the voltage DC-link topology, the DM pre-filter noise of the current DC-link topology is primarily attributed to the current pulses generated by its switching stage, resulting in high-frequency voltage drops across the 50-Ω measurement resistor employed in line-impedance stabilization networks (LISNs) as defined by, e.g., the CISPR 11 standard. Addressing this aspect, low-complexity analytical expressions for approximating the envelopes of the pre-filter DM and CM noise amplitude spectra are derived and experimentally verified using 400 V (line-to-line rms), 10 kW voltage and current DC-link AC/DC converter demonstrator systems. The DM pre-filter noise of current DC-link converters is lower than that of the voltage DC-link converters if the equivalent AC resistance the converter represents to the mains is higher than the LISN's 50-Ω measurement resistor. On the other hand, the current DC-link converter's CM pre-filter noise is, in typical cases, lower than the voltage DC-link converter's; current DC-link converters are thus an interesting choice for motor drive inverter applications.**

I. Introduction

To ensure electromagnetic compatibility (EMC), all power electronic converter systems connected to the public low-voltage mains must comply with specific limits for electromagnetic interference (EMI) noise emissions defined in standards such as CISPR 11 [1]. These limits are specified as a voltage across a 50-Ω measurement resistor R_m that is part of a line impedance stabilization network (LISN), see **Fig. 1a**. The voltage limits are frequency-dependent ($150\,\mathrm{kHz}$ to $30\,\mathrm{MHz}$ today [1]; future extensions down to $2\,\mathrm{kHz}$ are in preparation [2]) and typically in the range of $0.2\,\mathrm{mV}$ to $10\,\mathrm{mV}$ ($46\,\mathrm{dB\mu V}$ to $80\,\mathrm{dB\mu V}$). Power converters achieve compliance with EMI limits by employing one or more LC filter stages to attenuate the pre-filter noise generated by the switching stage [3]–[7], whereby separate filter stages for differential-mode (DM) and common-mode (CM) noise components are always implemented [8]–[10]. The required filter attenuation determines the EMI filter's size and losses. Thus, converter topologies with low pre-filter noise emission levels are preferred.

Three-phase (3-Φ) pulse-width modulated (PWM) converters find a wide range of industrial applications, e.g., as EV chargers or PV inverters. There are two fundamental, dual converter topologies [11], [12]. For both, i.e., for voltage DC-link (voltage source) converters [13], [14] and current DC-link (current source) converters [15], [16], extensive research has been conducted on modeling the DM and CM EMI noise sources and designing the corresponding EMI filters, e.g., the required attenuation of the EMI filter is conventionally determined using circuit simulations [17]–[19]. Comparisons of DM and CM EMI filtering efforts between voltage and current DC-link converters have also been presented for several specific realizations [20]–[23].

However, a generic comparison of the DM and CM EMI filter attenuation requirements for voltage and current DC-link converters is still missing. Such a generic comparison should be based on modeling the DM and CM noise sources using straightforward analytic expressions. Whereas [24] provides a suitable simplified modeling procedure for the DM emissions of single-phase voltage DC-link systems, a similar approach for 3-Φ systems remains absent.

Therefore, in this paper, the method from [24] is first extended to model the pre-filter DM and CM noise emissions of 3-Φ voltage DC-link (**Section II**) and current DC -link converters (**Section III**). The resulting low-complexity analytic approximations of the DM and CM pre-filter noise emission amplitude spectra capture the characteristic dependencies on the mains voltage and output power level and/or DC-link voltage and DC-link current. Second, these analytical approximations facilitate a *generic* comparison of the DM and CM EMI filter attenuation requirements of voltage and current DC-link converters in **Section IV**. Depending on the equivalent AC resistance the converter represents to the mains in relation to the LISN measurement resistance, either voltage or current DC-link rectifiers result in lower pre-filter DM EMI noise emissions and, therefore, require less filter attenuation. On the other hand, the pre-filter CM noise emissions of current DC-link converters tend to be lower for most typical voltage and power levels, which is especially advantageous for motor drive inverter applications.[1] Finally, **Section V** concludes the paper.

II. EMI Pre-Filter Noise Emission of Three-Phase Voltage DC-Link PFC Rectifier Systems

The two-level 3-Φ voltage DC-link PFC rectifier (see **Fig. 1a**) is a widely used industry-standard solution due to its simplicity and reliability. Depending on the 3-Φ switching

[1]For the sake of clarity, the paper considers PFC rectifiers for the explanations. Nevertheless, the derived expressions for the DM and CM pre-filter noise emissions and the conclusions are also valid for the opposite power flow direction of, e.g., PV inverter or motor drive inverter systems.

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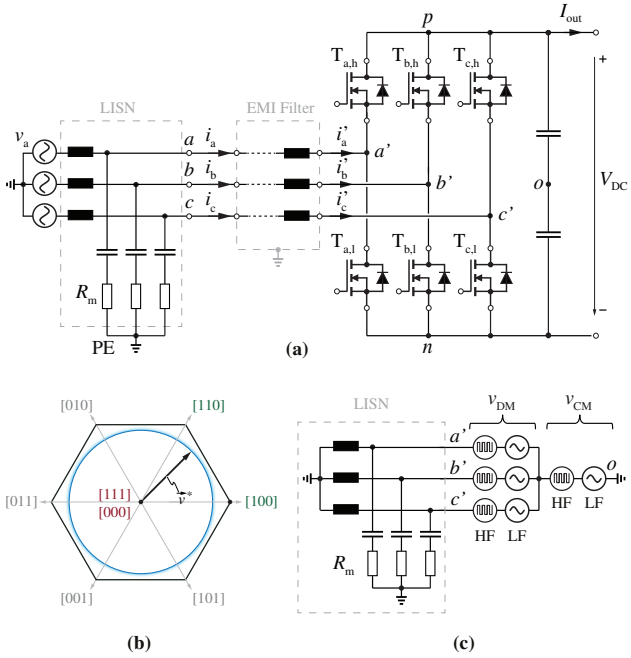

Fig. 1: **(a)** Power circuit of a two-level three-phase (3-Φ) voltage DC-link PFC rectifier (including an EMI filter stage where boost inductors are shown as the first filtering components) connected to the mains via a LISN. **(b)** The rectifier's switching stage can generate six active and two zero voltage space vectors (SVs) at the switching nodes; SVPWM is typically used to synthesize a desired local average voltage SV $\vec{v}^*$. **(c)** Combined DM and CM equivalent circuit where the switching stage is modeled by DM and CM voltage sources (both LF and HF); the HF DM and CM voltage sources represent the DM and CM pre-filter noise emissions.

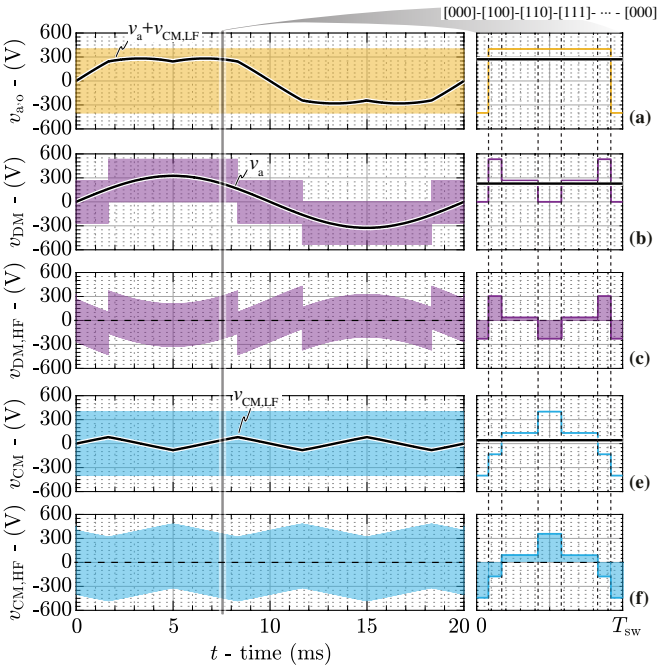

Fig. 2: Simulated key waveforms (with a zoomed view over one switching period) of the two-level 3-Φ voltage DC-link PFC rectifier (see **Fig. 1a**) operating with a 400 V (line-to-line rms) mains, 800 V DC-link and/or output voltage, and 10 kW output power using the standard SVPWM. Taking phase a as an example, **(a)** shows the switching stage phase voltage $v_{a'o}$, which can be decomposed into **(b)** DM and **(e)** CM components. Furthermore, **(c)** and **(f)** show the DM and CM HF noise voltages (i.e., the pre-filter DM and CM noise emissions). Note that a typical symmetric switching sequence, i.e., mirrored with respect to the center of a switching period or the switching state [111] in the selected sector, is applied, and only the first half over one switching period is shown on top.

state, typically formed by three two-level bridge legs, a total of six active and two zero voltage space vectors (SVs) shown in **Fig. 1b** can be generated at the input of the switching stage. During each switching period, a local average voltage SV $\vec{v}^*$ is generated, corresponding to three local average values of the 3-Φ voltages. This is achieved by applying each adjacent voltage SV during its respective dwell time. Typically, the correct sequence and dwell times are obtained using SV pulse-width modulation (SVPWM), which is further explained in **Appendix A**.

Furthermore, the pre-filter DM and CM EMI noise emissions can be modeled by replacing the switching stage with three voltage sources that represent the switch-node phase voltages with respect to the (virtual) midpoint o of the DC output, i.e., $v_{a'o}$, $v_{b'o}$, and $v_{c'o}$. These voltage sources can then be decomposed into dedicated voltage sources for low-frequency (LF) DM and CM components (e.g., the desired synthesized DM input voltage) as well as high-frequency (HF) DM and CM noise voltage sources (see **Fig. 1c**). This facilitates a decoupled analysis of DM and CM pre-filter noise emissions and, ultimately, of the filter designs. Note that the direct connection of the DC-link midpoint to protective earth (PE) shown in **Fig. 1c** represents the worst case for CM noise. This worst case for CM noise emissions is ensured by shorting the parasitic capacitances, which would be in series with the LISN measurement resistors as voltage dividers, and by disconnecting the capacitances, which would be connected in parallel to the LISN measurement resistors as current shunts. Both effects would result in reduced CM noise emissions. [2]

Taking phase a of the analyzed two-level 3-Φ voltage DC-Link PFC rectifier as an example, the DM and CM voltage sources are expressed as [13], [14]:

$$v_{\mathrm{DM}} = v_{\mathrm{DM,LF}} + v_{\mathrm{DM,HF}} = v_{\mathrm{a'o}} - v_{\mathrm{CM}}, \tag{1}$$

$$v_{\mathrm{CM}} = v_{\mathrm{CM,LF}} + v_{\mathrm{CM,HF}} = {}^1\!/_3 \cdot (v_{\mathrm{a'o}} + v_{\mathrm{b'o}} + v_{\mathrm{c'o}}). \tag{2}$$

Fig. 2 shows simulated key waveforms of these LF and HF DM and CM voltages.

A. Analytical DM and CM Pre-Filter Noise Envelopes

Aiming for a generic comparison of the pre-filter noise emissions of voltage and current DC-link converters, low-complexity expressions that characterize the respective noise spectra are needed. Reference [24] has proposed a method for estimating the DM noise by concentrating the entire DM HF noise energy (i.e., the total HF rms noise voltage) in a single harmonic at the switching frequency, f_{sw}, and then assuming an envelope with a decay of $-20\,\mathrm{dB/dec}$ for $f > f_{\mathrm{sw}}$, see

[2]The parasitic capacitances (transistors' drain tabs to the heat sink, DC bus rails to housings, etc.) at the DC rails p and n are shorted; otherwise, these parasitic capacitors and the LISN measurement resistors would form a frequency-dependent voltage divider and result in reduced CM noise emissions. Also, the parasitic capacitances (transistors' drain tabs to the heat sink) at the AC terminals a', b' and c' are assumed to be open-circuit to eliminate possible frequency-dependent current shunt paths.

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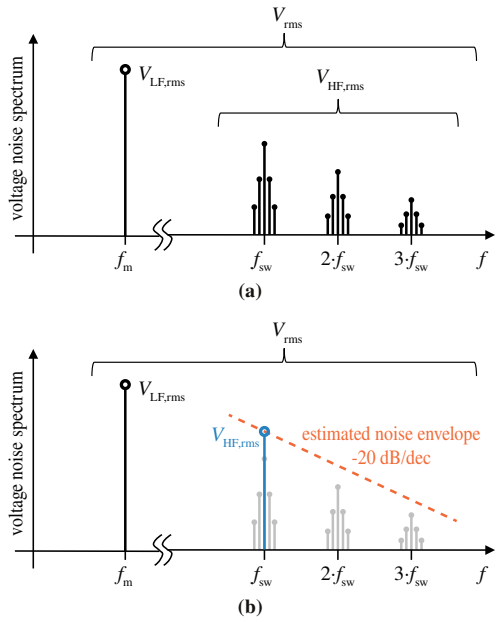

Fig. 3: **(a)** Typical rms spectrum of a switched voltage waveform including an LF fundamental component (frequency f_m) $V_{LF,rms}$ and HF harmonics $V_{HF,rms}$ at integer multiples of the switching frequency (side bands). **(b)** Simplified noise estimation method presented in [24] for single-phase converters: all HF rms noise energy is concentrated in a lumped/single harmonic $V_{HF,rms}$ at the switching frequency f_{sw} and an envelope with a slope of $-20\,\mathrm{dB/dec}$ is used for estimating noise levels for $f > f_{sw}$.

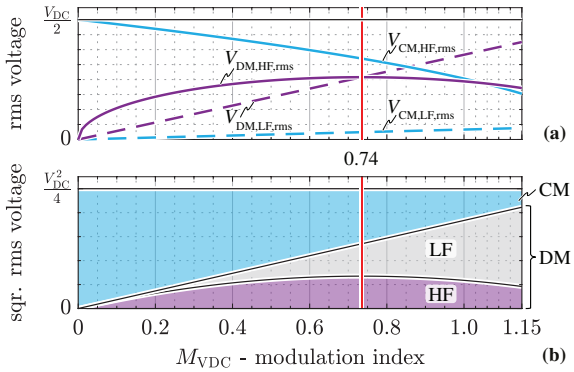

Fig. 4: **(a)** Analytical rms CM and DM voltages (both LF and HF components) of a two-level 3-Φ voltage DC-link PFC rectifier operating with varying modulation indices M_{VDC} while maintaining a constant DC-link voltage of V_{DC} to interface with different 3-Φ mains voltages. **(b)** Breakdowns of the total squared rms voltage generated by the switching stage, i.e., noise partition variation between CM and DM components, with changing M_{VDC}. Note that the peak HF DM rms voltage at $M_{VDC} = 4/(\sqrt{3}\pi) = 0.74$ (solid red line). Also note that $V^2_{CM,LF,rms}$ is too small to get noticed in **(b)**.

Fig. 3. Whereas reference [24] finds adequate accuracy when predicting DM quasi-peak (QP) emissions, we show a very good match between the simplified envelope and the amplitude spectra of the pre-filter DM and CM noise for voltage DC-link converters and, later, current DC-link converters (see **Section III**); this, in any case, is sufficient for the intended comparative analysis of the DM and CM pre-filter noise emissions generated by voltage and current DC-link systems.

The simplified analytical DM and CM noise envelopes are based on the rms values of the HF DM and CM noise voltages (see $v_{DM,HF}$ and $v_{CM,HF}$ in **Fig. 2c** and **Fig. 2f**). Therefore, analytic expressions are derived in the following. Again, taking phase a as an example, $v_{a'o}$ (see **Fig. 2a**) is a rectangular switched voltage attaining the two levels $+V_{DC}/2$ and $-V_{DC}/2$; thus

$$V_{a'o,rms} = \frac{V_{DC}}{2}, \tag{3}$$

which is independent of the modulation scheme and the modulation index. Out of the switched voltage $v_{a'o}$, an LF (i.e., fundamental frequency of 50 Hz or 60 Hz for a PFC rectifier) DM sinusoidal phase voltage $v_{DM,LF}$ (see **Fig. 2b**) is generated to interface the 3-Φ mains with a rms value of

$$V_{DM,LF,rms} = V_{a,rms} = \frac{M_{VDC}}{2\sqrt{2}} \cdot V_{DC}, \tag{4}$$

where the modulation index is defined as $M_{VDC} = {}^{2V_{ph,pk}}/_{V_{DC}}$.

Due to symmetry, one 60°-sector of a mains period (specifically, the sector where $v_a > v_b > v_c$) is selected to quantify the rms value of the generated CM voltage v_{CM}. One switching period consists of two active switching states, i.e., [100] and [110], and two zero switching states, i.e., [000] and [111].[3] Note that active states and zero states result in different CM voltage levels, i.e., $\pm V_{DC}/6$ for active states and $\pm V_{DC}/2$ for zero states. Thus, the rms CM voltage of one switching period $v_{CM,rms}(\varphi)$ at the mains angle φ is

$$v_{CM,rms}(\varphi) = \sqrt{(\delta_{100} + \delta_{110}) \cdot \frac{V_{DC}^2}{6^2} + (\delta_{111} + \delta_{000}) \cdot \frac{V_{DC}^2}{2^2}}, \tag{5}$$

where δ_{xxx} denotes the dwell time of the active or the zero switching states and varies with the mains angle φ. Finally, the rms CM voltage over one 60°-sector (equals the rms CM voltage over the entire mains period) $V_{CM,rms}$ is calculated as

$$\begin{aligned} V_{CM,rms} &= \sqrt{\frac{6}{2\pi} \int_0^{\frac{2\pi}{6}} v^2_{CM,rms}(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{1}{4} - \frac{\sqrt{3} M_{VDC}}{3\pi}} \cdot V_{DC}, \end{aligned} \tag{6}$$

with a detailed derivation in **Appendix A**.

Then, subtracting the CM and LF DM components from $v_{a'o}$ leads to the HF DM noise voltage $v_{DM,HF}$ (see **Fig. 2c**) according to (1), and thus the HF DM rms noise voltage is

$$\begin{aligned} V_{DM,HF,rms} &= \sqrt{V^2_{a'o,rms} - v^2_{DM,LF,rms} - V^2_{CM,rms}}, \\ &= \sqrt{\frac{\sqrt{3} M_{VDC}}{3\pi} - \frac{M^2_{VDC}}{8}} \cdot V_{DC}. \end{aligned} \tag{7}$$

Similarly, the HF CM noise voltage $v_{CM,HF,rms}$ (see **Fig. 2f**) is obtained by subtracting the LF CM noise $v_{CM,LF}$ from the total CM noise voltage v_{CM}. The rms value of the LF CM

[3]The switching state of the two-level 3-Φ voltage DC-link PFC rectifier is expressed by the states of three bridge legs, e.g., [100], indicating that the high-side switch $T_{a,h}$ for phase-a and the low-side switches $T_{b,l}$ and $T_{c,l}$ for phase-b and phase-c are ON.

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noise voltage can be calculated as

$$V_{\text{CM,LF,rms}} = \sqrt{\frac{6}{2\pi}\int_0^{\frac{2\pi}{6}} v_{\text{CM,LF}}^2(\varphi)\, d\varphi}, \\ = \sqrt{\frac{1}{32} - \frac{3\sqrt{3}}{56\pi}} \cdot M_{\text{VDC}} \cdot V_{\text{DC}}, \tag{8}$$

(see **Appendix A** for a detailed derivation) where the standard SVPWM injects

$$v_{\text{CM,LF}}(\varphi) = \frac{1}{2} \cdot v_{\text{b}}(\varphi), \tag{9}$$

in the selected 60°-sector ($v_{\text{a}} > v_{\text{b}} > v_{\text{c}}$). Then, the rms value of the HF CM noise voltage is

$$V_{\text{CM,HF,rms}} = \sqrt{V_{\text{CM,rms}}^2 - V_{\text{CM,LF,rms}}^2}, \\ = \sqrt{\frac{1}{4} - \frac{\sqrt{3}M_{\text{VDC}}}{3\pi} - \left(\frac{1}{32} - \frac{3\sqrt{3}}{56\pi}\right) M_{\text{VDC}}^2} \cdot V_{\text{DC}}. \tag{10}$$

Fig. 4a depicts the calculated rms CM and DM voltages (both LF and HF components) of a two-level 3-Φ voltage DC-link PFC rectifier operating with varying modulation indices M_{VDC} while maintaining a constant DC-link voltage of V_{DC} to interface with different 3-Φ mains voltages. The total squared rms voltage generated by the switching stage consistently equals $V_{\text{DC}}^2/4$, irrespective of the modulation index M_{VDC}. The variation in the noise partition between CM and DM components, which changes with different M_{VDC}, is of great interest, and is further explained by considering the total squared rms voltage and its breakdown in **Fig. 4b**.

With an increase in M_{VDC}, the dwell times of zero switching states decrease linearly, and the dwell times of active switching states increase linearly. It's noteworthy that the CM voltages generated by the zero switching states consistently surpass those of the active switching states, i.e., $\pm V_{\text{DC}}/6$ for active states and $\pm V_{\text{DC}}/2$ for zero states. Consequently, (6) indicates a linear reduction in the total (including HF and LF) squared rms CM voltages $V_{\text{CM,rms}}^2$ and, thus, a linear increase in the total squared rms DM voltages $V_{\text{DM,rms}}^2$. The LF CM voltage $V_{\text{CM,LF,rms}}$, i.e., proportional to M_{VDC} [see (8)], results in a monotonic decrease in the CM pre-filter noise $V_{\text{CM,HF,rms}}$ with an increasing M_{VDC}.

The total squared DM voltage $V_{\text{DM,rms}}^2$ shows a linear increase with M_{VDC}, and $V_{\text{DM,LF,rms}}^2$ experiences a quadratic growth [see (4)]. This leads to $V_{\text{DM,HF,rms}}^2$ taking the form of a downward-opening parabola, peaking at $M_{\text{VDC}} = 4/(\sqrt{3}\pi) = 0.74$. Importantly, this outcome remains independent of V_{DC} and can be computed using (7).

Finally, the analytical envelopes for the DM and CM pre-filter voltage spectra at frequencies $f \geq f_{\text{sw}}$ are expressed as

$$V_{\text{DM,VDC}}(f) = V_{\text{DM,HF,rms}}(V_{\text{DC}}, M_{\text{VDC}}) \cdot f_{\text{sw}}/f, \tag{11}$$

$$V_{\text{CM,VDC}}(f) = V_{\text{CM,HF,rms}}(V_{\text{DC}}, M_{\text{VDC}}) \cdot f_{\text{sw}}/f, \tag{12}$$

where the expressions for the HF rms values obtained in (7) and (10) are used, respectively.

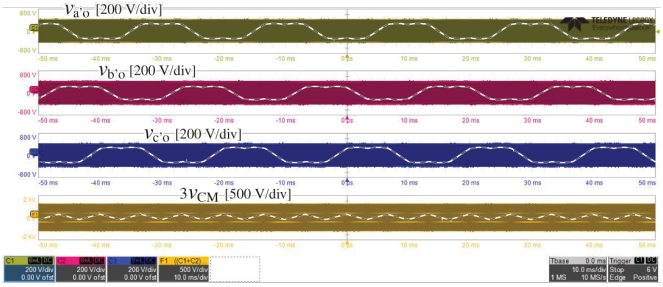

Fig. 5: Measured switch-node voltages $v_{\text{a'o}}$, $v_{\text{b'o}}$, and $v_{\text{c'o}}$, and CM voltage v_{CM} when operating the 3-Φ two-level voltage DC-link hardware demonstrator from [25] at a 400 V mains with standard SVPWM, an output voltage of 800 V, an output power of 10 kW, and a switching frequency of 100 kHz; the LF voltage components are indicated (see also **Fig. 2a** and **Fig. 2e**). The key specifications of this hardware demonstrator are listed in **Tab. I**.

B. Experimental Verification

The spectra of the DM and CM pre-filter noise voltages, $v_{\text{DM,HF}}$ and $v_{\text{CM,HF}}$, are then experimentally quantified by post-processing the measured $v_{\text{a'o}}$, $v_{\text{b'o}}$, and $v_{\text{c'o}}$ of a two-level voltage DC-link hardware demonstrator (see **Fig. 5**) using (1) and (2), and for several operating points with different DC-link voltages and hence different modulation indices. The key specifications of this hardware demonstrator are listed in **Tab. I**. **Fig. 6** shows the amplitude spectra of the measured $v_{\text{DM,HF}}$ and $v_{\text{CM,HF}}$ and compares them against the analytical envelopes from (11) and (12), respectively. Excellent agreement between the calculated envelopes and the measured amplitude spectra can be observed for the common modulation index range of $M_{\text{VDC}} = 0.8$ to $M_{\text{VDC}} = 1.0$.

Generic characteristics of the voltage DC-link rectifier's DM and CM pre-filter noise emissions can be summarized based on the derived analytical envelopes:

- The DM envelopes $V_{\text{DM,VDC}}(f)$ indicate that the DM noise emission level depends solely on the switched voltage, i.e., the DC-link voltage V_{DC} (or, equivalently, the 3-Φ input voltage $V_{\text{ph,pk}}$) and the modulation index M_{VDC} but not the output power. Since PFC rectifiers typically operate with high modulation indices within a relatively narrow range, the impact of M_{VDC} is limited, which can be clearly observed in **Fig. 6**.
- The CM envelopes $V_{\text{CM,VDC}}(f)$ reveal that the CM noise emission level is again determined by the DC-link voltage V_{DC} (or, equivalently, the 3-Φ input voltage $V_{\text{ph,pk}}$) and the modulation index M_{VDC}.
- As both DM and CM mode pre-filter noise emissions are DC-link voltage-dependent but largely independent of the power level, the total EMI noise emission, i.e., the voltage ultimately measured across the LISN resistance R_{m}, is also largely independent of the output power.

III. EMI Pre-Filter Noise Emission of Three-Phase Current DC-Link PFC Rectifier Systems

3-Φ buck-type current DC-link PFC rectifiers (see **Fig. 7a**) offer the advantage of requiring a reduced number of main magnetic components, specifically just one DC-link inductor, as opposed to three inductors on the AC side for voltage DC-link converters (see **Fig. 1a**). This allows for more compact

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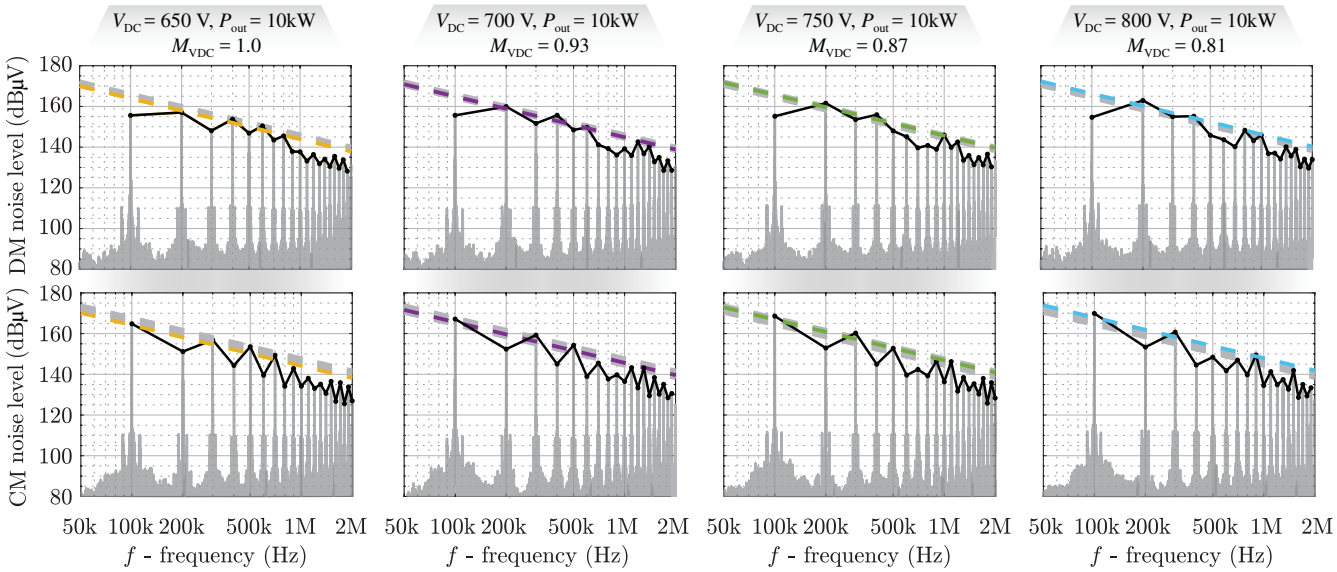

Fig. 6: DM (top row) and CM (bottom row) pre-filter noise amplitude spectra (the black solid lines indicate the envelopes of the measured spectra) extracted from measurements (see **Fig. 5**) of a 10 kW two-level 3-Φ voltage DC-link PFC rectifier interfacing a 400 V mains using different DC-link voltages V_{DC} (different modulation indices M_{VDC}) and a switching frequency of $f_{sw} = 100$ kHz. The dashed envelopes are obtained with the low-complexity analytical expressions (11) for DM and (12) for CM, and are grouped by colors according to the respective operating points; the envelopes corresponding to the respective other three operating points are shown in gray for reference.

TABLE I: System specifications the 3-Φ two-level voltage DC-link hardware demonstrator from [25].

	Description	Value
V_{in}	Rms input mains volt.	400 V
V_{DC}	DC output volt. range	650 V ... 800 V
I_{DC}	DC output current	15.4 A ... 12.5 A
M_{VDC}	Modulation index	1.0 ... 0.81
P_{out}	Output power	10 kW
f_{sw}	Switching frequency	100 kHz

hardware realization and less labor-intensive manufacturing [16]. Additionally, the 3-Φ current DC-link converter inherently generates continuous sinusoidal 3-Φ voltages, making it an attractive solution for motor inverters [20]–[22], [26].

In contrast to voltage DC-link converters, current DC-link converters typically feature a constant DC-link *current*. The switching stage consists of an upper and a lower commutation cell, each consisting of three switches with bipolar voltage-blocking capability, and AC-side commutation capacitors. Each commutation cell can route the constant DC-link current to one of the three phase terminals, resulting in the six active and three zero/freewheeling switching states shown in **Fig. 7b**. Note that these switching states correspond to *current* SVs: the desired 3-Φ sinusoidal input currents are generated by using current DC-link SVPWM to synthesize the desired input current SV $\vec{i}^*$, i.e., the DC-link current is essentially distributed to the three phases using PWM, which is further explained in **Appendix B**.

The DM and CM equivalent circuits of the switching stage are then shown in **Fig. 7c**. Taking phase a as an example, the DM behavior of the current DC-link rectifier can be modeled by the switched current pulses $i_a^{'}$, which can further be decomposed into the contributions from the upper $i_{ap}^{'}$ and the lower $i_{an}^{'}$ commutation cells. Then, the pre-filter DM EMI noise can be quantified by the voltage that appears across the LISN measurement resistor R_m as a consequence of the HF components of $i_a^{'}$ flowing through it (note that the LISN's decoupling capacitor prevents the LF components of $i_a^{'}$ from flowing through R_m), i.e.,

$$v_{DM,HF} = i_{a,HF}^{'} \cdot R_m = (i_{ap,HF}^{'} + i_{an,HF}^{'}) \cdot R_m. \qquad (13)$$

The CM voltage of the 3-Φ current DC-link PFC rectifier can be obtained from the two switch-node voltages (v_{nk} and v_{pk}) as shown in **Fig. 7c**

$$v_{CM} = 1/2 \cdot (v_{no} + v_{po}) = 1/2 \cdot (v_{nk} + v_{pk}), \qquad (14)$$

considering that the 3-Φ filter capacitor voltages are nearly equal to the 3-Φ mains voltages and the artificial neutral point (start point of filter capacitor) k can be assumed at the potential o. Note again that the worst case for the CM noise measurement is assumed by connecting the negative output terminal to PE, and, neglecting the impedance of the DC output capacitor at HF, implicitly also the positive terminal. Furthermore, considering the DM DC-link inductance L_{DC} is provided by two windings arranged on a single magnetic core with nearly ideal inverse coupling, only the leakage inductance L_σ contributes to the DC-link CM impedance, which is very low and, thus, can be neglected such that the CM noise source is directly connected to the LISN. Similar to modeling the voltage DC-link converter, this worst case for CM noise emissions is ensured by shorting the parasitic capacitances, which would be in series with the LISN measurement resistors as voltage dividers, and by disconnecting the capacitances, which would be connected in parallel to the LISN measurement resistors as current shunts. Both effects would result in reduced CM noise emissions. **Fig. 8** shows simulated key waveforms of the LF

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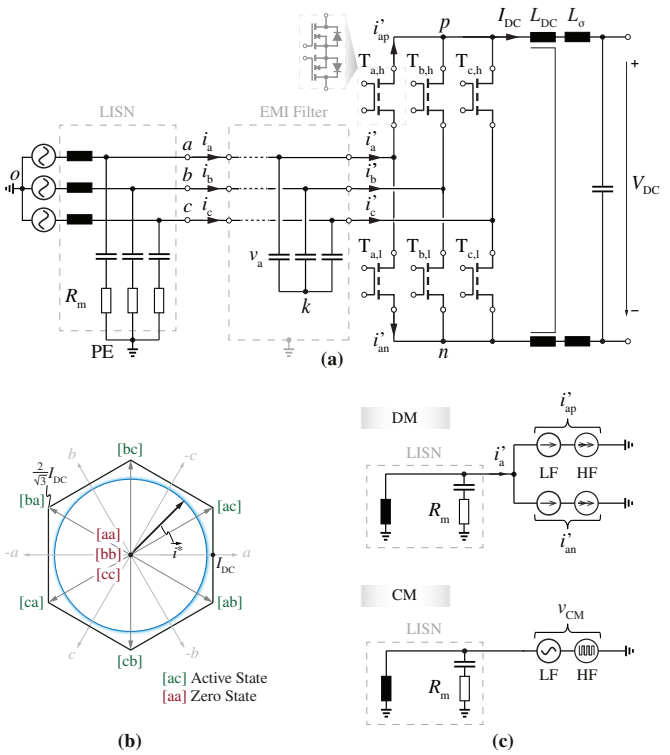

Fig. 7: **(a)** Power circuit of a 3-Φ buck-type current DC-link PFC rectifier (including an EMI filter stage where AC-side filter/commutation capacitors are shown as the first filtering components) connected to the mains via a LISN. **(b)** The rectifier's switching stage can generate six active and two zero current space vectors (SVs) at the switching nodes; the switching states are defined by the turned-on transistors of the high-side and low-side commutation cells as, for example, [ac], which indicates that the DC-link current flows through $T_{a,h}$ and returns through $T_{c,l}$, respectively. SVPWM is typically used to synthesize a desired local average input current SV $\vec{i}^*$. **(c)** DM and CM equivalent circuits where the switching stage is modeled as LF and HF current sources for DM and as LF and HF voltage sources for CM; the HF DM current sources and CM voltage sources represent the respective pre-filter noise emissions.

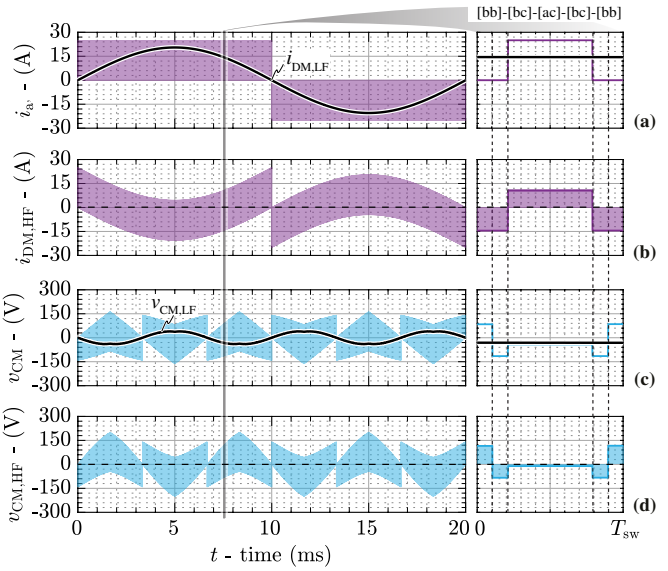

Fig. 8: Simulated key waveforms (with a zoomed view over one switching period) of the 3-Φ current DC-link PFC rectifier (see **Fig. 7a**) operating with reduced CM SVPWM from a 400 V (line-to-line rms) mains with 400 V DC output voltage, 10 kW output power, and a DC-link current of 25 A. Taking phase a as an example, **(a)** shows the total DM input current $i_{a'}$ and **(b)** its HF component $i_{DM,HF}$; **(c)** shows the total CM noise voltage v_{CM} and **(d)** its HF component $v_{CM,HF}$, i.e., **(b)** and **(d)** indicate the pre-filter DM and CM noise emissions.

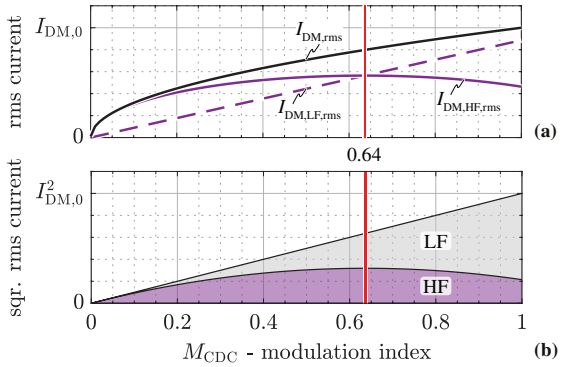

Fig. 9: **(a)** Analytical HF and LF DM rms currents of a 3-Φ current DC-link PFC rectifier interfacing a 400 V mains with varying modulation indices M_{CDC} while maintaining a constant DC-link current of I_{DC} to supply different DC output voltages. **(b)** Breakdowns of the total squared rms DM currents generated by the switching stage, i.e., the LF and HF components with different modulation indices M_{CDC}. Note that a maximum HF DM rms current is observed when $M_{CDC} = 2/\pi = 0.64$ (solid red line).

and HF DM currents and CM voltages.

A. Analytical DM and CM Pre-Filter Noise Envelopes

The same approach as used in [24] and introduced above in **Section II-A** is now applied to the current DC-link converter. Using phase a as an example, the switching stage input current $i_a^{'}$ (see **Fig. 8a**) is a switched current waveform attaining the values $+I_{DC}$, 0 (during the zero switching state [aa] for phase a), and $-I_{DC}$, i.e., three current values and not only two voltage values as was the case for the voltage DC-link system above. Thus, the total DM rms current value has to be calculated considering quarter-wave symmetry within one mains period as

$$I_{DM,rms} = i'_{a,rms} = \sqrt{\frac{2}{\pi}\int_0^{\frac{\pi}{2}} [d_a(\varphi)\cdot I_{DC}^2]\, d\varphi}, = \sqrt{\frac{2M_{CDC}}{\pi}}\cdot I_{DC}, \tag{15}$$

where $M_{CDC} = {}^{I_{ph,pk}}/_{I_{DC}}$ is the modulation index and $d_a = {}^{|i_a|}/_{I_{DC}}$ is the duty cycle of phase a, which is independent of the modulation scheme (i.e., the switching state sequence and the selection of the zero states, see below), and a detailed derivation is provided in **Appendix B**. Then, excluding the fundamental component, i.e., the desired phase current i_a from i_{DM} results in the HF DM rms current (see **Fig. 8b**)

$$I_{DM,HF,rms} = \sqrt{I_{DM,rms}^2 - i_{a,rms}^2}, = \sqrt{\frac{2M_{CDC}}{\pi} - \frac{M_{CDC}^2}{2}}\cdot I_{DC}. \tag{16}$$

Fig. 9 illustrates the analytical, i.e., using (15) and (16), LF and HF rms DM currents of a 3-Φ current DC-link PFC rectifier interfacing a 400 V mains with varying modulation indices M_{CDC} while maintaining a constant DC-link current I_{DC} to supply different DC output voltages. An increase in

M_{CDC} leads to reduced dwell times of zero switching states and, consequently, an increase in the total DM noise $I^2_{\text{DM,rms}}$ generated by the switching stage. This was not the case in the aforementioned voltage DC-link converter, where the total noise source generated by the switching stage consistently equals $V^2_{\text{DC}}/4$ (see **Fig. 4b**). $I^2_{\text{DM,rms}}$ is linearly proportional to M_{CDC}, reaching its maximum value of $I_{\text{DM},0} = \sqrt{2/\pi} I_{\text{DC}}$ at $M_{\text{CDC}} = 1$ [see (15)]. However, its LF component $I^2_{\text{DM,LF,rms}}$ is quadratically proportional to M_{CDC} [see (16)]. This results in $I^2_{\text{DM,HF,rms}}$ obtaining the shape of a downward-opening parabola, attaining its maximum at $M_{\text{CDC}} = 2/\pi = 0.64$.

The CM noise emission of the calculated 3-Φ current DC-link rectifier depends on the applied switching states, i.e., on the specific SVPWM method employed. A 30°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > 0 > v_{\text{c}}$, see **Fig. 7b**) is selected where the switching states [bb], [bc], and [ac] are used according to the implemented SVPWM with reduced CM [16], [27]. The rms CM voltage of one switching period $v_{\text{CM,rms}}(\varphi)$ at a mains angle φ is first calculated as

$$v_{\text{CM,rms}}(\varphi) = \sqrt{\delta_{\text{ac}} \cdot v^2_{\text{CM,ac}} + \delta_{\text{bc}} \cdot v^2_{\text{CM,bc}} + \delta_{\text{bb}} \cdot v^2_{\text{CM,bb}}}, \quad (17)$$

where, e.g., δ_{ac} is the dwell time of the switching state [ac] with the CM voltage of $v_{\text{CM,ac}} = (v_{\text{a}} + v_{\text{c}})/2$; v_{a} and v_{c} denote the phase voltages of the phases a and c, respectively.[4] Then, the total CM noise emission $V_{\text{CM,rms}}$ (see **Fig. 8c**) can be obtained by integrating the local average value (rms CM voltage of one switching period) over the selected 30°-sector:

$$\begin{aligned} V_{\text{CM,rms}} &= \sqrt{\frac{6}{\pi} \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} v^2_{\text{CM,rms}}(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{8\sqrt{3}-15}{8\pi} M_{\text{CDC}} + \frac{2\pi - 3\sqrt{3}}{4\pi}} \cdot V_{\text{ph,pk}}, \end{aligned} \quad (18)$$

with a detailed derivation provided in **Appendix B**.

Furthermore, the rms value of the LF CM voltage is calculated by first defining the local average (not rms) CM voltage $v_{\text{CM,LF}}(\varphi)$ as

$$v_{\text{CM,LF}}(\varphi) = \delta_{\text{ac}} \cdot v_{\text{CM,ac}} + \delta_{\text{bc}} \cdot v_{\text{CM,bc}} + \delta_{\text{bb}} \cdot v_{\text{CM,bb}}, \quad (19)$$

with a detailed derivation provided in **Appendix B**. Then, the rms value of LF CM voltage over the selected 30°-sector (same as over one mains period) becomes

$$\begin{aligned} V_{\text{CM,LF,rms}} &= \sqrt{\frac{6}{\pi} \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} v^2_{\text{CM,LF}}(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{2\pi - 3\sqrt{3}}{4\pi} - \frac{\sqrt{3}}{2\pi} M_{\text{CDC}} + \frac{12\pi - 9\sqrt{3}}{32\pi} M^2_{\text{CDC}}} \cdot V_{\text{ph,pk}}. \end{aligned} \quad (20)$$

Subtracting the LF CM voltage $v_{\text{CM,LF}}$ from the total CM voltage v_{CM} results in the HF CM noise rms voltage

$$\begin{aligned} V_{\text{CM,HF,rms}} &= \sqrt{V^2_{\text{CM,rms}} - V^2_{\text{CM,LF,rms}}}, \\ &= \sqrt{\frac{12\sqrt{3}-15}{8\pi} M_{\text{CDC}} + \frac{9\sqrt{3}-12\pi}{32\pi} M^2_{\text{CDC}}} \cdot V_{\text{ph,pk}}. \end{aligned} \quad (21)$$

Fig. 10 illustrates the analytical LF and HF rms CM voltages of a 3-Φ current DC-link PFC rectifier interfacing a 400 V mains with varying modulation indices M_{CDC} while maintaining a constant DC-link current to supply different DC output voltages. The total CM noise $V^2_{\text{CM,rms}}$ generated by the switching stage varies with the modulation indices M_{CDC} since shortened dwell times of zero switching states are needed as M_{CDC} increases; and, for the PFC operation, zero switching states contributes to larger CM noise (see **Fig. 8c**).

Furthermore, in PFC operation, active and zero switching states generate CM voltages with opposite signs (see **Appendix B**). This results in a curve of $V_{\text{CM,LF,rms}}$ exhibiting a turning point, i.e., $M_{\text{CDC}} = 8\sqrt{3}/(12\pi - 9\sqrt{3}) = 0.63$ (dashed vertical line), where it transitions from a descending to an ascending slope (see **Fig. 10**). In the range of $M_{\text{CDC}} < 0.63$, CM voltages of zero switching states dominate, such that an increased M_{CDC} results in shorter dwell times of zero switching state and reduced $V_{\text{CM,LF,rms}}$. When $M_{\text{CDC}} > 0.63$, active switching states become dominant, causing an increase in $V_{\text{CM,LF,rms}}$ with M_{CDC}. Consequently, the HF pre-filter CM voltage $V_{\text{CM,HF,rms}}$ obtains a convex shape with a maximum value at $M_{\text{CDC}} = (8\sqrt{3} - 10)/(4\pi - 3\sqrt{3}) = 0.52$ (solid red line) as shown in **Fig. 10**.

Finally, the analytical envelopes of the pre-filter DM and CM voltage spectra for frequencies $f \geq f_{\text{sw}}$ are

$$V_{\text{DM,CDC}}(f) = I_{\text{DM,HF,rms}}(I_{\text{DC}}, M_{\text{CDC}}) \cdot R_{\text{m}} \cdot f_{\text{sw}}/f, \quad (22)$$

$$V_{\text{CM,CDC}}(f) = V_{\text{CM,HF,rms}}(V_{\text{ph,pk}}, M_{\text{CDC}}) \cdot f_{\text{sw}}/f, \quad (23)$$

where the expressions for the HF rms values obtained in (16) and (21) are used, respectively; note further the multiplication with the LISN measurement resistor R_{m} in (22) as explained above in the context of (13).

TABLE II: System specifications the 3-Φ buck-type current DC-link PFC rectifier hardware demonstrator from [16].

	Description	Value
V_{in}	Rms input mains volt.	400 V
V_{DC}	DC output volt. range	300 V ... 450 V
I_{DC}	DC output current	25 A
M_{CDC}	Modulation index	0.61 ... 0.92
P_{out}	Output power	7.5 kW ... 10 kW
f_{sw}	Switching frequency	100 kHz

B. Experimental Verification

The spectra of the DM and CM EMI noise voltages i_{DM} and v_{CM} are then experimentally quantified as shown in **Fig. 11** using the hardware demonstrator of [16]. The key specifications of this hardware demonstrator are listed in **Tab. II**. Since the three AC-side filter capacitors are realized by several parallel film capacitors interconnected by copper

[4] In the switching state [ac], the lower switch node n is connected to phase c and the upper switch node p is connected to phase a; hence, $v_{\text{nk}} = v_{\text{c}}$ and $v_{\text{pk}} = v_{\text{a}}$ in (14).

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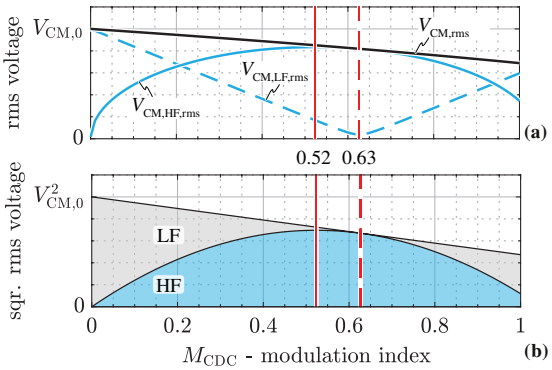

Fig. 10: (a) Analytical HF and LF CM rms voltages considering 3-Φ current DC-link PFC rectifier interfacing a 400 V mains with different modulation indices M_{CDC} and a constant DC-link current of I_{DC} to supply different DC output voltages. **(b)** illustrates the squared rms CM voltage and its breakdown into LF and HF components with different modulation indices M_{CDC}. Note that a maximum HF CM rms voltage is observed when $M_{CDC} = {}^{(8\sqrt{3}-10)}/_{(4\pi-3\sqrt{3})} = 0.52$ (solid red line) and a minimum LF CM rms voltage is attained when $M_{CDC} = {}^{8\sqrt{3}}/_{(12\pi-9\sqrt{3})} = 0.63$ (dashed red line).

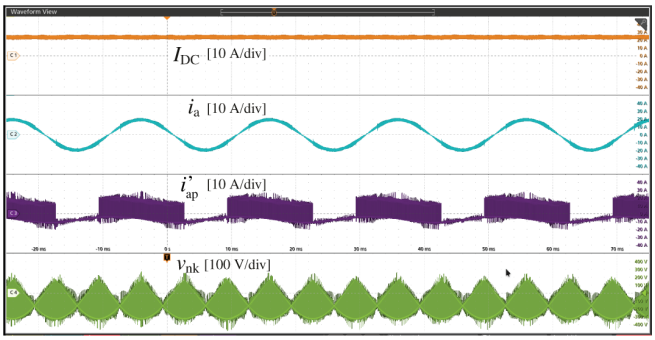

Fig. 11: Measurement results when operating the demonstrator from [16] at a 400 V mains with reduced CM SVPWM [27], an output voltage of 400 V, an output power of 10 kW, and a switching frequency of 100 kHz. In addition to the DC-link current, I_{DC}, the (filtered) input current of phase a, i_a, the switched transistor current i'_{ap} (see also **Fig. 7a**) and the voltage v_{nk} are shown. Similarly, the currents i'_{an} and the voltage v_{pk} are measured (not shown), which allows to calculate $v_{DM,HF}$ from (13) and v_{cm} from (14). Note a small phase shift between i_a and i'_{ap} due to the capacitive current flowing through the first-stage filter capacitors. The key specifications of this hardware demonstrator are listed in **Tab. II**.

planes in a printed circuit board, it is not possible to directly measure i'_a, i.e., the total phase-a input current of the switching stage. Instead, its two components (see **Fig. 7a**) contributed by the top (i'_{ap}) and the bottom (i'_{an}) commutation cells are individually measured by placing Rogowski coils (PEM CWT1BUM) around the drain legs of the transistor's TO-247 packages. These measured currents are then superimposed to obtain i'_a, and the DM pre-filter noise voltage $v_{DM,HF}$ follows from (13). The CM pre-filter noise voltage $v_{CM,HF}$ is obtained according to (14) by measuring v_{nk} and v_{pk}. **Fig. 12** shows the amplitude spectra of the experimentally obtained $v_{DM,HF}$ and $v_{CM,HF}$, and compares them against the analytical envelopes from (22) and (23), respectively. Again, excellent agreement between the analytical envelopes and the measured spectra can be observed.

Generic characteristics of the current DC-link rectifier regarding its DM and CM pre-filter noise emissions can be summarized based on the derived analytical envelopes:

- The DM envelopes $V_{DM,CDC}$ clearly show that the DM noise emission level is proportional to the DC-link current I_{DC} and depends on the modulation index M_{CDC}, i.e., it is power-dependent for a given mains voltage level.
- The CM envelopes $V_{CM,CDC}$ reveal that the CM noise emission level is proportional to the 3-Φ mains voltage $V_{ph,pk}$ and also depends on the modulation index M_{CDC}.
- Note that the CM noise levels are far (in the order of 20 dB) below the DM noise levels (see **Fig. 12**). Thus, the total EMI noise emission, i.e., the voltage ultimately measured across the LISN resistance R_m, is dominated by the DM components, which are mostly dependent on the DC-link current and/or output power [16] but not on the mains voltage; note that the voltage DC-link rectifier shows opposite characteristics (see **Section II-B**).

IV. EMI Noise Emissions Comparison

As the derived analytical approximations for DM and CM pre-filter noise emissions of both voltage DC-link and current DC-link PFC rectifiers show a close match with measurements, they enable a straightforward and generic comparison of voltage DC-link and current DC-link converters regarding the pre-filter EMI noise emissions and, consequently regarding the required EMI filter attenuation.

The DM pre-filter noise level of the voltage DC-link PFC rectifier $V_{DM,VDC}(f)$ depends on the DC-link voltage V_{DC} while the DM noise source level of the current DC-link PFC rectifier $V_{DM,CDC}(f)$ is proportional to the DC-link current I_{DC}. Considering typical modulation indices of $M_{VDC} = 1$ for the voltage DC-link PFC rectifier and of $M_{CDC} = 0.85$ for the current DC-link PFC rectifier,[5] the HF DM rms voltage $V_{DM,HF,rms}$ of voltage DC-link PFC rectifier according to (7) is

$$V_{DM,HF,rms} = \sqrt{\frac{4\sqrt{3}}{3\pi M_{VDC}} - \frac{1}{2}} \cdot V_{ph,pk} \approx 0.5 V_{ph,pk}, \qquad (24)$$

and the HF DM rms current $I_{DM,HF,rms}$ of current DC-link PFC rectifier according to (16) is

$$I_{DM,HF,rms} = \sqrt{\frac{2}{\pi M_{CDC}} - \frac{1}{2}} \cdot I_{ph,pk} \approx 0.5 I_{ph,pk}. \qquad (25)$$

Then, both rectifiers generate equal DM pre-filter noise emissions if the equivalent 3-Φ AC resistance the converter represents to the mains, i.e., $R_{AC} = {}^{V_{ph,pk}}/_{I_{ph,pk}}$, approximately equals the LISN measurement resistance R_m:

$$\begin{aligned} V_{DM,HF,rms} &= I_{DM,HF,rms} \cdot R_m \\ \Rightarrow V_{DM,HF,rms}/I_{DM,HF,rms} &= R_m, \end{aligned} \qquad (26)$$

and considering (24) and (25), we have

$$V_{DM,HF,rms}/I_{DM,HF,rms} = V_{ph,pk}/I_{ph,pk} = R_{AC} \Rightarrow R_{AC} \approx R_m. \qquad (27)$$

For higher equivalent AC resistances $R_{AC} > R_m$, i.e., lower mains current fundamentals at given mains voltage, the DM

[5]Note that the maximum modulation index without over-modulation equals $M_{VDC,max} = 2/\sqrt{3} = 1.15$ for voltage DC-link and $M_{CDC,max} = 1$ for current DC-link converter, i.e., a modulation reserve of about 15% is considered for both converters.

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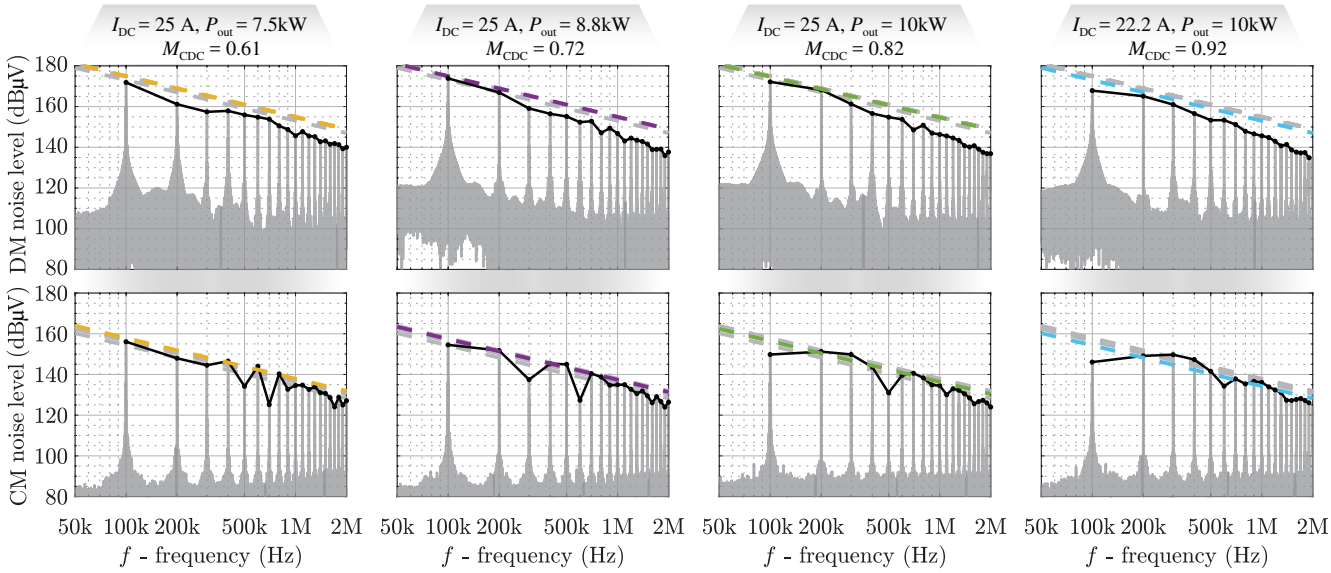

Fig. 12: DM (top row) and CM (bottom row) pre-filter noise amplitude spectra (the black solid lines indicate the envelopes of the measured spectra) extracted from measurements (see **Fig. 11**) of a 10 kW 3-Φ current DC-link PFC rectifier interfacing a 400 V mains using reduced CM SVPWM at a switching frequency of 100 kHz to supply four different output power levels with the maximum DC-link current of 25 A (hardware limitation in [16]), i.e., different modulation indices M_{CDC} are applied. The dashed envelopes are obtained with the low-complexity analytical expressions (22) for DM and (23) for CM, and are grouped by colors according to the respective operating points; the envelopes corresponding to the respective other three operating points are shown in gray for reference.

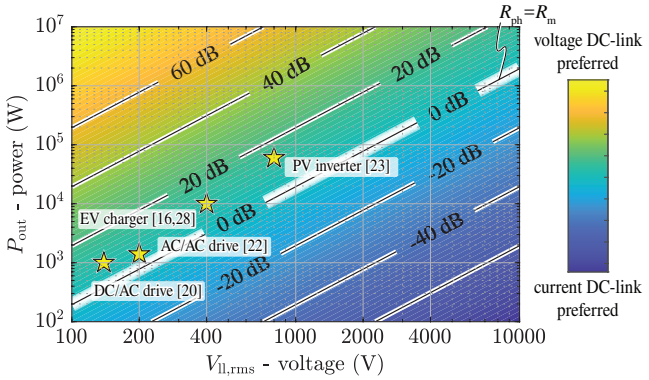

Fig. 13: Ratio of DM pre-filter noise levels of current DC-link and voltage DC-link converters in decibels, i.e., $20\log_{10}\left(V_{DM,CDC}(f)/V_{DM,VDC}(f)\right)$, in dependence of the mains line-to-line rms voltage $V_{ll,rms}$ and the output power P_{out} considering typical nominal modulation indices of $M_{VDC} = 1$ for voltage DC-link converters and of $M_{CDC} = 0.85$ for current DC-link converters.

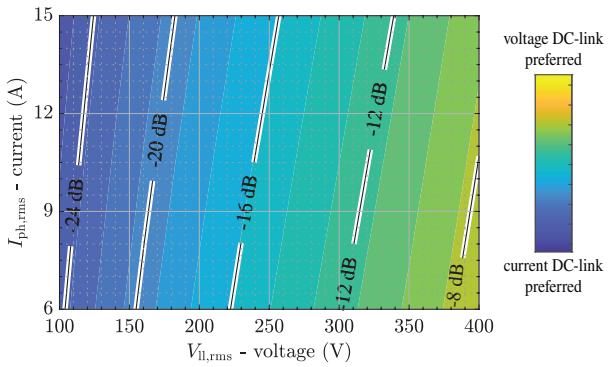

Fig. 14: Ratio of CM pre-filter noise levels of current DC-link and voltage DC-link motor drive inverters in decibels, i.e., $20\log_{10}\left(V_{CM,CDC}(f)/V_{CM,VDC}(f)\right)$ in dependence of line-to-line rms motor voltage $V_{ll,rms}$ and phase rms motor current $I_{ph,rms}$. The exemplary 10 kW motor drive system features a nominal motor voltage of 400 V (line-to-line, rms) and nominal modulation indices of $M_{VDC} = 1$ and $M_{CDC} = 0.85$. Note that a nominal constant DC-link voltage of 650 V for the voltage DC-link system and a nominal constant DC-link current of 24 A for the current DC-link system are maintained during operation with reduced AC current or voltages.

pre-filter noise emission of a current DC-link PFC rectifier is lower than that of a voltage DC-link PFC rectifier; whereas for lower AC equivalent resistance $R_{AC} < R_m$, i.e., higher mains current fundamentals at given mains voltage, the voltage DC-link PFC rectifier achieves lower DM pre-filter noise levels. Thus, **Fig. 13** shows the ratio $V_{DM,CDC}/V_{DM,VDC}$ in dependence of the mains line-to-line rms voltage $V_{ll,rms}$ and the output power P_{out}, considering $R_m = 50\,\Omega$. Generally, considering the required DM EMI filter attenuation (and hence size/effort), the voltage DC-link PFC rectifier is preferred for high-power applications at relatively low mains voltages; conversely, the current DC-link solution becomes more attractive for applications with higher mains voltages and/or lower power levels. **Fig. 13** also highlights a few current DC-link and voltage DC-link systems discussed in the recent literature for various applications, e.g., for EV charger modules [16], [28], PV inverters [23], DC/AC motor inverters [20], and AC/AC motor drives [22]. These applications exhibit system requirements resulting in $R_{AC} \approx R_m$, i.e., similar DM pre-filter noise levels and hence similar EMI filter realization effort is expected for current DC-link and voltage DC-link solutions. This underscores the importance of comprehensive, multi-dimensional comparisons between the two converter types under such scenarios.

The CM pre-filter voltage noise levels of both, voltage and current DC-link converters depend on the mains voltage and the modulation index. Assuming again typical modulation indices of $M_{VDC} = 1$ for the voltage DC-link rectifier and of

$M_{\text{CDC}} = 0.85$ for the current DC-link rectifier, the ratio of the CM noise levels when interfacing the same 3-Φ mains becomes

$$V_{\text{CM,CDC}}(f)/V_{\text{CM,VDC}}(f) = 37.7\,\% = -8.5\,\text{dB}. \tag{28}$$

This implies that the current DC-link topology, in typical cases[6], generates less CM EMI noise compared to the voltage DC-link topology. This observation is further supported by comparing the absolute values of the CM noise emission in **Fig. 6** and **Fig. 12**.

Current DC-link converters, using the modulation scheme with reduced CM noise emissions (see **Section III**), generate relatively low CM pre-filter noise compared to voltage DC-link converters, which can be explained by their respective switched CM voltage noise sources: The CM voltage levels of a voltage DC-link converter are determined solely by the DC-link voltage level (see **Fig. 2e** for the CM voltage waveforms), i.e.,

$$\pm V_{\text{DC}}/2 = \pm 325\,\text{V}, \quad \text{and} \quad \pm V_{\text{DC}}/6 = \pm 108\,\text{V},$$

considering a typical modulation index $M_{\text{VDC}} = 1$ to interface a 400 V (line-to-line rms) mains with a DC-link voltage of 650 V. However, the CM voltage levels of a current DC-link converter are determined by the 3-Φ AC input voltages (see **Appendix B**). In the selected 30°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > 0 > v_{\text{c}}$, see **Fig. 7b**), the voltage levels

$$\begin{aligned} 0\,\text{V} < v_{\text{CM,[bb]}} = v_{\text{b}} < V_{\text{ph,pk}}/2 = 163\,\text{V}, \\ -81\,\text{V} = -V_{\text{ph,pk}}/4 < v_{\text{CM,[ac]}} = (v_{\text{a}}+v_{\text{c}})/2 < 0\,\text{V}, \\ -140\,\text{V} = -\sqrt{3}V_{\text{ph,pk}}/4 < v_{\text{CM,[bc]}} = (v_{\text{b}}+v_{\text{c}})/2 < -V_{\text{ph,pk}}/4 = -81\,\text{V}, \end{aligned}$$

are attained by the CM voltage (see **Fig. 8c** for the CM voltage waveforms). Due to phase symmetry, a full mains period can be reconstructed by mirroring and/or inverting the selected 30°-sector. Therefore, analyzing only the 30°-sector is sufficient to represent the entire mains period without any loss of generality. Finally, in contrast to voltage DC-link converters, relatively low amplitudes of the CM (switched voltage) noise sources lead to low CM noise emissions of current DC-link converters.

CM noise levels are of particular interest in the context of motor drive systems, where CM currents might, for example, damage mechanical bearings [29], [30]. Therefore, **Fig. 14** compares the pre-filter CM noise levels of voltage DC-link and current DC-link systems considering an exemplary 10 kW motor drive system with a nominal motor voltage of 400 V (line-to-line, rms) and again assuming typical nominal modulation indices for the voltage DC-link converter $M_{\text{VDC}} = 1$ and the current DC-link converter $M_{\text{CDC}} = 0.85$. The figure covers the typical torque/speed (current/voltage) range of a permanent magnet synchronous motor operating with a near-unity power factor. It can be observed that the current DC-link topology generates lower CM pre-filter noise compared to the voltage DC-link topology for most operating points.

[6]Current DC-link converters typically operate using a modulation scheme that achieves a reduced CM voltage without sacrificing switching losses, a technique known as RCM SVPWM [27]. However, current DC-link converters using other modulation schemes, e.g., conventional SVPWM (see **Appendix D**), can potentially generate comparable CM pre-filter noise as voltage DC-link converters.

V. Conclusion

This paper presents a generic comparison of three-phase voltage and current DC-link converters (rectifiers or inverters) with regard to DM and CM pre-filter EMI noise emissions. The comparison is enabled by simplified analytical models for the envelopes of the DM and CM pre-filter noise emission amplitude spectra, whose accuracy is confirmed by experimental verification with 10 kW, 400 V (line-to-line rms) current DC-link and voltage DC-link demonstrator systems. For DM, the current DC-link converter shows lower pre-filter noise emissions if the equivalent AC resistance it represents to the mains is higher than the LISN's 50-Ω measurement resistor, i.e., for lower power level and/or higher mains voltages. In contrast, the current DC-link converter features significantly lower CM pre-filter noise emissions, in typical cases, which makes it an interesting option for motor drive inverters.

Appendix A - Voltage DC-link SVPWM

In the following, first, the SVPWM of voltage DC-link converters [13], [14] is briefly described, including a detailed explanation of the switching sequence within the selected 60°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > v_{\text{c}}$, see **Fig. 1b**), along with the DM and CM noise voltages associated with each switching state. Subsequently, comprehensive derivations of (6) and (8) in **Section II-A** are also provided.

I. Voltage DC-Link SVPWM

The switching state of a two-level 3-Φ voltage DC-link PFC rectifier involves the 3-Φ switching states, typically formed by three two-level bridge legs. This results in a total of six active and two zero voltage space vectors (SVs) (see **Fig. 1b**). As an example, the active switching state [100] denotes that the phase-*a* bridge leg connects to the high-side DC-link rail *p* by turning $T_{\text{a,h}}$ on and the other two phase (phase *b* and *c*) bridge legs connect to the low-side DC-link rail *n* by activating $T_{\text{b,l}}$ and $T_{\text{c,l}}$. When all three phase bridge legs are connected to the same side of the DC-link, e.g., to the high-side [111] or to the low-side [000], the zero switching state is applied. In these instances, there is no DM voltage, but a relatively large CM voltage is present, i.e., $|v_{\text{CM}}| = V_{\text{DC}}/2$ for zero switching states is larger than $|v_{\text{CM}}| = V_{\text{DC}}/6$ for active switching states. **Tab. A.1** lists the switching states for the analyzed two-level 3-Φ voltage DC-link PFC rectifier, and the DM and CM voltages can then be calculated according to (1) and (2).

To synthesize a desired 3-Φ voltage space vector $\vec{v}^*$, each switching period consists of two closest active switching states and two zero switching states. For illustration, a 60°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > v_{\text{c}}$, see **Fig. 1b**) is considered as an example, and a typical symmetric switching sequence, mirrored with respect to the center of a switching period, is applied

$$[000] \rightarrow [100] \rightarrow [110] \rightarrow [111] \rightarrow [110] \rightarrow [100] \rightarrow [000],$$

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TABLE A.1: Switching states of a two-level 3-Φ voltage DC-link PFC rectifier using the SVPWM.

S	on-state			$v_{\text{DM,a}}$	$v_{\text{DM,b}}$	$v_{\text{DM,c}}$	v_{CM}
[000]	$\text{T}_{\text{a,l}}$	$\text{T}_{\text{b,l}}$	$\text{T}_{\text{c,l}}$	0 V	0 V	0 V	$-V_{\text{DC}}/2$
[111]	$\text{T}_{\text{a,h}}$	$\text{T}_{\text{b,h}}$	$\text{T}_{\text{c,h}}$	0 V	0 V	0 V	$+V_{\text{DC}}/2$
[100]	$\text{T}_{\text{a,h}}$	$\text{T}_{\text{b,l}}$	$\text{T}_{\text{c,l}}$	$+2V_{\text{DC}}/3$	$-V_{\text{DC}}/3$	$-V_{\text{DC}}/3$	$-V_{\text{DC}}/6$
[110]	$\text{T}_{\text{a,h}}$	$\text{T}_{\text{b,h}}$	$\text{T}_{\text{c,l}}$	$+V_{\text{DC}}/3$	$+V_{\text{DC}}/3$	$-2V_{\text{DC}}/3$	$+V_{\text{DC}}/6$
[010]	$\text{T}_{\text{a,l}}$	$\text{T}_{\text{b,h}}$	$\text{T}_{\text{c,l}}$	$-V_{\text{DC}}/3$	$+2V_{\text{DC}}/3$	$-V_{\text{DC}}/3$	$-V_{\text{DC}}/6$
[011]	$\text{T}_{\text{a,l}}$	$\text{T}_{\text{b,h}}$	$\text{T}_{\text{c,h}}$	$-2V_{\text{DC}}/3$	$+V_{\text{DC}}/3$	$+V_{\text{DC}}/3$	$+V_{\text{DC}}/6$
[001]	$\text{T}_{\text{a,l}}$	$\text{T}_{\text{b,l}}$	$\text{T}_{\text{c,h}}$	$-V_{\text{DC}}/3$	$-V_{\text{DC}}/3$	$+2V_{\text{DC}}/3$	$-V_{\text{DC}}/6$
[101]	$\text{T}_{\text{a,h}}$	$\text{T}_{\text{b,l}}$	$\text{T}_{\text{c,h}}$	$+V_{\text{DC}}/3$	$-2V_{\text{DC}}/3$	$+V_{\text{DC}}/3$	$+V_{\text{DC}}/6$

with the generated DM voltage of phase *a*

$$0\,\text{V} \rightarrow {}^{2V_{\text{DC}}}\!/_{3} \rightarrow {}^{V_{\text{DC}}}\!/_{3} \rightarrow 0\,\text{V} \rightarrow {}^{V_{\text{DC}}}\!/_{3} \rightarrow {}^{2V_{\text{DC}}}\!/_{3} \rightarrow 0\,\text{V},$$

and the CM voltage

$$-{}^{V_{\text{DC}}}\!/_{2} \rightarrow -{}^{V_{\text{DC}}}\!/_{6} \rightarrow {}^{V_{\text{DC}}}\!/_{6} \rightarrow {}^{V_{\text{DC}}}\!/_{2} \rightarrow {}^{V_{\text{DC}}}\!/_{6} \rightarrow -{}^{V_{\text{DC}}}\!/_{6} \rightarrow -{}^{V_{\text{DC}}}\!/_{2}.$$

II. DM & CM Noise Source Derivation

The duty cycles of three-phase bridge legs at the mains angle φ are

$$\begin{aligned} d_{\text{a}}(\varphi) &= {}^1\!/_2 + {}^{[v_{\text{a}}(\varphi)+v_{\text{CM,LF}}(\varphi)]}\!/_{V_{\text{DC}}}, \\ d_{\text{b}}(\varphi) &= {}^1\!/_2 + {}^{[v_{\text{b}}(\varphi)+v_{\text{CM,LF}}(\varphi)]}\!/_{V_{\text{DC}}}, \\ d_{\text{c}}(\varphi) &= {}^1\!/_2 + {}^{[v_{\text{c}}(\varphi)+v_{\text{CM,LF}}(\varphi)]}\!/_{V_{\text{DC}}}, \end{aligned} \tag{A.1}$$

and in the considered 60°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > v_{\text{c}}$, see **Fig. 1b**), the LF CM injection voltage is

$$v_{\text{CM,LF}}(\varphi) = {}^1\!/_2 \cdot v_{\text{b}}(\varphi) \tag{A.2}$$

if using the standard voltage DC-link SVPWM [13], [14]. Thus, the dwell times of switching states can be derived from the obtained duty cycles of bridge legs. [000] is the only switching state where low-side switch $\text{T}_{\text{a,l}}$ of phase *a* is turned on, over one switching period, and therefore,

$$\delta_{000}(\varphi) = 1 - d_{\text{a}}(\varphi). \tag{A.3}$$

The same philosophy is applied to another zero-switching state [111], which is the only state with the on-state of $\text{T}_{\text{c,h}}$ over one switching period

$$\delta_{111}(\varphi) = d_{\text{c}}(\varphi). \tag{A.4}$$

Then, the duty cycle of phase-*b* bridge leg is applied to calculate the dwell times of the other two active switching states as

$$\begin{aligned} \delta_{110}(\varphi) &= d_{\text{b}}(\varphi) - d_{\text{c}}(\varphi), \\ \delta_{100}(\varphi) &= d_{\text{a}}(\varphi) - d_{\text{b}}(\varphi). \end{aligned} \tag{A.5}$$

Based on the obtained dwell times of each switching state, the total CM rms voltage value [see (6) in **Section II-A**] can be calculated in the considered 60°-sector of one mains period as

$$\begin{aligned} V_{\text{CM,rms}} &= \sqrt{\frac{6}{2\pi}\int_0^{\frac{2\pi}{6}} v_{\text{CM,rms}}^2(\varphi)\,d\varphi}, \\ &= \sqrt{\frac{6}{2\pi}\int_0^{\frac{2\pi}{6}} [(\delta_{100}+\delta_{110})\cdot\frac{V_{\text{DC}}^2}{6^2} + (\delta_{111}+\delta_{000})\cdot\frac{V_{\text{DC}}^2}{2^2}]\,d\varphi} \\ &= \sqrt{\frac{1}{4} - \frac{\sqrt{3}M_{\text{VDC}}}{3\pi}}\cdot V_{\text{DC}}. \end{aligned} \tag{A.6) \& (6}$$

For (8) in **Section II-A**, the rms value of the LF CM noise voltage can be calculated in the considered 60°-sector of one mains period as

$$\begin{aligned} V_{\text{CM,LF,rms}} &= \sqrt{\frac{6}{2\pi}\int_0^{\frac{2\pi}{6}} v_{\text{CM,LF}}^2(\varphi)\,d\varphi}, \\ &= \sqrt{\frac{6}{2\pi}\int_0^{\frac{2\pi}{6}} [{}^1\!/_{2^2}\cdot v_{\text{b}}^2(\varphi)]\,d\varphi}, \\ &= \sqrt{\frac{1}{32} - \frac{3\sqrt{3}}{56\pi}}\cdot M_{\text{VDC}}\cdot V_{\text{DC}}, \end{aligned} \tag{A.7) \& (8}$$

APPENDIX B - CURRENT DC-LINK SVPWM

In the following, first, the reduced CM (RCM) current DC-link SVPWM [27], [31] is briefly described, including a detailed explanation of the switching sequence within the selected 30°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > 0 > v_{\text{c}}$, see **Fig. 7b**), along with the DM and CM noise currents or voltages associated with each switching state. Subsequently, comprehensive derivations of (15), (18), and (20) in **Section III-A** are also provided.

I. Reduced CM (RCM) Current DC-Link SVPWM

The switching states of a current DC-link PFC rectifier can be categorized into active and zero (freewheeling) switching states, which are expressed by the turned-on switches in the high-side and low-side commutation cells. The active switching state [ab] indicates the DC-link current I_{DC} closing its path through $\text{T}_{\text{a,h}}$ and $\text{T}_{\text{b,l}}$, resulting in $i_{\text{a}}^{'} = +I_{\text{DC}}$ in phase *a*, $i_{\text{c}}^{'} = -I_{\text{DC}}$ in phase *c*, and $i_{\text{b}}^{'} = 0\,\text{A}$ in phase *b*. Eq. (14) provides the CM voltage of the switching state [ab], i.e., ${}^{(v_{\text{a}}+v_{\text{b}})}\!/_2$. Moreover, the zero switching state [aa] indicates the DC-link current closing its path through $\text{T}_{\text{a,h}}$ and $\text{T}_{\text{a,l}}$ resulting in zero DM currents in all three phases, but a CM voltage of v_{a} is injected. The switching states are summarized in **Tab. B.1**, together with the information on phase DM currents and the generated CM noise voltages.

To synthesize a desired 3-Φ current space vector $\vec{i}^{*}$, each switching period consists of two closest active switching states and one zero switching state. As an example, we consider a 30°-sector of one mains period ($v_{\text{a}} > v_{\text{b}} > 0 > v_{\text{c}}$, see **Fig. 7b**), where the active switching states [ac] and [bc] are used and the selection of the zero state ([aa] or [bb] or [cc]) provides a degree of freedom.

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TABLE B.1: Switching states of a 3-Φ current DC-link PFC rectifier using the RCM SVPWM.

S	**on-state**		$i_{\mathrm{a}}^{'}$	$i_{\mathrm{b}}^{'}$	$i_{\mathrm{c}}^{'}$	v_{pk}	v_{nk}	v_{CM}
[aa]	$\mathrm{T_{a,h}}$	$\mathrm{T_{a,l}}$	0 A	0 A	0 A	v_{a}	v_{a}	v_{a}
[bb]	$\mathrm{T_{b,h}}$	$\mathrm{T_{b,l}}$	0 A	0 A	0 A	v_{b}	v_{b}	v_{b}
[cc]	$\mathrm{T_{c,h}}$	$\mathrm{T_{c,l}}$	0 A	0 A	0 A	v_{c}	v_{c}	v_{c}
[ab]	$\mathrm{T_{a,h}}$	$\mathrm{T_{b,l}}$	$+I_{\mathrm{DC}}$	$-I_{\mathrm{DC}}$	0 A	v_{a}	v_{b}	$(v_{\mathrm{a}}+v_{\mathrm{b}})/2$
[ba]	$\mathrm{T_{b,h}}$	$\mathrm{T_{a,l}}$	$-I_{\mathrm{DC}}$	$+I_{\mathrm{DC}}$	0 A	v_{b}	v_{a}	$(v_{\mathrm{a}}+v_{\mathrm{b}})/2$
[bc]	$\mathrm{T_{b,h}}$	$\mathrm{T_{c,l}}$	0 A	$+I_{\mathrm{DC}}$	$-I_{\mathrm{DC}}$	v_{b}	v_{c}	$(v_{\mathrm{b}}+v_{\mathrm{c}})/2$
[cb]	$\mathrm{T_{c,h}}$	$\mathrm{T_{b,l}}$	0 A	$-I_{\mathrm{DC}}$	$+I_{\mathrm{DC}}$	v_{c}	v_{b}	$(v_{\mathrm{b}}+v_{\mathrm{c}})/2$
[ca]	$\mathrm{T_{c,h}}$	$\mathrm{T_{a,l}}$	$-I_{\mathrm{DC}}$	0 A	$+I_{\mathrm{DC}}$	v_{c}	v_{a}	$(v_{\mathrm{a}}+v_{\mathrm{c}})/2$
[ac]	$\mathrm{T_{a,h}}$	$\mathrm{T_{c,l}}$	$+I_{\mathrm{DC}}$	0 A	$-I_{\mathrm{DC}}$	v_{a}	v_{c}	$(v_{\mathrm{a}}+v_{\mathrm{c}})/2$

In this paper, the zero state is determined by the phase with the minimum voltage, i.e., phase *b* in the analyzed sector. This modulation scheme is made to achieve a reduced CM voltage without sacrificing switching losses, a technique known as RCM SVPWM [27]. Importantly, this method also advantageously facilitates the integrated CM filter by ensuring a continuous LF CM voltage without any voltage step at the sector boundary. Thus, considering one switching period in the analyzed sector (see **Fig. 8**), the switching sequence is

$$[\mathrm{bb}] \rightarrow [\mathrm{bc}] \rightarrow [\mathrm{ac}] \rightarrow [\mathrm{bc}] \rightarrow [\mathrm{bb}],$$

the DM current noise of phase *a* is

$$0\,\mathrm{A} \rightarrow 0\,\mathrm{A} \rightarrow I_{\mathrm{DC}} \rightarrow 0\,\mathrm{A} \rightarrow 0\,\mathrm{A},$$

and the generated CM voltage is

$$v_{\mathrm{b}} \rightarrow {}^{(v_{\mathrm{b}}+v_{\mathrm{c}})}\!/_{2} \rightarrow {}^{(v_{\mathrm{a}}+v_{\mathrm{c}})}\!/_{2} \rightarrow {}^{(v_{\mathrm{b}}+v_{\mathrm{c}})}\!/_{2} \rightarrow v_{\mathrm{b}}.$$

Note that, for the PFC operation, CM voltages of the active switching states and the zero switching states have the opposite sign, e.g., in the selected sector where $v_{\mathrm{a}} > v_{\mathrm{b}} > 0 > v_{\mathrm{c}}$

$$v_{\mathrm{b}} > 0 > {}^{(v_{\mathrm{a}}+v_{\mathrm{c}})}\!/_{2} > {}^{(v_{\mathrm{b}}+v_{\mathrm{c}})}\!/_{2}$$

is obtained. This explains the shape of $V_{\mathrm{CM,LF,rms}}$ exhibiting a turning point, where it transitions from a descending to an ascending slope (see **Fig. 10a**).

II. DM & CM Noise Source Derivation

The 3-Φ duty cycles at the mains angle φ are:

$$\begin{aligned} d_{\mathrm{a}}(\varphi) &= {}^{|i_{\mathrm{a}}(\varphi)|}\!/_{I_{\mathrm{DC}}} = M_{\mathrm{CDC}} \cdot |\cos(\varphi)|, \\ d_{\mathrm{b}}(\varphi) &= {}^{|i_{\mathrm{b}}(\varphi)|}\!/_{I_{\mathrm{DC}}} = M_{\mathrm{CDC}} \cdot |\cos(\varphi - 2/3\pi)|, \\ d_{\mathrm{c}}(\varphi) &= {}^{|i_{\mathrm{c}}(\varphi)|}\!/_{I_{\mathrm{DC}}} = M_{\mathrm{CDC}} \cdot |\cos(\varphi + 2/3\pi)|, \end{aligned} \tag{B.1}$$

and in the selected 30°-sector of one mains period ($v_{\mathrm{a}} > v_{\mathrm{b}} > 0 > v_{\mathrm{c}}$, see **Fig. 7b**), dwell time of three switching states are

$$\begin{aligned} \delta_{\mathrm{ac}}(\varphi) &= d_{\mathrm{a}}(\varphi), \\ \delta_{\mathrm{bc}}(\varphi) &= d_{\mathrm{b}}(\varphi), \\ \delta_{\mathrm{bb}}(\varphi) &= 1 - d_{\mathrm{a}}(\varphi) - d_{\mathrm{b}}(\varphi). \end{aligned} \tag{B.2}$$

Based on the obtained dwell times of each switching state, the total DM rms current value [see (15) in **Section III-A**] can be calculated considering quarter-wave symmetry within one mains period as

$$\begin{aligned} I_{\mathrm{DM,rms}} = i_{\mathrm{a,rms}}^{'} &= \sqrt{\frac{2}{\pi}\int_{0}^{\frac{\pi}{2}} [d_{\mathrm{a}}(\varphi) \cdot I_{\mathrm{DC}}^{2}]\, d\varphi}, \\ &= \sqrt{\frac{2}{\pi} M_{\mathrm{CDC}} \cdot I_{\mathrm{DC}}^{2} \cdot \int_{0}^{\frac{\pi}{2}} \cos(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{2M_{\mathrm{CDC}}}{\pi}} \cdot I_{\mathrm{DC}}. \end{aligned} \tag{B.3) \& (15}$$

For (18) in **Section III-A**, the total DM rms current value can be calculated over the selected 30°-sector as

$$\begin{aligned} V_{\mathrm{CM,rms}} &= \sqrt{\frac{6}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} v_{\mathrm{CM,rms}}^{2}(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{6}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} [\delta_{\mathrm{ac}} \cdot (\frac{v_{\mathrm{a}}+v_{\mathrm{c}}}{2})^{2} + \delta_{\mathrm{bc}} \cdot (\frac{v_{\mathrm{b}}+v_{\mathrm{c}}}{2})^{2} + \delta_{\mathrm{bb}} \cdot v_{\mathrm{b}}^{2}]\, d\varphi}, \\ &= \sqrt{\frac{8\sqrt{3}-15}{8\pi} M_{\mathrm{CDC}} + \frac{2\pi - 3\sqrt{3}}{4\pi}} \cdot V_{\mathrm{ph,pk}}. \end{aligned} \tag{B.4) \& (18}$$

For (20) in **Section III-A**, the rms value of LF CM voltage over the selected 30°-sector (same as over one mains period) becomes

$$\begin{aligned} V_{\mathrm{CM,LF,rms}} &= \sqrt{\frac{6}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} v_{\mathrm{CM,LF}}^{2}(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{6}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} [\delta_{\mathrm{ac}} \cdot (\frac{v_{\mathrm{a}}+v_{\mathrm{c}}}{2}) + \delta_{\mathrm{bc}} \cdot (\frac{v_{\mathrm{b}}+v_{\mathrm{c}}}{2}) + \delta_{\mathrm{bb}} \cdot v_{\mathrm{b}}]^{2}\, d\varphi}, \\ &= \sqrt{\frac{2\pi - 3\sqrt{3}}{4\pi} - \frac{\sqrt{3}}{2\pi} M_{\mathrm{CDC}} + \frac{12\pi - 9\sqrt{3}}{32\pi} M_{\mathrm{CDC}}^{2}} \cdot V_{\mathrm{ph,pk}}. \end{aligned} \tag{B.5) \& (20}$$

APPENDIX C - PRE-FILTER NOISE ENVELOPES OF OTHER VOLTAGE DC-LINK PWMS

This Appendix analyzes the applicability of the low-complexity analytical pre-filter noise envelopes from (11) for DM and (12) for CM noise emissions, which are derived in **Section II-A**, to the voltage DC-link converter modulated by PWM schemes other than the standard SVPWM. A discontinuous SVPWM (*DPWM*) is taken as an example, where the phase with the maximum absolute voltage is always clamped (i.e., the corresponding half-bridge is not switched during the corresponding interval), and, accordingly, either [111] or [000] is selected as the zero state within a given switching period. To synthesize a desired voltage space vector $\vec{v}^{*}$, the switching state sequence of each switching period is composed of the two closest active switching states and one zero switching state. For illustration, a 60°-sector of one mains period where phase c retains the minimum phase voltage is considered as an example, and a typical symmetric switching sequence,

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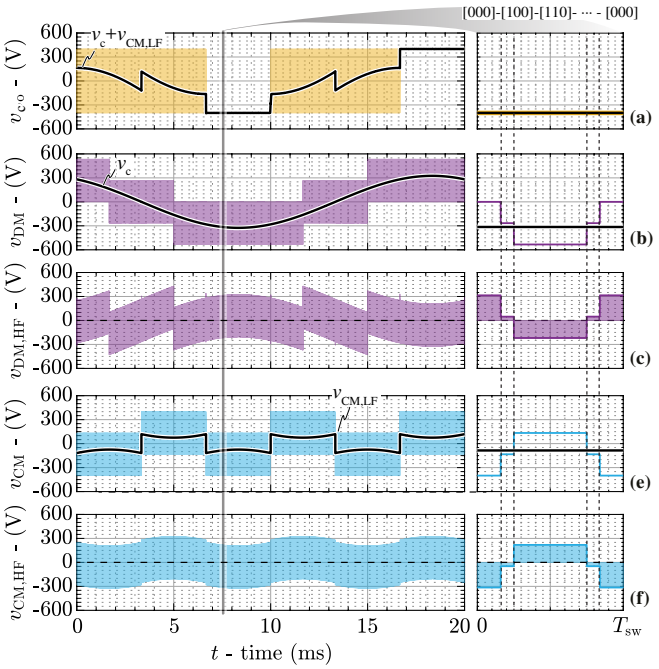

Fig. 15: Simulated key waveforms (with a zoomed view over one switching period) of the two-level 3-Φ voltage DC-link PFC rectifier (see **Fig. 1a**) operating with a 400 V (line-to-line rms) mains, 800 V DC-link and/or output voltage, and 10 kW output power using discontinuous SVPWM (DPWM). Taking phase c as an example, **(a)** shows the switching stage phase voltage $v_{c'o}$, which can be decomposed into **(b)** DM and **(e)** CM components. Furthermore, **(c)** and **(f)** show the DM and CM HF noise voltages (i.e., the pre-filter DM and CM noise emissions). Note that the phase with the maximum absolute voltage, i.e., phase c in the selected sector, is clamped during the entire sector, which is achieved by a suitable LF CM injection $v_{CM,LF}$, and hence the corresponding bridge leg is not switching within the switching period (only the first half of one switching period is shown in the zoomed view due to the switching sequence symmetry).

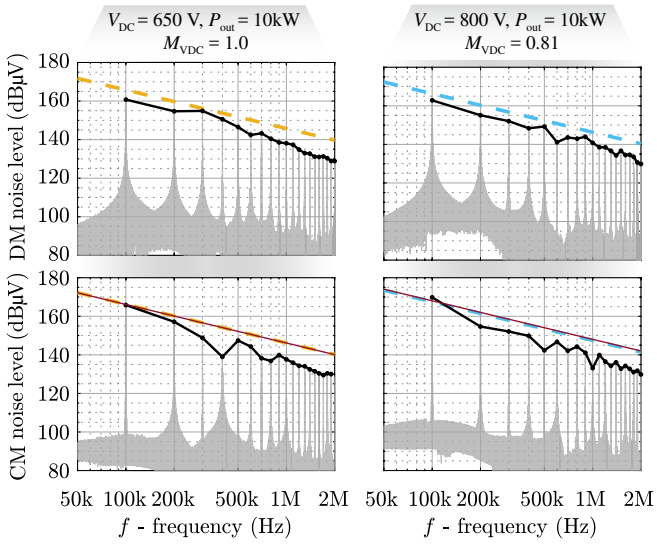

Fig. 16: DM (top row) and CM (bottom row) pre-filter noise amplitude spectra (the black solid lines indicate the envelopes of the measured spectra) extracted from circuit simulations of a 10 kW two-level 3-Φ voltage DC-link PFC rectifier modulated by DPWM. The rectifier interfaces a 400 V mains using different DC-link voltages V_{DC} (different modulation indices M_{VDC}) and a switching frequency of $f_{sw} = 100$ kHz. The envelopes are obtained with the low-complexity analytical expressions (11) for DM and (12) for CM, respectively. Note that the dashed lines represent the analytical pre-filter noise envelopes derived in **Section II-A**, which are grouped by colors according to the respective operating points. As a comparison, the CM noise envelopes specifically derived for the DPWM in **Appendix C** are shown in red solid lines; the DM noise envelopes are identical for both PWM schemes.

mirrored with respect to the center of a switching period, is applied:

$$[000] \rightarrow [100] \rightarrow [110] \rightarrow [110] \rightarrow [100] \rightarrow [000].$$

In the selected sector, phase c bridge leg is always connected to the low-side DC rail n during one switching period, as only [000] (see **Fig. 15**, and not also [111] as in conventional SVPWM shown in **Fig. 2**) is applied as the zero state.

The analytical envelopes derived for the conventional SVPWM (see (7) and (10) in **Section II-A**) are first applied to estimate the amplitude spectra of the simulated $v_{DM,HF}$ and $v_{CM,HF}$ using the DPWM as shown in **Fig. 16**. Excellent agreement between the analytical envelopes and the simulated amplitude spectra can be observed for the exemplary modulation indices of $M_{VDC} = 0.8$ and $M_{VDC} = 1.0$. This can be explained with **Fig. 4**, where, regardless of M_{VDC}, $V_{CM,LF,rms}$ always contributes a small part and $V^2_{CM,LF,rms}$ is even too small to get noticed. Therefore, without losing accuracy, the analytical envelopes from (7) and (10) can be directly applied to voltage DC-link converters modulated by other PWM schemes, i.e., with different injected LF CM voltages.

Furthermore, to highlight the generality of the modeling method proposed in [24] and utilized herein, the low-complexity analytical expressions for the pre-filter noise envelopes resulting for DPWM shown in **Fig. 15** are specifically derived hereafter. Since the difference between the considered DPWM and the standard SVPWM only lies in the relative shares of two zero states ([000] and [111]), $V_{a'o,rms}$ in (3), $V_{DM,LF,rms}$ in (4), $V_{CM,rms}$ in (6), and $V_{DM,HF,rms}$ in (7) remain as derived in **Section II-A**. A CM voltage

$$v_{CM,LF}(\varphi) = -\frac{1}{2}V_{DC} - v_c(\varphi), \tag{C.1}$$

is injected to ensure that phase c bridge leg is always connected to the low-side DC rail n in the selected sector, and thus,

$$\begin{aligned} V_{CM,LF,rms} &= \sqrt{\frac{3}{\pi}\int_{\frac{6}{\pi}}^{\frac{\pi}{2}} v^2_{CM,LF}(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{1}{4} - \frac{3}{2\pi}M_{VDC} + \frac{2\pi+3\sqrt{3}}{16\pi}M^2_{VDC}}\cdot V_{DC}. \end{aligned} \tag{C.2}$$

Then, the rms value of the HF CM noise voltage is

$$\begin{aligned} V_{CM,HF,rms} &= \sqrt{V^2_{CM,rms} - V^2_{CM,LF,rms}}, \\ &= \sqrt{\frac{9-2\sqrt{3}}{6\pi}M_{VDC} - \frac{3\sqrt{3}+2\pi}{16\pi}M^2_{VDC}}\cdot V_{DC}. \end{aligned} \tag{C.3}$$

Fig. 16 shows the obtained envelopes (red solid lines) and compares them against the analytical envelopes using (10), resulting in a negligible difference.

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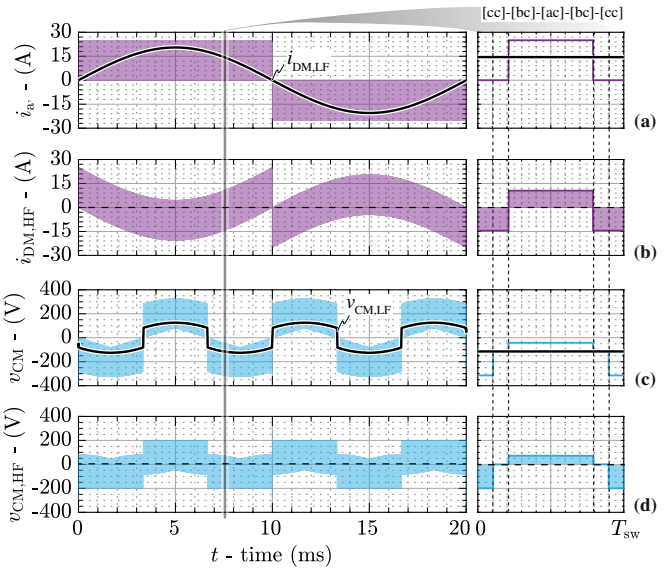

Fig. 17: Simulated key waveforms (with a zoomed view over one switching period) of the 3-Φ current DC-link PFC rectifier (see **Fig. 7a**) operating with the conventional SVPWM, i.e., using the phase with the maximum absolute voltage as the zero state instead of the phase with the minimum absolute voltage in the RCM SPWM (see **Fig. 8**), from a 400 V (line-to-line rms) mains with 400 V DC output voltage, 10 kW output power, and a DC-link current of 25 A. Taking phase a as an example, **(a)** shows the total DM input current $i_{a'}$ and **(b)** its HF component $i_{DM,HF}$; **(c)** shows the total CM noise voltage v_{CM} and **(d)** its HF component $v_{CM,HF}$.

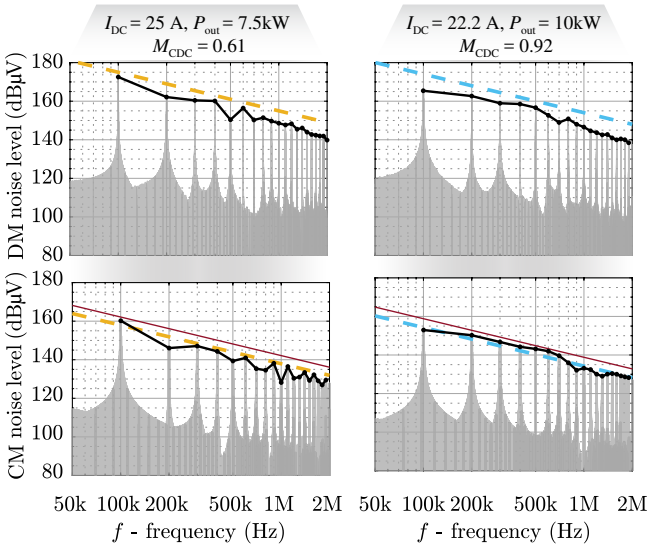

Fig. 18: DM (top row) and CM (bottom row) pre-filter noise amplitude spectra (the black solid lines indicate the envelopes of the measured spectra) extracted from circuit simulations of a 10 kW 3-Φ current DC-link PFC rectifier modulated by the conventional SVPWM. The rectifier interfaces a 400 V mains using a switching frequency of 100 kHz with different modulation indices M_{CDC} (i.e., different power levels). The envelopes (dashed) are obtained with the low-complexity analytical expressions (16) for DM and (21) for CM, respectively as derived in **Section III-A** for the RCM SVPWM, which are grouped by colors according to the respective operating points. As a comparison, the CM noise envelopes specifically derived for the conventional SVPWM in **Appendix D** are shown as red solid lines; the DM noise envelopes are identical for both PWM schemes.

Appendix D - Pre-Filter Noise Envelopes of Other Current DC-Link PWMs

This Appendix analyzes the applicability of the derived low-complexity analytical pre-filter noise envelopes from (16) for DM and (21) for CM noise emissions to other current DC-link PWM schemes. The conventional current DC-link SVPWM is selected as a representative example, which generates the same DM but higher CM noise emissions compared to the reduced-CM (RCM) SVPWM considered in **Section III-A**.

To synthesize a desired current space vector $\vec{i}^*$, the switching state sequence of each switching period is composed of the two closest active switching states and one zero switching state. As an example, we consider a 30°-sector of one mains period ($v_a > v_b > 0 > v_c$, see **Fig. 7b**), where the same active switching states [ac] and [bc] are used as in the RCM SVPWM but the zero state [cc] instead of [bb] is selected in the conventional SVPWM. Thus, considering one switching period in the analyzed sector (see **Fig. 7b**), the switching sequence is

$$[\text{cc}] \rightarrow [\text{bc}] \rightarrow [\text{ac}] \rightarrow [\text{bc}] \rightarrow [\text{cc}].$$

The selection of the zero states has no impact on the total DM input current $i_{a'}$ and its HF component $i_{DM,HF}$ (cf. **Fig. 8** and **Fig. 17**). Thus, $I_{DM,rms}$ in (15), and $I_{DM,HF,rms}$ in (16) derived in **Section III-A** can be directly applied, and the same holds for the DM pre-filter noise envelopes (see **Fig. 18**). For CM components, since the zero state is the main contributor to the CM noise emission in the current DC-link converter, the rms CM voltage of one switching period $v_{CM,rms}(\varphi)$ at a mains angle φ has to be recalculated as

$$v_{CM,rms}(\varphi) = \sqrt{\delta_{ac} \cdot v_{CM,ac}^2 + \delta_{bc} \cdot v_{CM,bc}^2 + \delta_{cc} \cdot v_{CM,cc}^2}, \tag{D.1}$$

where δ_{cc} is the dwell time of the zero switching state [cc] with the CM voltage of $v_{CM,cc} = v_c$. Then, the total CM noise emission $V_{CM,rms}$ can be obtained by integrating the local average value (rms CM voltage of one switching period) over the selected 30°-sector:

$$\begin{aligned} V_{CM,rms} &= \sqrt{\frac{6}{\pi} \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} v_{CM,rms}^2(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{2\pi + 3\sqrt{3}}{4\pi} - \frac{21}{8\pi} M_{CDC}} \cdot V_{ph,pk}. \end{aligned} \tag{D.2}$$

Furthermore, the rms value of the LF CM voltage is recalculated by first defining the local average (not rms) CM voltage $v_{CM,LF}(\varphi)$ as

$$v_{CM,LF}(\varphi) = \delta_{ac} \cdot v_{CM,ac} + \delta_{bc} \cdot v_{CM,bc} + \delta_{cc} \cdot v_{CM,cc}. \tag{D.3}$$

Then, the rms value of LF CM voltage over the selected 30°-sector (same as over one mains period) becomes

$$\begin{aligned} V_{CM,LF,rms} &= \sqrt{\frac{6}{\pi} \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} v_{CM,LF}^2(\varphi)\, d\varphi}, \\ &= \sqrt{\frac{2\pi + 3\sqrt{3}}{4\pi} - \frac{9}{2\pi} M_{CDC} + \frac{9}{16} M_{CDC}^2} \cdot V_{ph,pk}. \end{aligned} \tag{D.4}$$

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Subtracting the LF CM voltage $v_{\text{CM,LF,}}$ from the total CM voltage v_{CM} results in the HF CM noise rms voltage

$$\begin{aligned} V_{\text{CM,HF,rms}} &= \sqrt{V_{\text{CM,rms}}^2 - V_{\text{CM,LF,rms}}^2}, \\ &= \sqrt{\frac{15}{8\pi} M_{\text{CDC}} - \frac{9}{16} M_{\text{CDC}}^2} \cdot V_{\text{ph,pk}}. \end{aligned} \tag{D.5}$$

Fig. 18 shows the amplitude spectra of the simulated $v_{\text{CM,HF}}$ using the conventional (not RCM) current DC-link SVPWM and compares them against the pre-filter noise envelope from (21) calculated in **Section III-A** (i.e., for the RCM SVPWM) and the pre-filter noise envelope from (D.5) calculated here specifically for the conventional SVPWM. Applying the conventional current DC-link SVPWM results in a slight increase of the emission level by $5\,\text{dB}\mu\text{V}$ compared to RCM SVPWM, which is fully captured by the updated calculations presented here. Further, as the increase is small, employing conventional current DC-link SVPWM instead of RCM SVPWM would not change the comparative analysis and the obtained conclusion in **Section IV**. **explain the dashed connection**

Appendix E - DM and CM Equivalent Circuit Derivations

This Appendix first derives an equivalent circuit of a DC/DC boost converter (see **Fig. 19a**) to provide a basis for the explanation of the DM and CM equivalent circuits of three-phase voltage DC-link converters shown in **Fig. 1c**. Then, we derive an equivalent circuit for a DC/DC buck converter (see **Fig. 19b**) to explain the DM and CM equivalent circuits of three-phase current DC-link converters shown in **Fig. 7c**, which follows the duality principle [11]. The modeling methods implemented for both voltage and current DC-link converters advantageously allow full degrees of freedom in optimizing the EMI filter volume and/or power loss. This means that all the passive components belonging to the EMI filter, especially the input inductor of the boost converter and the input capacitor of the buck converter, are degrees of freedom to minimize the total volume and/or power losses of the EMI filter [32].

Fig. 19a shows a DC/DC boost converter and its equivalent circuits. The converter comprises three main sections (see **Fig. 19a.i**): the input-side EMI filter, the switching stage, and the output-side voltage DC-link (DC-link capacitor). Depend-ing on the switch position (i.e., the state of the switching stage), the output voltage V_{out} or zero volts are applied to the switch node, generating a switched voltage v_{sw}. On the other hand, again depending on the switch position, the switching stage output current i_{sw} either equals the inductor current i_{L} or zero, i.e., can be represented by a switched current source. To derive a simplified equivalent circuit, therefore the switching stage is replaced by two equivalent noise sources (see **Fig. 19a.ii**): a switched voltage noise source connected to the input and a switched current source connected to the output. The single mixed-mode voltage noise source is then further decomposed into DM and CM noise sources (see **Fig. 19a.iii**) for analytical EMI noise source modeling. A two-level 3-Φ voltage DC-link PFC rectifier (see **Fig. 1a**) can be synthesized from three individual DC/DC boost converters.

Thus, **Section II** employs switched voltage noise sources to model the analytical AC-side EMI pre-filter noise emissions of the voltage DC-link converter as shown in **Fig. 1c**.

Fig. 19b illustrates a DC/DC buck converter and its equivalent circuits. Again, the converter consists of three main sections: the input-side EMI filter, the switching stage, and the output-side current DC-link (DC-link inductor), as shown in **Fig. 19b.i**. Note the duality between the boost converter discussed above and the buck converter. A switched current i_{sw} appearing at the interface between the EMI filter and the switching stage is, depending on the switch position, either equal to the output inductor current i_{L} or zero. The voltage at that interface, in contrast, is given by the input EMI filter capacitor and hence continuous, whereas a switched voltage v_{sw} (equals to the EMI filter capacitor voltage V_{in} or zero, depending on the switch position) appears at the interface between switching stage and buck inductor (current DC-link). To derive a simplified equivalent circuit, the switching stage is again replaced by two noise sources (see **Fig. 19b.ii**): a switched current noise source connected to the input and a switched voltage source connected to the output. The single mixed-mode voltage noise source can also be decomposed into DM and CM noise sources (see **Fig. 19b.iii**). The switched current noise, directly emitting towards the input port, is the model of the DM noise source. This allows the buck capacitor to be considered as the first component in the EMI filter optimization [32], [33]. The switched CM voltage source is used to represent the CM noise emission, which is similar to the DC/DC boost converter; however, it actes on the converter output and not the input side. A two-level 3-Φ current DC-link PFC rectifier (see **Fig. 7a**) can be synthesized from three individual DC/DC buck converters. Thus, switched DM current and switched CM voltage noise sources are applied to model the analytical EMI pre-filter noise emissions of the current DC-link converter in **Section III** and **Fig. 7c**. A similar modeling approach of current DC-link converters can be found in [33] (**Fig. 3**) and [15] (**Fig. 11**).

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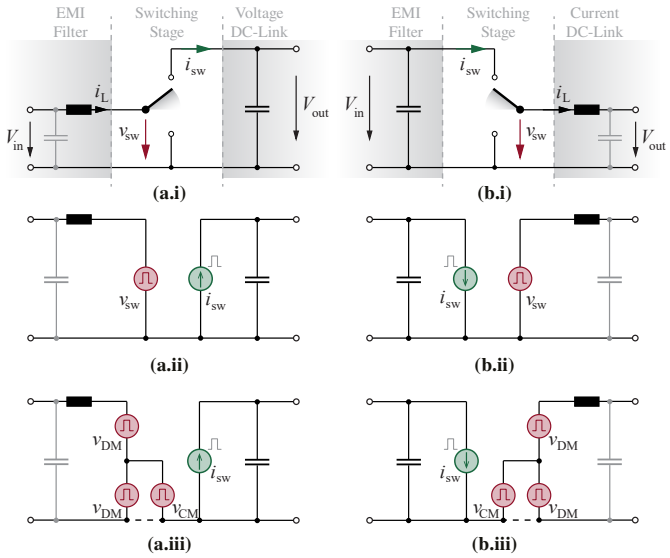

Fig. 19: Derivation of equivalent circuits of the switching stages of **(a)** a DC/DC boost converter (i.e., essentially a voltage DC-link converter) and **(b)** a DC/DC buck converter (i.e., essentially a current DC-link converter). The equivalent circuits do not include or modify any of the passive elements, thereby ensuring the maximum degrees of freedom in optimizing the EMI filter. The DM noise emitted towards the boost converter input can be modeled by a switched voltage source, whereas the DM noise emitted towards the buck converter input can be modeled by a switched current source, which follows the duality principle [11]. The CM noise, in both cases, is best modeled by a switched voltage source.

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