Power Electronic Systems
Laboratory

IEEE Transactions on Power Electronics, Vol. 38, No. 4, pp. 4195-4202, April 2023

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This article has been accepted for publication in IEEE Transactions on Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2022.3222236

Three-Phase Synergetically Controlled Current DC-Link AC/DC Buck-Boost Converter with Two Independently Regulated DC Outputs

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***Abstract*—A three-phase current DC-link AC/DC buck-boost converter, composed of a three-phase current-source rectifier (CSR) front-end and a three-level DC/DC-stage, can provide two independently regulated DC outputs. A conventional synergetic control strategy, which coordinates the modulation of the CSR and the DC/DC converter stage to achieve minimum overall switching losses, is extended to the case of two independent DC outputs, retaining all advantageous features such as seamless transitions between operating modes and modulation schemes. The extended synergetic control strategy allows loss-optimum operation (i.e., reduced number of switching instants due to clamping of a phase of the CSR-stage (switching only two out of the three phases, i.e., 2/3-PWM) or individual clamping of the DC/DC-stage's two half-bridges, and minimum possible DC-link current) for any operating point, especially also for two *different* output voltages and/or two *different* loads. Finally, experimental confirmation of the proposed control scheme using a $10\,\mathrm{kW}$ demonstrator system is provided. Operating in the boost-mode at a total output voltage of $800\,\mathrm{V}$, the proposed synergetic control achieves a significant measured efficiency improvement over a wide load range, e.g., from $95.7\,\%$ to $96.9\,\%$ ($1.2\,\%$) at $2\,\mathrm{kW}$ and from $97.9\,\%$ to $98.4\,\%$ ($0.5\,\%$) at $10\,\mathrm{kW}$, which is largely independent of output voltage asymmetries and load asymmetries.**

***Index Terms*—Three-Phase Buck-Boost Current DC-Link PFC Rectifier, Two Independent DC Outputs, Synergetic DC-Link Current Control, Two-Third Pulse-Width Modulation.**

I. Introduction

The availability of two independently regulated DC outputs presents a considerable cost-saving potential for advanced three-phase (3-Φ) Power Factor Corrected (PFC) AC/DC converter systems that supply separate loads, e.g., high-power heaters for different process stages [1], or chargers of future high-voltage batteries for heavy-duty electric vehicles [2], which could advantageously be split into upper and lower halves [3]. Recently, research on fully controllable hybrid or monolithic bidirectional bipolar switches [4], [5] has triggered renewed interest in current DC-link systems [6]–[10]. Compared to conventional voltage DC-link boost-buck rectifiers, 3-Φ current DC-link buck-boost (bB) rectifiers offer several advantages, i.e., most prominently a reduced number of magnetic components as the DC-link inductor employed in the front-end buck-type current-source rectifier (CSR) stage [11]–[13] is shared with the boost DC/DC output stage [14], [15] (see **Fig. 1a**, where a three-level (3-L) boost DC/DC-stage is used).

The 3-L boost DC/DC-stage inherently can provide two DC outputs. Thus, independent control of the two output voltages of a similar system has been analyzed in [1]. In general, the two partial output voltages $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$ can be controlled to equal or to different values, and at the same time the loads connected to either DC output can differ, i.e., $R_{\mathrm{out,p}} \neq R_{\mathrm{out,n}}$ is possible. However, the concept presented in [1] considers only conventional operation with a constant DC-link current i_{DC}, which must be selected at least as high as the mains phase current amplitudes such that the desired sinusoidal phase currents can be obtained by pulse-width modulated distribution of the constant DC-link current to the three phases. The CSR-stage thus operates with the so-called 3/3-PWM, i.e., all three phases of the CSR-stage are operated with PWM regardless of the operating mode (buck-mode if $V_{\mathrm{out,p}} + V_{\mathrm{out,n}} < {}^{3}\!/_{2}\hat{V}_{\mathrm{in}}$ or boost-mode if $V_{\mathrm{out,p}} + V_{\mathrm{out,n}} > \sqrt{3}\hat{V}_{\mathrm{in}}$, where $\hat{V}_{\mathrm{in}}$ denotes the grid phase voltage amplitude). Similarly, the two output DC currents, $I_{\mathrm{out,p}}$ and $I_{\mathrm{out,n}}$, are again obtained from the constant DC-link current by PWM operation of the two DC/DC-stage bridge-legs. Consequently, the constant DC-link current must also be at least as high as the higher of the two output DC currents and/or load currents. This is illustrated in **Fig. 1b.(i)** and **Fig. 1b.(ii)**, respectively.

In the buck-mode, the DC-link current is selected equal to the larger of the two output DC currents (i.e., $i_{\mathrm{DC}} = I_{\mathrm{out,p}}$ in the example shown in the figure) and hence the corresponding half-bridge (HB) of the DC/DC-stage can be clamped (i.e., operated with duty cycle $d_{\mathrm{p}} = 1$ and thus $\mathrm{T}_{\mathrm{DC,hp}}$ permanently turned on). On the other hand, the second HB of the DC/DC-stage operates with a duty cycle $d_{\mathrm{n}} < 1$ to reduce the DC-link current to the second, lower output current $I_{\mathrm{out,n}}$. Furthermore, as the DC-link current is larger than the peak phase current (only phase a is shown in the figure for better readability), the CSR-stage operates all three phases with PWM (i.e., with duty cycles $d_{\mathrm{a,b,c}} < 1$).

In the boost-mode, the DC-link current is still constant but the minimum required value is given by the amplitude of the phase currents and not by one of the two output currents, which are both lower than the DC-link current. Consequently, both HBs of the DC/DC-stage operate with $d_{\mathrm{p,n}} < 1$ to adapt the DC-link current to the respective output currents, $I_{\mathrm{out,p}}$ and

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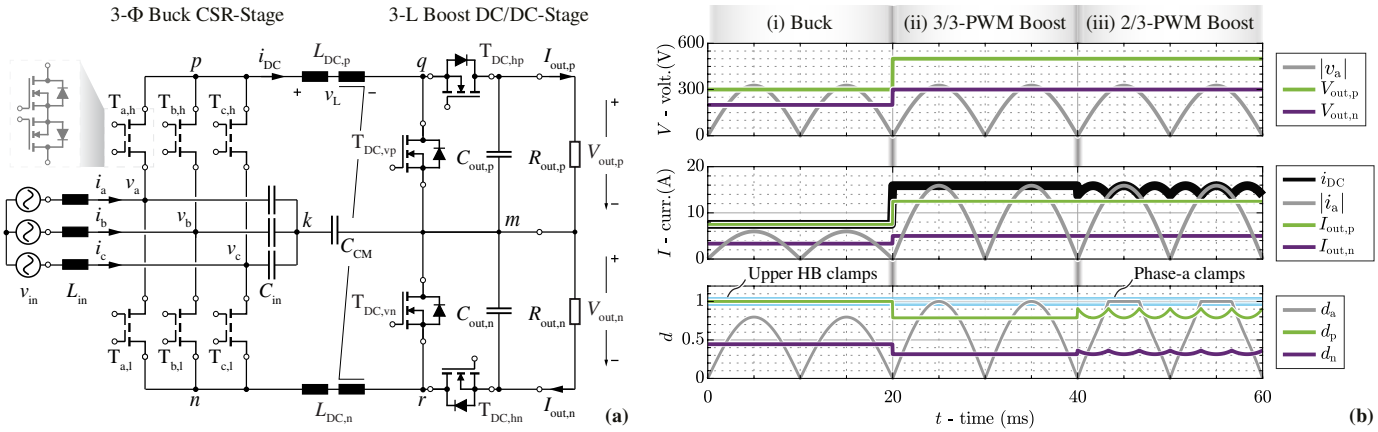

Fig. 1: (a) Circuit schematic of the considered 10 kW three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier system. The two DC output voltages, $V_{\text{out,p}}$ and $V_{\text{out,n}}$, are independently regulated to enable asymmetric loading capability. Circuit parameters are designed based on [16], i.e., switching frequencies $f_{\text{CSR}} = f_{\text{DC/DC}} = 100\,\text{kHz}$, DM DC-link inductor $L_{\text{DC,DM}} = 250\,\mu\text{H}$, input filter capacitor $C_{\text{in}} = 3 \times 6\,\mu\text{F}$, CM DC-link inductor $L_{\text{DC,CM}} = 14\,\text{mH}$, CM filter capacitor $C_{\text{CM}} = 88\,\text{nF}$, and output capacitor $C_{\text{out}} = 2 \times 11.2\,\mu\text{F}$. **(b)** Exemplary key waveforms for **(i)** operation in the buck-mode (identical for the conventional concept [1] and proposed concepts), **(ii)** conventional boost-mode with 3/3-PWM, and **(iii)** proposed boost-mode with 2/3-PWM where the DC/DC-stage controls the DC-link current to follow the six-pulse shape of the upper envelope of the phase current absolute values. Thus, at all times in boost-mode operation, only two out of the CSR-stage's three phases are operated with PWM while the third phase is clamped, which results in a considerable reduction of switching losses.

$I_{\text{out,n}}$. As the DC-link current is still constant, also all phases of the CSR-stage operate with PWM as in the buck-mode, i.e., with $d_{\text{a,b,c}} < 1$ at all times, and hence with 3/3-PWM.

However, if a time-varying (i.e., not constant) DC-link current is accepted, this current only needs to be at least as high as the highest *instantaneous* value of the rectified three-phase input currents. A two-stage 3-Φ bB current DC-link PFC rectifier system can thus advantageously operate the CSR-stage with so-called 2/3-PWM [17], [18] in the boost-mode by using the DC/DC-stage to control the DC-link current into the six-pulse shape of the upper envelope of the phase current absolute values. This is possible if the DC output current is lower than the minimum value of that envelope, i.e., if the converter operates in boost-mode. This then allows switching only two instead of three phases of the CSR-stage with a corresponding reduction in switching losses as illustrated in **Fig. 1b.(iii)**. Note that $d_{\text{a}} = 1$ for 1/3 of the grid period, i.e., the phase is clamped. Considering only a single load connected between the upper positive and the lower negative output terminals, a synergetic control concept that achieves 2/3-PWM whenever possible and ensures seamless transitions between the buck-mode (the CSR-stage operates with 3/3-PWM and regulates the DC-link current, while the switches $\text{T}_{\text{DC,hp}}$ and $\text{T}_{\text{DC,hn}}$ of the DC/DC-stage permanently conduct) and the boost-mode (the CSR-stage operates with 2/3-PWM, while the DC/DC-stage regulates the DC-link current along the above mentioned six-pulse shaped envelope) has been proposed in [19].

In this letter, we extend this synergetic and/or collaborative control concept to the case with two fully independently controlled DC outputs. The control scheme (see **Fig. 2**, **Fig. 3** and the detailed description in **Section III**) achieves loss-optimal operation of the converter system over a wide output voltage range, and still ensures seamless transitions between the different operating modes (i.e., buck- and boost-mode) and modulation schemes (i.e., 2/3-PWM and 3/3-PWM), considering especially also corner cases with zero loading of one output. Experimental results of a 10 kW demonstrator system confirm the proposed concept and reveal a considerable efficiency improvement over a wide load range, e.g., from 95.7 % to 96.9 % (1.2 %) at 2 kW and from 97.9 % to 98.4 % (0.5 %) at 10 kW with 800 V output voltage, also for boost-mode operation with unequal loads and with unequal output voltages.

II. Operating Modes with Independent Outputs

A 3-Φ bB current DC-link PFC rectifier system as shown in **Fig. 1a** with its two partial output voltages $V_{\text{out,p}}$ and $V_{\text{out,n}}$ utilized as a single output $V_{\text{out}} = V_{\text{out,p}} + V_{\text{out,n}}$ (connection of the load between the positive terminal of $V_{\text{out,p}}$ and the negative terminal of $V_{\text{out,n}}$) features only two main operating modes, i.e., buck-mode ($^3/_2\hat{V}_{\text{in}} > V_{\text{out}}$) and boost-mode ($\sqrt{3}\hat{V}_{\text{in}} < V_{\text{out}}$) as described in [19]. However, *four* main operating modes (see **Tab. I**) must be distinguished in case of utilizing $V_{\text{out,p}}$ and $V_{\text{out,n}}$ as individual, independently regulated DC outputs.

Similar to the single-output case, operation in these modes should optimally feature reduced switching losses by using 2/3-PWM of the CSR-stage whenever possible, or, alternatively, clamping both, one or none of the 3L DC/DC-stage's HBs, depending on the load conditions. Furthermore, minimum overall conduction losses should be achieved by ensuring operation with the minimum possible DC-link current: The

TABLE I: Operating modes of the proposed synergetically controlled 3-Φ bB current DC-link PFC rectifier system with two independent DC outputs (for the definition of x_{p}^* and x_{n}^* see **Section III**).

Mode	CSR-stage	DC/DC-stage	i_{DC}	x_{p}^*	x_{n}^*
Buck-I	3/3-PWM	No HB Sw.	I_{out}	0	0
Buck-II	3/3-PWM	1 HB Sw.	$I_{\text{out,max}}$	0 (1)	1 (0)
Boost-I	2/3-PWM	1 HB Sw.	$i_{\text{DC,2/3}}$	0 (1)	1 (0)
Boost-II	2/3-PWM	2 HBs Sw.	$i_{\text{DC,2/3}}$	α_{p}^*	α_{n}^*

3-Φ input currents and the two output DC currents are obtained by PWM-based reduction of the impressed DC-link current. Consequently, the DC-link current value has to be at least as high as the six-pulse time-varying upper envelope $i_{\text{DC,2/3}}$ of the instantaneous values of the rectified mains phase currents and at least as high as each of the two output DC currents. The minimum possible DC-link current at any given point in time is thus the maximum of these three currents, i.e., $i_{\text{DC}} = \max\{I_{\text{out,p}}, I_{\text{out,n}}, i_{\text{DC,2/3}}\}$, where $i_{\text{DC,2/3}}$ denotes the upper envelope of the absolute values of the 3-Φ mains currents (see also **Fig. 1b**) [19].

On the basis of the generic explanations given in the context of **Fig. 1b** and for the sake of brevity, the following description of the four operating modes (see **Tab. I**) is directly illustrated by later experimental results of a $10\,\text{kW}$ hardware demonstrator (see Fig. 4), which are in excellent agreement with simulation results (see Fig. 5 for buck-mode and Fig. 6 for boost-mode operation). **Section III** addresses the challenge of finding a control system that operates the converter in the respective optimum mode for a given load condition and furthermore achieves seamless transitions between the modes when the operating point changes.

A. Buck Modes

The converter operates in the buck-mode if $I_{\text{out,max}} = \max\{I_{\text{out,p}}, I_{\text{out,n}}\} > i_{\text{DC,2/3}}$ and hence the DC-link current is defined by $i_{\text{DC}} = I_{\text{out,max}}$. The CSR-stage then operates with conventional 3/3-PWM to step down the 3-Φ mains voltages to a lower DC output voltage (AC/DC voltage conversion of the CSR-stage and control the DC-link current). Considering the DC/AC current conversion of the CSR-stage, 3/3-PWM sinusoidally distributes i_{DC} to the three mains phases. Because $i_{\text{DC}} = I_{\text{out,max}}$, advantageously at least one HB of the DC/DC-stage is clamped to reduce the switching losses.

Specifically, in the **Buck-I** mode, the output power is only delivered through one of the two outputs, e.g., the upper output (i.e., no load is present at the lower output, $I_{\text{out,n}} = 0$) and the DC/DC-stage switching losses are avoided by ensuring $i_{\text{DC}} = I_{\text{out,p}}$ and permanently turning on $\text{T}_{\text{DC,hp}}$ and $\text{T}_{\text{DC,vn}}$, where the continuous on-state of $\text{T}_{\text{DC,vn}}$ prevents a current flow into $C_{\text{out,n}}$.

In the **Buck-II** mode, both outputs deliver power to their respective (possibly different) loads at (in the general case) two independent voltages. If, e.g., $I_{\text{out,n}} > I_{\text{out,p}}$, the lower HB is clamped, i.e., $\text{T}_{\text{DC,hn}}$ is continuously turned on and i_{DC} is controlled to $I_{\text{out,n}}$. However, switching of the upper HB is required to step down i_{DC} to $I_{\text{out,p}}$ and, at the same time, this HB regulates i_{DC}. The CSR-stage modulates the thus externally impressed i_{DC} into sinusoidal 3-Φ input currents with 3/3-PWM as i_{DC} is constant. The modulation index M of the CSR-stage can then be calculated as

$$M = \frac{\hat{I}_{\text{in}}}{i_{\text{DC}}} = \frac{\bar{v}_{\text{pn}}}{\frac{3}{2}\hat{V}_{\text{in}}} = \frac{\bar{v}_{\text{qr}}}{\frac{3}{2}\hat{V}_{\text{in}}} = \frac{d_{\text{p}} \cdot V_{\text{out,p}} + V_{\text{out,n}}}{\frac{3}{2}\hat{V}_{\text{in}}}, \qquad (1)$$

where $\hat{I}_{\text{in}}$ denotes the grid phase current amplitude. Thus, the input power drawn from the mains through the CSR-stage is controlled indirectly by the upper HB duty cycle d_{p} which ultimately modifies the CSR-stage modulation index M.

B. Boost Modes

The converter operates in the boost-mode if $I_{\text{out,max}} < i_{\text{DC,2/3}}$ and $i_{\text{DC}} = i_{\text{DC,2/3}}$, as shown in **Fig. 1b.(iii)**. The CSR-stage then operates with 2/3-PWM where no zero switching state is employed (v_{pn} never attains $0\,\text{V}$). To still obtain sinusoidal 3-Φ mains currents, at least one HB of the DC/DC-stage is required to regulate i_{DC} to follow the six-pulse shape $i_{\text{DC,2/3}}$ needed for 2/3-PWM.

Specifically, in the **Boost-I** mode, the output power is only delivered through one of the two outputs, e.g., the upper output, so that the upper HB switches to control the DC-link current.

Differently, both, the upper and the lower HBs are activated in the **Boost-II** operation and both outputs are loaded. The DC/DC-stage's two HBs are modulated such that they together control the DC-link current to the required six-pulse shape, while at the same time adapting this common DC-link current to the respective, possibly different output currents $I_{\text{out,p}}$ and $I_{\text{out,n}}$.

C. Hybrid Modes

Furthermore, **hybrid** modes, i.e., combinations of the aforementioned buck- and boost-modes within one mains period, occur because of the time-varying characteristic of $i_{\text{DC,2/3}}$, which could be lower and higher than $I_{\text{out,max}}$ over the course of one mains period; e.g., the converter operation could change between **Buck-II** mode (when $I_{\text{out,max}} > i_{\text{DC,2/3}}$) and **Boost-II** ($I_{\text{out,max}} < i_{\text{DC,2/3}}$) mode.

III. Synergetic Control Strategy

The proposed synergetic control strategy (see **Fig. 2**) ensures that the converter always operates in the optimum mode for a given operating point, i.e., with minimum possible losses, and transitions seamlessly between modes in case of changing operating points. As shown in **Fig. 2**, the control system consists of three functional blocks whose roles are explained in detail in the following subsections.

A. Independent Output Voltage Control

The two outermost control loops track the two output voltage references $V^*_{\text{out,p}}$ and $V^*_{\text{out,n}}$, respectively, by calculating the corresponding output power references $P^*_{\text{out,p}}$ and $P^*_{\text{out,n}}$. From that, the total power reference, i.e., the power that the CSR-stage must ultimately draw from the grid, $P^*_{\text{out}} = P^*_{\text{out,p}} + P^*_{\text{out,n}}$, follows. Furthermore, it is convenient to define the corresponding power shares α^*_{p} and α^*_{n} as

$$\alpha^*_{\text{p}} = \frac{P^*_{\text{out,p}}}{P^*_{\text{out}}} \quad \text{and} \quad \alpha^*_{\text{n}} = \frac{P^*_{\text{out,n}}}{P^*_{\text{out}}} \qquad (2)$$

for later use in the *DC-Link Current Control* block (see **Fig. 2**). Finally, the output current references, $I^*_{\text{out,p}}$ and $I^*_{\text{out,n}}$, are obtained and fed to the the next functional block.

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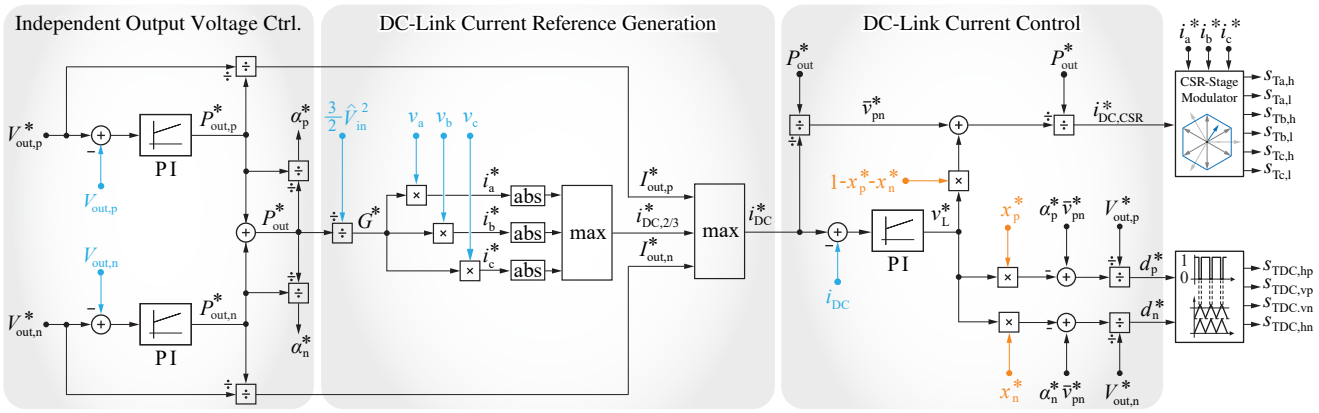

Fig. 2: Block diagram of the proposed synergetic control strategy for the 3-Φ bB current DC-link PFC rectifier system shown in **Fig. 1**, which achieves fully independent regulation of the two DC output voltages, $V_{\text{out,p}}$ and $V_{\text{out,n}}$, and optimum clamping of the CSR-stage and the two individual DC/DC-stage half-bridges (HBs).

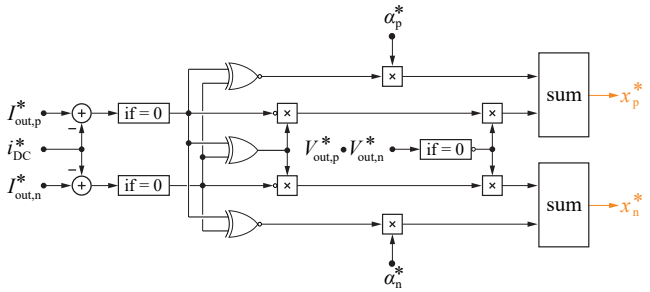

Fig. 3: Algorithm to calculate the distribution factors x_{p}^* and x_{n}^* (continuous values between 0 and 1) for the upper and lower DC/DC-stage HBs, respectively. Outputs are listed in **Tab. I** for different operating modes.

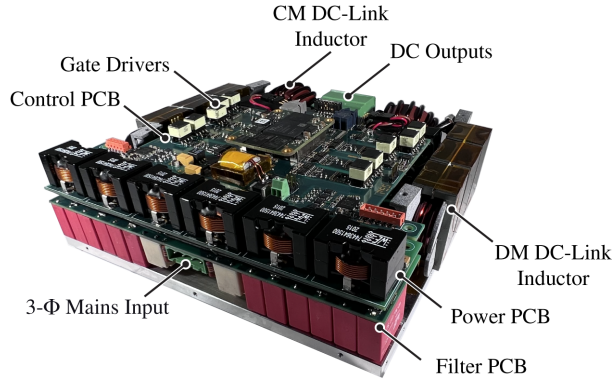

Fig. 4: 10 kW hardware demonstrator ($184 \times 172 \times 49\,\text{mm}^3$, $6.4\,\text{kW/L}$, $7.2 \times 6.8 \times 1.9\,\text{in}^3$, $107.5\,\text{W/in}^3$) of the system shown in **Fig. 1** operating from the 400 V 3-Φ mains. 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs are employed. Both DC outputs can operate independently, whereby the maximum output voltages are limited to 600 V (in order not to exceed 2/3 of the 900 V rated blocking capability of the DC/DC-stage power semiconductors) and the maximum output currents are limited to 25 A (DC-link design current). Circuit parameters are specified in **Fig. 1**.

B. DC-Link Current Reference Generation

First, a CSR-stage input reference conductance G^* is derived from the total power reference P_{out}^*. The 3-Φ sinusoidal mains current references i_{a}^*, i_{b}^*, and i_{c}^* that are proportional to the corresponding (measured) 3-Φ input voltages v_{a}, v_{b}, and v_{c}, i.e., ensure purely ohmic operation, directly follow. The upper envelope of the absolute 3-Φ sinusoidal mains current references defines the varying DC-link current reference $i_{\text{DC,2/3}}^*$ for 2/3-PWM operation.

As mentioned earlier, the minimal and thus optimal DC-link current value for a given operating condition is the maximum of the three possible reference values discussed so far, i.e., $i_{\text{DC}}^* = \max\{i_{\text{DC,2/3}}^*, I_{\text{out,p}}^*, I_{\text{out,n}}^*\}$. Thus, a DC-link current following the reference i_{DC}^* ensures minimized converter switching and conduction losses for any operating point, because (i) the DC-link current has the lowest possible value that is necessary to supply both outputs and to draw the total power from the grid, and (ii) because it facilitates clamping of one DC/DC-stage HB in buck-mode operation[1] and advantageous, in contrast to the state of the art [1], operation of the CSR-stage with 2/3-PWM in the boost-mode[2].

C. DC-Link Current Control

The next functional block is the DC-link current controller that uses the CSR-stage and the two DC/DC-stage HBs to synergetically control the DC-link current to the aforementioned reference value i_{DC}^*. The required voltage v_{L}^* across the DC-link inductor L_{DC} is first calculated by comparing the reference i_{DC}^* and the measured DC-link current i_{DC}. The realization of this voltage is then synergetically assigned to either the CSR-stage or the DC/DC-stage, e.g., a positive v_{L}^* can be generated by either an increased output voltage v_{pn} of the CSR-stage or a decreased input voltage v_{qr} of the DC/DC-stage (see **Fig. 1a** for the definition of these voltages). Note that a feedforward of the local average voltage $\bar{v}_{\text{pn}}^*$ at the CSR-stage's output can be obtained from the DC-link current reference i_{DC}^* and the total power (reference) P_{out}^*.

Different from the case with a single DC output [19], the synergetic generation of v_{L}^* now must consider two HBs of the DC/DC-stage individually. Thus, the two distribution factors x_{p}^* and x_{n}^* are introduced, whereby $x_{\text{p}}^*, x_{\text{n}}^* \in [0, 1]$ and $0 \leq x_{\text{p}}^* + x_{\text{n}}^* \leq 1$. The distribution factors are determined from

[1]The HB corresponding to the output with the higher current can be clamped, as the DC-link current i_{DC} equals that output current.

[2]The DC-link current follows $i_{\text{DC,2/3}}^*$, i.e., it always equals the (absolute value of) one phase current, and thus the corresponding phase of the CSR-stage can be clamped.

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Fig. 5: Experimental waveforms of the converter shown in **Fig. 1a** with the proposed synergetic control operating in the two buck-modes with a load resistance of $R_p = 30\,\Omega$ at the upper and of $R_n = 40\,\Omega$ at the lower DC output, for different set points of the two output voltages $V_{out,p}$ and $V_{out,n}$. Note that for unequal DC output voltages a corresponding offset appears in the voltage v_{mk} across the CM filter capacitor C_{CM} in addition to the third-harmonic voltage component (as $C_{CM} = 88\,\text{nF}$ only, the resulting low-frequency current flow is negligible, however). Note further the smooth and seamless transitions between different operating modes and modulation schemes.

i^*_{DC}, $I^*_{out,p}$ and $I^*_{out,n}$ (i.e., from the operating point) as shown in **Fig. 3**. To better understand that flowchart and the role of the distribution factors, it is useful to consider the effect of x^*_p and x^*_n in the DC-link current controller from **Fig. 2** for the different operating modes:

For operating points in the **Buck-I** mode, $x^*_p = x^*_n = 0$ and consequently the entire v^*_L is added to $\bar{v}^*_{pn}$. This modifies the reference DC-link current $i^*_{DC,CSR}$ used in the space-vector pulse-width modulator (SVPWM) of the CSR-stage as

$$i^*_{DC,CSR} = \frac{P^*_{out}}{\bar{v}^*_{pn} + (1 - x^*_p - x^*_n) \cdot v^*_L}. \tag{3}$$

For $v^*_L > 0$, a reduced $i^*_{DC,CSR}$ leads to prolonged active switching states of the CSR-stage and thus realizes the desired increase of $\bar{v}_{pn}$. Thus, only the CSR-stage regulates i_{DC} (to track, e.g., $i^*_{DC} = I^*_{out,p}$ if only the positive output port is activated) and the DC/DC-stage HBs can remain clamped (for the considered example, $d^*_p = 1$ and $d^*_n = 0$ follow from the control diagram[3]). This is clearly visible from the measured waveforms shown **Fig. 5.(i)** and **Fig. 5.(iv)**, where 3/3-PWM operation of the CSR-stage can be recognized from v_{pn} attaining the zero voltage level, and where both DC/DC-stage HBs are not switching.

Differently, in **Buck-II** mode and assuming, as an example, $I^*_{out,p} > I^*_{out,n}$ and hence $i^*_{DC} = I^*_{out,p}$, we find $x^*_p = 0$ and $x^*_n = 1$. Thus, the CSR-stage has no need to participate in the generation of v^*_L and only the DC/DC-stage controls the DC-link current. The CSR-stage modulation index M can be calculated as in (1). As discussed above, the upper HB of the DC/DC-stage remains clamped as $x^*_p = 0$ leads to $d^*_p = 1$. In contrast, $x^*_n = 1$ modifies the duty cycle d^*_n of the DC/DC-stage's lower HB such that its input voltage v_{mr} (see **Fig. 1a**) is decreased (again considering the example of realizing a $v^*_L >$

[3]For example, we find

$$d^*_p = \frac{\alpha^*_p \bar{v}^*_{pn}}{V^*_{out,p}} = \frac{P^*_{out,p}}{P^*_{out}} \cdot \frac{P^*_{out}}{i^*_{DC}} \cdot \frac{1}{V^*_{out,p}} = \frac{P^*_{out,p}}{I^*_{out,p} V^*_{out,p}} = 1$$

using the earlier definitions; $d^*_n = 0$ follows likewise.

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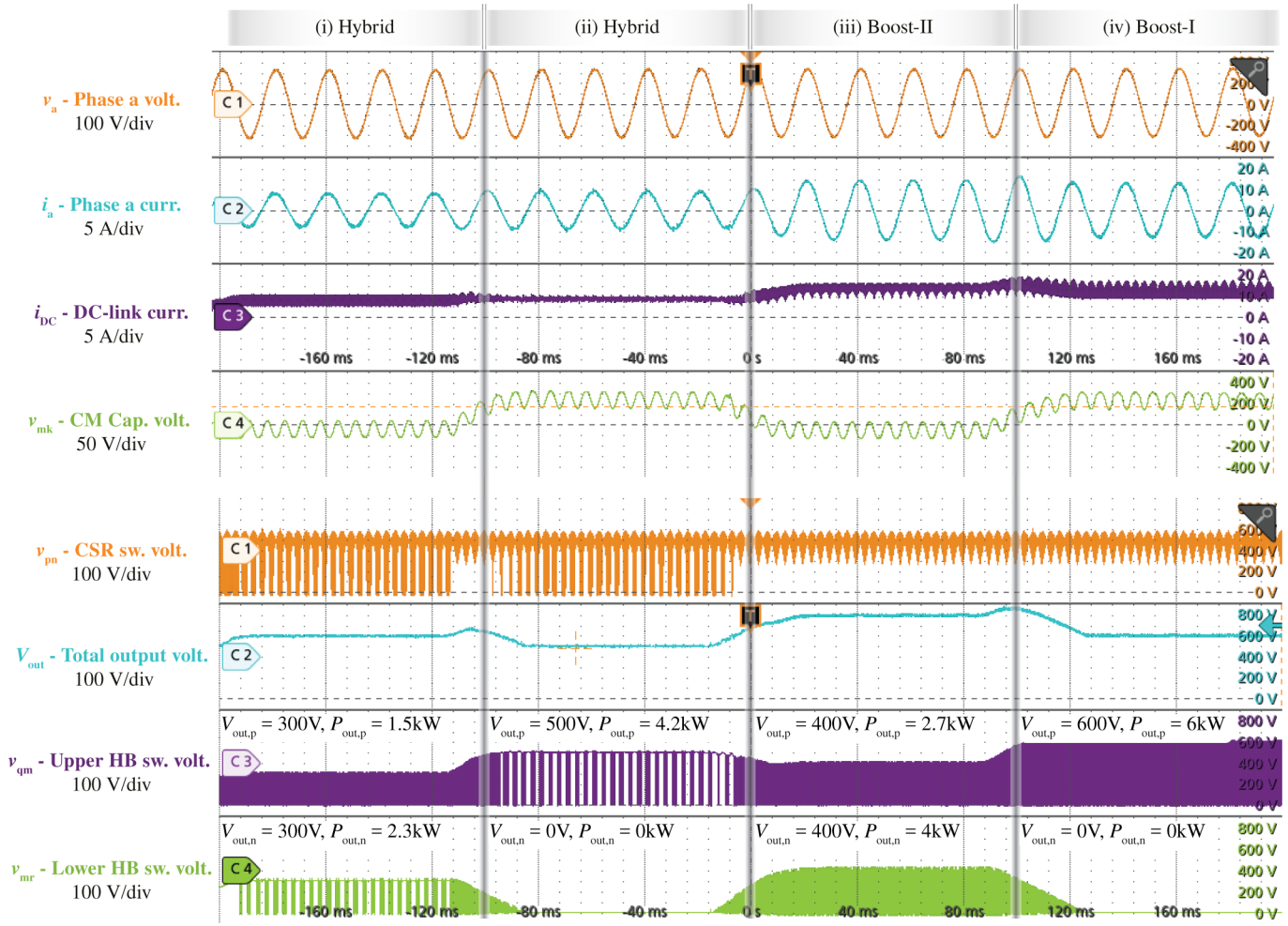

Fig. 6: Experimental waveforms of the converter shown in **Fig. 1a** with the proposed synergetic control operating in the two boost-modes with a load resistance of $R_p = 60\,\Omega$ at the upper and of $R_n = 40\,\Omega$ at the lower DC output. Note the absence of zero states in v_{pn} when the CSR-stage operates with 2/3-PWM. Note further that for unequal DC output voltages a corresponding offset appears in the voltage v_{mk} across the CM filter capacitor C_{CM} in addition to the third-harmonic voltage component (as $C_{CM} = 88\,\text{nF}$ only, the resulting low-frequency current flow is negligible, however). Note again (cf. **Fig. 5**) the smooth and seamless transitions between different operating modes and modulation schemes.

0) accordingly. The distribution factors α_p^* and α_n^* adjust the ratio between v_{qm} and v_{mr} according to the two ports' output powers, and the two duty cycles are given by

$$d_p^* = \frac{\alpha_p^* \cdot \bar{v}_{pn}^* - x_p^* v_L^*}{V_{out,p}^*} \text{ and } d_n^* = \frac{\alpha_n^* \cdot \bar{v}_{pn}^* - x_n^* v_L^*}{V_{out,n}^*}. \quad (4)$$

Fig. 5.(ii) illustrates that in the **Buck-II** mode the CSR-stage still operates with 3/3-PWM, and that always one of the two DC/DC-stage HBs is switching while the other is clamped.

In the boost-modes, $x_p^* = \alpha_p^*$ and $x_n^* = \alpha_n^*$ are obtained according to **Tab. I**. Since, by the definition in (2), $\alpha_p^* + \alpha_n^* = 1$, only the DC/DC-stage HBs are used to control the DC-link current i_{DC} to the six-pulse shape $i_{DC,2/3}^*$ that enables the CSR-stage to advantageously operate with 2/3-PWM, i.e., the proposed synergetic control concept automatically ensures that once possible (once the system operates in the boost mode) 2/3-PWM operation of the CSR-stage is achieved. In general, if both outputs are loaded, the v_L^* required by the DC-link current controller is distributed between the two HBs of the DC/DC-stage according to the power ratio (note that v_L^* is scaled with x_p^* and x_n^* in (4), respectively, before it is used to modify the duty cycles d_p^* and d_n^*, respectively, and $x_p^* = \alpha_p^*$, $x_n^* = \alpha_n^*$), i.e., both HBs are switching when operating in the **Boost-II** mode. **Fig. 6.(iii)** clearly proves that the CSR-stage operates with 2/3-PWM as v_{pn} does not attain the zero voltage level.

If only one output delivers power at a high-enough voltage, the converter operates in **Boost-I** mode, which can be considered a special case with, e.g., $\alpha_p^* = 1$ and $\alpha_n^* = 0$ if only the upper DC output delivers power.

Importantly, the inner DC-link current control loop gain is not affected by the seamless transitions between the modes, i.e., there are no abrupt changes in v_L^* but only different stages/HBs realize the required v_L^* at different operating modes. This ensures a resilient and robust DC-link current tracking capability, especially in the **hybrid** operating modes, where the system may transition between buck and boost modes several times during a grid period.

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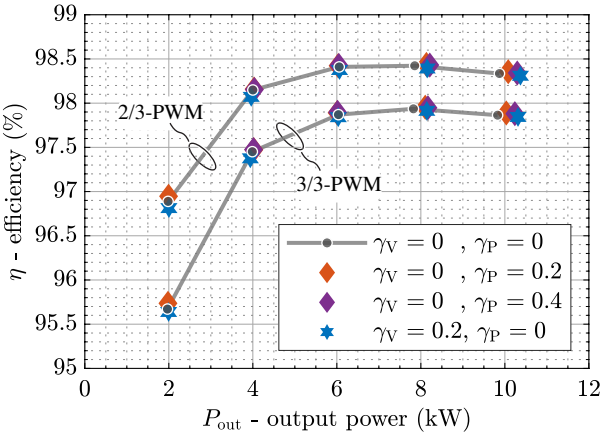

Fig. 7: Measured (Yokogawa WT3000) efficiencies of the 10 kW hardware demonstrator (see **Fig. 4**) in boost-mode operation ($V_{\text{out,p}} + V_{\text{out,n}} = 800\,\text{V}$) using the conventional approach with 3/3-PWM and the proposed synergetic control concept that facilitates 2/3-PWM of the CSR-stage. There is little impact of unequal output voltages ($\gamma_\text{V} \neq 0$) or of unequal loads ($\gamma_\text{P} \neq 0$). The total output power P_out is defined as $P_\text{out} = P_{\text{out,p}} + P_{\text{out,n}}$.

IV. Measured Efficiency Improvement

As outlined above, whereas in buck-mode the system behaves in the same way as a conventional realization [1], the proposed synergetic control concept promises significant loss reductions in boost-mode operation compared to the state of the art [1], which would maintain a constant DC-link current and 3/3-PWM even though the DC/DC-stage, which needs to operate anyway to step-up the CSR-stage output voltage and/or step-down the DC-link current, could be utilized to shape the DC-link current into the six-pulse shape that would facilitate 2/3-PWM operation of the CSR-stage. **Fig. 7** quantifies the efficiency improvements obtained when operating the 10 kW hardware demonstrator (see **Fig. 4**) at different boost operating modes with either the conventional approach (i.e., 3/3-PWM) or the proposed synergetic control concept (i.e., 2/3-PWM). All efficiencies have been measured with a Yokogawa WT3000 power analyzer and for a total output voltage of $V_{\text{out,p}} + V_{\text{out,n}} = 800\,\text{V}$.

As a baseline, symmetric conditions are considered, i.e., equal output voltages $V_{\text{out,p}} = V_{\text{out,n}}$ and hence

$$\gamma_\text{V} = (V_{\text{out,p}} - V_{\text{out,n}})/(V_{\text{out,p}} + V_{\text{out,n}}) = 0; \tag{5}$$

as well as equal loads $P_{\text{out,p}} = P_{\text{out,n}}$ and hence

$$\gamma_\text{P} = (P_{\text{out,p}} - P_{\text{out,n}})/(P_{\text{out,p}} + P_{\text{out,n}}) = 0. \tag{6}$$

For this case, an efficiency improvement of more than 0.5 % is found over a wide load range (e.g., from 95.7 % to 96.9 % at 2 kW and from 97.9 % to 98.4 % at 10 kW). Then, two cases with equal voltages ($\gamma_\text{V} = 0$) but asymmetric loads ($\gamma_\text{P} = 0.2$, i.e., a 60 % : 40 % split of the total output power $P_\text{out} = P_{\text{out,p}} + P_{\text{out,n}}$, and $\gamma_\text{P} = 0.4$, i.e., a 70 % : 30 % split) show almost exactly the same efficiencies and especially efficiency improvements between the conventional and the proposed control methods. This is expected because the operating conditions of the CSR-stage do not change, and even though the conduction times of the DC/DC-stage's switches change, the total generated conduction and switching losses of the DC/DC-stage remain the same. Finally, a case with equal load powers ($\gamma_\text{P} = 0$) but asymmetric output voltages ($\gamma_\text{V} = 0.2$, i.e., $V_{\text{out,p}} = 480\,\text{V}$ and $V_{\text{out,p}} = 320\,\text{V}$) also shows very similar efficiency improvements; an ever so slight reduction can be attributed to the higher switched voltage of one DC/DC-stage HB. These measurements thus confirm (i) a significant efficiency improvement in the boost-mode and (ii) that this efficiency improvement is rather independent of the asymmetries of the output voltages and the two loads.

V. Conclusion

In this letter, a synergetic control concept for a three-phase (3-Φ) buck-boost (bB) current DC-link AC/DC converter featuring two independently regulated DC outputs is proposed. The control scheme achieves a synergetic and/or collaborative operation of the 3-Φ buck-type CSR-stage and the two half-bridges (HBs) of the boost-type DC/DC-stage with minimum losses for any operating point (2/3-PWM of the CSR-stage or clamping of DC/DC converter HBs, and minimum possible DC-link current). Furthermore, seamless transitions between the different optimal operating modes and modulation schemes are ensured. All features are experimentally verified with a 10 kW hardware demonstrator system over a wide output voltage range, i.e., a total output voltage of 200 V to 800 V and individual port voltages of up to 600 V. Efficiency measurements show a significant improvement over a wide load range, e.g., from 95.7 % to 96.9 % (1.2 %) at 2 kW and from 97.9 % to 98.4 % (0.5 %) at 10 kW, compared to the state of the art methods when operating in the boost mode. This improvement is largely independent of output voltage asymmetries and/or load asymmetries.

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