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Optimal Common-Mode Voltage Injection for Phase-Modular Three-Phase PFC Rectifiers Minimizing Energy Buffering Requirement

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***Abstract*—Realizing an isolated three-phase Power Factor Correction (PFC) ac-dc converter as a phase-modular system, i.e, by star-connecting three single-phase PFC rectifier front-ends with individual isolated dc-dc converter stages generating a common dc output voltage advantageously facilitates the use of standard single-phase converter modules. Further the low dc-link voltage level of typically 400 V (for a grid with 230 V_{rms} line-to-neutral voltage) allows to employ high performance 600 V power semiconductors. The main drawback of this concept, however, is the fact that the time-varying single-phase input power only sums to a constant three-phase output power at the isolated dc output, such that large dc-link capacitor values are required in each module (in the range of several 100 µF for a 6 kW system), thereby limiting the achievable power density. It is known from literature that the dc-link energy buffering requirement ΔE_{dc} can be reduced by means of a third-harmonic common-mode (CM) voltage injection modulation and this paper identifies the optimal CM voltage waveform with respect to minimizing ΔE_{dc}, i.e., reducing ΔE_{dc} to the theoretical minimum by combining a brute-force evaluation of the time-domain CM voltage waveform with phase-symmetry considerations. Additionally, converter operation with minimum dc-link voltage and/or dc-link capacitor values is analyzed and a saturable grid current controller allowing operation of the PFC rectifier front-ends with the optimal CM voltage waveform is investigated. Experimental results with a 6 kW prototype system yield a reduction in ΔE_{dc} by up to 42 % (compared to conventional sinusoidal modulation), which closely matches the theoretical prediction. Also, PFC rectifier operation with a dc-link voltage level as low as 285 V (i.e., below the 325 V_{pk} grid line-to-neutral voltage amplitude) and with ultra-low dc-link capacitor values is demonstrated.**

***Index Terms*—ac-dc converter, three-phase, PFC rectifier, modular, harmonic injection, zero sequence, CM voltage injection**

I. Introduction

Forming a phase-modular isolated three-phase Power Factor Correction (PFC) ac-dc converter system comprising three single-phase PFC rectifier front-ends (with individual isolated dc-dc converter stages) connected to a common star-point $\bar{N}$ as highlighted in **Fig. 1** [1]–[5] has two major advantages: First, standard single-phase PFC rectifiers [6] can be employed, which is beneficial in terms of economies of scale, design effort, and maintainability. Second, the low average dc-link voltage level of typically $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ (compared to a standard non-modular/monolithic PFC ac-dc converter with an 800 V dc-link and 1.2 kV Silicon Carbide (SiC) semiconductors [7]–[9]) allows the usage of superior 600 V Gallium Nitride (GaN) semiconductors and thereby enables high conversion efficiencies $\eta > 99\,\%$ even for the simple two-level totem-pole PFC rectifier front-end structure considered here [6,10]–[13].

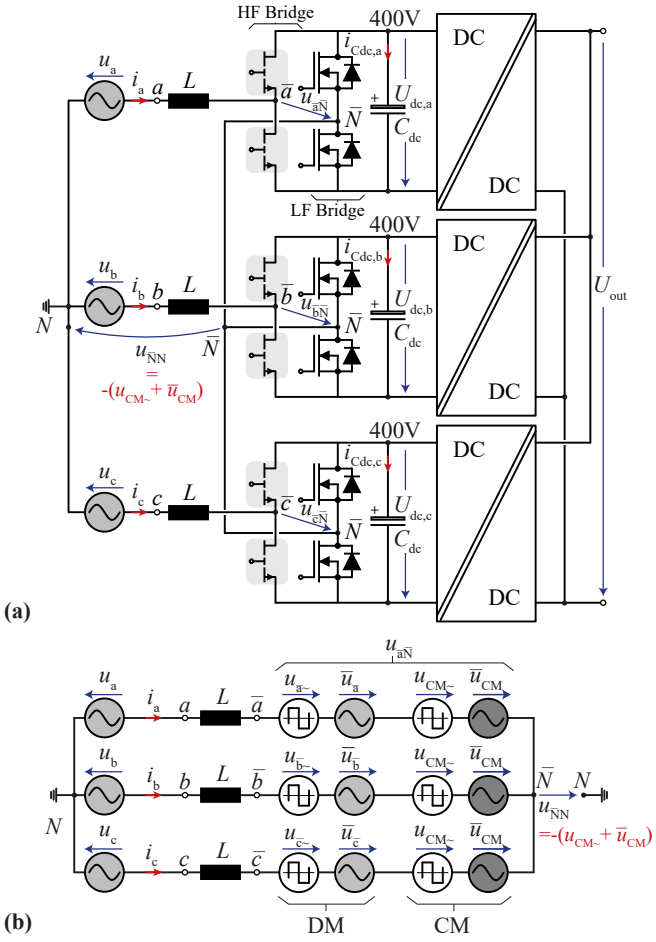

Fig. 1. (a) Considered converter structure of a phase-modular three-phase isolated Power Factor Correction (PFC) ac-dc converter system (main specifications are listed in **Table I**): Each phase module comprises a totem-pole PFC rectifier front-end with an HF bridge-leg and an LF unfolder bridge-leg combined with an isolated dc-dc converter stage connected to a common dc output voltage U_{out}. The module starpoint $\bar{N}$ is not connected to the grid starpoint N such that the CM voltage $u_{\bar{N}N}$ does not drive any current in the grid [14]. **(b)** ac-side equivalent circuit of the system: Although the CM voltage does not impact the grid currents, the grid currents flow through the Low-Frequency (LF) Common-Mode (CM) voltage $\bar{u}_{\mathrm{CM}}$ which hence can be used to alter the LF module input power flow.

The main drawback of the concept depicted in **Fig. 1**, however, is given by the fact that each converter module $x \in \{a, b, c\}$ is subject to a time-varying single-phase input power. Hence, large dc-link capacitor values C_{dc} are required which limit the maximally achievable volumetric

This paper has **not** been previously presented at any conference or submitted for review elsewhere.

TABLE I: SYSTEM SPECIFICATIONS.

Design.	Description	Value
U_{ac}	Grid voltage (line-to-neutral)	$3 \times 230\,\mathrm{V_{rms}}$
I_{ac}	Grid phase current	$3 \times 8.7\,\mathrm{A_{rms}}$
f_{ac}	Grid frequency	50 Hz
P_{N}	Nominal system power	6 kW
$\bar{U}_{\mathrm{dc}}$	Average dc-link voltage	400 V
f_{s}	Switching frequency	72 kHz
L	Boost inductor value	600 µH
C_{dc}	dc-link capacitor value	240 µF

converter power density.

Third-harmonic CM voltage injection modulation [15] and Space Vector Modulation (SVM) [16] are known from the field of non-modular/monolithic three-phase motor drive inverter systems and allow to increase the linear voltage operating range and/or dc-link voltage utilization. It was shown in [14,17] that third-harmonic injection modulation, which results in a CM voltage u_{CM} between the grid starpoint N and the module starpoint $\bar{N}$ in **Fig. 1a**, allows to redirect the pulsating single-phase input power among the modules, where sinusoidal grid currents $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$ are maintained due to the open starpoint configuration (a similar concept is also known from cascaded modular H-bridge converters [18]–[20]). Thereby, the dc-link energy buffering requirement can be reduced by up to 30 % compared to conventional modulation (and up to 39 % for phase-shifted third-harmonic voltage injection) [17] and further the minimally required dc-link voltage $\bar{U}_{\mathrm{dc}}$ and/or dc-link capacitance value C_{dc} can be reduced. The analysis of CM voltage injection in literature is, however, thus far limited to specific voltage waveforms (e.g., the above mentioned third-harmonic voltage injection), and this paper derives the optimum CM voltage waveform to minimize the dc-link energy buffering requirement by combining a brute-force waveform evaluation within the (time-varying) range of feasible CM voltages and phase-symmetry considerations.

This paper is structured as follows: **Sec. II** discusses the impact of the LF CM voltage on the PFC rectifier front-end power pulsation and identifies the optimal time-domain CM voltage waveform. Further, the lower bound of the dc-link voltage and dc-link capacitor values for the optimal CM voltage modulation is derived. Then, **Sec. III** presents a collaborative control structure where at any given point in time only two out of three rectifier modules are switched at High-Frequency (HF), thereby enabling PFC rectifier front-end operation with the optimal CM voltage injection modulation. Experimental results with a 6 kW prototype system that verify the theoretical considerations are presented in **Sec. IV** and **Sec. V** summarizes the main findings of this paper. Additionally, **Appendix A** discusses several dc-link voltage levels and the corresponding optimal CM voltage waveforms.

II. OPTIMUM CM VOLTAGE INJECTION MODULATION

A. Power Flow Fundamentals

The primary goal of the PFC rectifier front-ends in **Fig. 1a** (main converter waveforms are shown in **Fig. 2**) is to

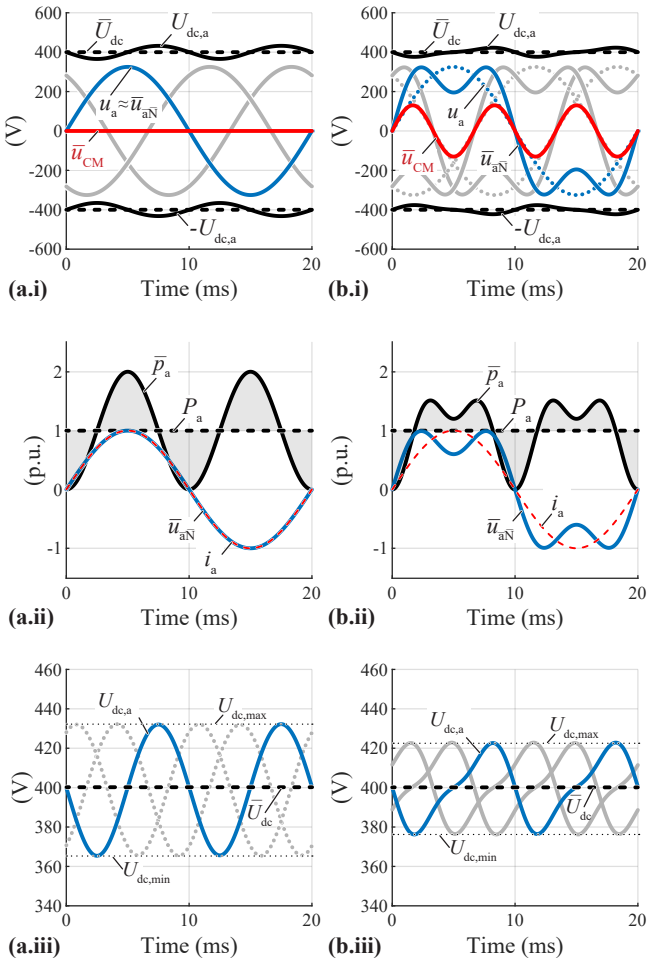

Fig. 2. Main PFC rectifier front-end waveforms (with focus on phase a) according to the system specifications in **Table I** for **(a)** conventional modulation (with $\bar{u}_{\mathrm{CM}} = 0$, $\Delta E_{\mathrm{dc,0}} = 6.4\,\mathrm{J}$, $\Delta U_{\mathrm{dc}} = 66.8\,\mathrm{V}$) and **(b)** third-harmonic voltage injection modulation [17] (with $\bar{u}_{\mathrm{CM}} = 0.4 \cdot \hat{U}_{\mathrm{ac}} \sin(3\omega_{\mathrm{ac}} t)$, $\Delta E_{\mathrm{dc}} = 4.5\,\mathrm{J}$, $\Delta U_{\mathrm{dc}} = 46.6\,\mathrm{V}$): **(x.i)** sinusoidal grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$, LF PFC rectifier front-end input voltages $\bar{u}_{\mathrm{a\bar{N}}}, \bar{u}_{\mathrm{b\bar{N}}}, \bar{u}_{\mathrm{c\bar{N}}}$ with respect to the common starpoint $\bar{N}$, and module a dc-link voltage $U_{\mathrm{dc,a}}$ (the average value $\bar{U}_{\mathrm{dc}}$ is represented by a dashed line). **(x.ii)** phase a LF PFC rectifier front-end input voltage $\bar{u}_{\mathrm{a\bar{N}}}$, grid current i_{a}, and LF input power $\bar{p}_{\mathrm{a}}$. **(x.iii)** module dc-link voltages $U_{\mathrm{dc,a}}, U_{\mathrm{dc,b}}, U_{\mathrm{dc,c}}$ and the resulting minimum $U_{\mathrm{dc,min}}$, average $\bar{U}_{\mathrm{dc}}$ and maximum $U_{\mathrm{dc,max}}$ values of the dc-link voltages.

regulate sinusoidal grid currents $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$ with amplitude $\hat{I}_{\mathrm{ac}}$ and in phase with the respective grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$ with amplitude $\hat{U}_{\mathrm{ac}}$. The grid power of phase $x \in \{a, b, c\}$ is defined as

$$p_{\mathrm{g,x}}(t) = u_{\mathrm{x}} \cdot i_{\mathrm{x}} = \underbrace{\frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}}_{P_{\mathrm{g,x}}} - \underbrace{\frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}\cos(2\omega_{\mathrm{ac}}t + 2\phi_{\mathrm{x}})}_{p_{\mathrm{g,x\sim}}(t)}, \tag{1}$$

with the phase angles $\phi_{\mathrm{x}} = \{0, -120°, -240°\}$, and comprises an ac component $p_{\mathrm{g,x\sim}}$ at twice the grid angular frequency $\omega_{\mathrm{ac}} = 2\pi f_{\mathrm{ac}}$ on top of the average phase input power $P_{\mathrm{g,x}} = \frac{1}{3}P_{\mathrm{N}}$, with P_{N} the nominal system power.

Fig. 1b depicts the ac-side equivalent circuit of the system. The module starpoint $\bar{N}$ is not connected to the grid starpoint N and therefore the CM voltage $u_{\mathrm{\bar{N}N}}$ (comprising an HF component $u_{\mathrm{CM\sim}}$ and an LF component $\bar{u}_{\mathrm{CM}}$) does not drive any current. However, the grid phase currents flow through

the LF CM voltage $\bar{u}_{\mathrm{CM}}$ in each module which thereby impacts the LF input power of module x as

$$\bar{p}_{\mathrm{x}}(t) = \bar{u}_{\mathrm{x\bar{N}}}(t) \cdot i_{\mathrm{x}}(t) = (u_{\mathrm{x}}(t) + \bar{u}_{\mathrm{CM}}(t)) \cdot i_{\mathrm{x}}(t). \quad (2)$$

For a constant PFC rectifier front-end dc output power $P_{\mathrm{x}} = P_{\mathrm{g,x}}$ (assuming a lossless power conversion) the energy buffered by the dc-link capacitor C_{dc} of module x is defined as

$$E_{\mathrm{dc,x}}(t) = \int_0^t (\bar{p}_{\mathrm{x}}(\tau) - P_{\mathrm{x}})\mathrm{d}\tau. \quad (3)$$

With $\Delta E_{\mathrm{dc}} = \max(E_{\mathrm{dc,x}}(t)) - \min(E_{\mathrm{dc,x}}(t))$ as energy buffering requirement of the dc-link capacitors C_{dc}, and the LF peak-to-peak voltage fluctuation of the dc-link capacitors results to

$$\Delta U_{\mathrm{dc}} = \frac{\Delta E_{\mathrm{dc}}}{C_{\mathrm{dc}} \bar{U}_{\mathrm{dc}}}. \quad (4)$$

Fig. 2a depicts the main converter waveforms of the module a for conventional operation with $\bar{u}_{\mathrm{CM}} = 0$ such that the module power $\bar{p}_{\mathrm{x}}(t) \approx p_{\mathrm{g,x}}(t)$ (see **Fig. 2a.ii**) shows the characteristic twice-mains-frequency single-phase grid variation. Here, the energy buffering requirement (highlighted by a gray area) results to

$$\Delta E_{\mathrm{dc},0} = \frac{\frac{1}{2}\hat{U}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}}{2\pi f_{\mathrm{ac}}}, \quad (5)$$

with $\Delta E_{\mathrm{dc},0} = 6.4\,\mathrm{J}$ for the specifications in **Table I**.

In contrast, **Fig. 2b** illustrates operation with a third-harmonic injection amplitude of $0.4 \times \hat{U}_{\mathrm{ac}}$. Here, the LF module input power is $\bar{p}_{\mathrm{x}}(t) \neq p_{\mathrm{g,x}}(t)$ and the power pulsation is shifted to higher frequencies such that $\Delta E_{\mathrm{dc}} = 4.5\,\mathrm{J}$ is reduced by 30 % compared to conventional modulation. This was verified experimentally in [17] and a reduction by up to 38 % was achieved for a third-harmonic injection amplitude $0.6 \times \hat{U}_{\mathrm{ac}}$ which, however, requires a third-harmonic voltage phase shift $\phi_{\mathrm{3rd}} = 11°$ to maintain grid current controllability.

The concept of CM voltage injection modulation is, however, not limited to third-harmonic voltages and the goal of the subsequent analysis is to identify the optimal LF CM voltage waveform $\bar{u}_{\mathrm{CM}}$ minimizing the dc-link energy buffering requirement ΔE_{dc}.

B. Optimal CM Voltage Waveform Identification

The system in **Fig. 1a** comprises three boost-type PFC rectifier front-ends such that the LF switch node voltage $\bar{u}_{\mathrm{x\bar{N}}}$ of each module $x \in \{a, b, c\}$ is limited by the respective dc-link voltage $U_{\mathrm{dc,x}}$ to values

$$\bar{u}_{\mathrm{x\bar{N}}}(t) = u_{\mathrm{x}}(t) + \bar{u}_{\mathrm{CM}}(t) \in [-U_{\mathrm{dc,x}}(t), U_{\mathrm{dc,x}}(t)]\,. \quad (6)$$

Hence, for a grid with $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ (line-to-neutral, $400\,\mathrm{V_{rms}}$ line-to-line), a typical dc-link voltage level $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ is considered here (for completeness, **Appendix A** further provides the optimal CM voltage waveforms for different values of $\bar{U}_{\mathrm{dc}}$ and **Appendix. B** discusses operation in an unbalanced grid) which advantageously allows the use of 600 V power semiconductors and ensures sufficient voltage margin to maintain grid current controllability in case of, e.g., a load step.

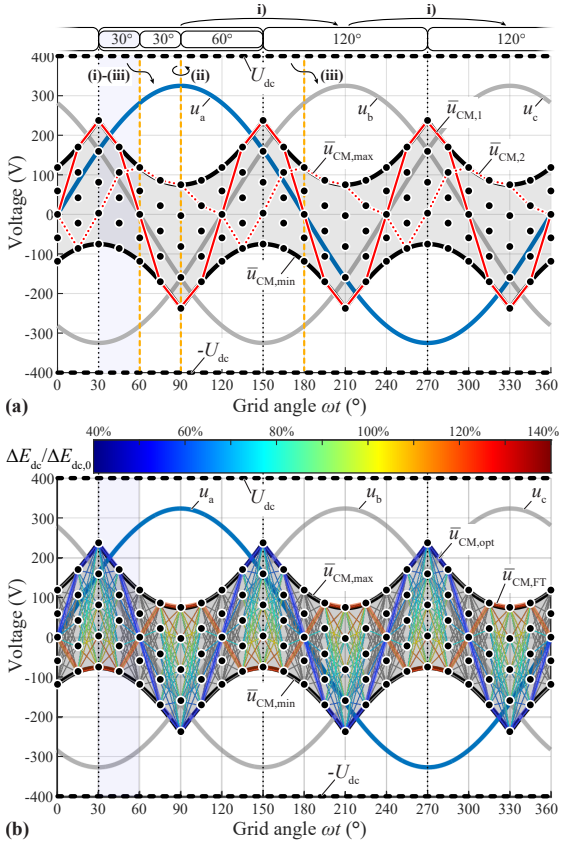

Fig. 3. Discrete LF CM voltage waveform optimization: grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$, ideally constant dc-link voltage $U_{\mathrm{dc}} = \bar{U}_{\mathrm{dc}}$ and eligible LF CM voltage range (highlighted by a light gray area) limited by $\bar{u}_{\mathrm{CM,max}}$ and $\bar{u}_{\mathrm{CM,min}}$ according to (7). The considered time- and value-discretized CM voltage values ($n_{\mathrm{u}} = 5$ and $n_{\mathrm{t}} = 25$) are highlighted with scatter points: **(a)** illustration of the symmetry conditions (i)-(iii) and two exemplary CM voltage waveforms $\bar{u}_{\mathrm{CM,1}}$ (complying with the conditions (i)-(iii)) and $\bar{u}_{\mathrm{CM,2}}$ (complying with the condition (i) but violating the conditions (ii) and (iii)). **(b)** illustration of the $n = 3125$ CM voltage waveforms obtained with (i) and (ii) represented by thin gray lines. The $n = 25$ waveforms according to (i)-(iii) are further highlighted with the line color indicating the resulting energy buffering requirement ΔE_{dc} relative to $\Delta E_{\mathrm{dc,0}}$ for modulation without CM voltage injection and $\bar{u}_{\mathrm{CM}} = 0$. The best $\bar{u}_{\mathrm{CM,opt}}$ and worst $\bar{u}_{\mathrm{CM,FT}}$ CM voltage waveforms with respect to the resulting ΔE_{dc} are highlighted with thicker lines and discussed in more detail in **Fig. 4**.

In the following, the LF fluctuation of the dc-link voltages caused by the LF input power pulsation is neglected, i.e., $C_{\mathrm{dc}} \gg 100\,\mu\mathrm{F}$ is assumed such that $U_{\mathrm{dc,x}}(t) = \bar{U}_{\mathrm{dc}}$. Hence, the boost-type converter input voltage limit (6) for all three modules can be solved for the eligible range of the LF CM voltage $\bar{u}_{\mathrm{CM}}$ which is defined by

$$\begin{aligned} \bar{u}_{\mathrm{CM,max}}(t) &= \bar{U}_{\mathrm{dc}} - \max(u_{\mathrm{a}}(t), u_{\mathrm{b}}(t), u_{\mathrm{c}}(t)) \\ \bar{u}_{\mathrm{CM,min}}(t) &= -\bar{U}_{\mathrm{dc}} - \min(u_{\mathrm{a}}(t), u_{\mathrm{b}}(t), u_{\mathrm{c}}(t)), \end{aligned} \quad (7)$$

as highlighted in **Fig. 3** for $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$. Note that current controllability according to (6) is lost in the phase with the instantaneously highest absolute grid voltage value $|u_{\mathrm{x}}|$ in case of $\bar{u}_{\mathrm{CM}}$ exceeding this limit (7).

In order to identify the optimal LF CM voltage waveform $\bar{u}_{\mathrm{CM}}$, the CM voltage range defined by (7) within one grid period $T_{\mathrm{ac}} = 1/f_{\mathrm{ac}}$ is discretized with n_{t} values in the time domain and with n_{u} CM voltage values.

Fig. 3 illustrates the discretized voltage and time values

with scatter points for $n_\mathrm{u} = 5$ and $n_\mathrm{t} = 25$. The number of possible LF CM voltage waveforms (i.e., the number of permutations for n_u discrete CM voltage values and n_t time positions) grows exponentially with the discretization resolution as $n = n_\mathrm{u}^{n_\mathrm{t}}$ with $n \approx 3 \times 10^{17}$ for the considered example, i.e., an excessive number of paths to be evaluated results even for the low example resolution. However, symmetry considerations allow to drastically decrease the number of paths n:

(i) The CM voltage waveform must equally impact the energy buffering requirement in all three PFC rectifier front-ends, which corresponds to a 120° symmetry of the CM voltage. Hence, the CM waveforms are only explored within one 120° interval ($\omega t \in [30°, 150°]$ highlighted in **Fig. 3**). The full 360° waveforms are then obtained by replicating the 120° waveforms (i.e., with $\bar{u}_\mathrm{CM}(\omega t) = \bar{u}_\mathrm{CM}(\omega t + 120°)$) and the total number of paths is reduced to $n = n_\mathrm{u}^{(n_\mathrm{t}-1)/3+1} \approx 2 \times 10^6$ for the considered example.

(ii) Within the considered 120° interval ($\omega t \in [30°, 150°]$), symmetry along the $\omega t = 90°$ axis is required as otherwise the energy buffering requirement ΔE_dc is, e.g., decreased in the first 60° segment but increased in the second 60° segment (or vice versa). Hence, the CM voltage waveforms are only explored within the first 60° segment ($\omega t \in [30°, 90°]$) and mirrored to the second segment (i.e., $\bar{u}_\mathrm{CM}(90° + \omega t) = \bar{u}_\mathrm{CM}(90° - \omega t)$). With (i) and (ii) the number of paths is reduced to $n = n_\mathrm{u}^{(n_\mathrm{t}-1)/6+1} \approx 3 \times 10^3$ for the considered example.

(iii) The number of CM waveforms to be evaluated can be further decreased by only considering the waveforms with half-wave symmetry (i.e., $\bar{u}_\mathrm{CM}(180° + \omega t) = -\bar{u}_\mathrm{CM}(180° - \omega t)$), as otherwise the energy buffering requirement ΔE_dc is, e.g., decreased in the first 180° half-period but increased in the second 180° half-period (or vice versa). Combined with (i) and (ii) this results to $\bar{u}_\mathrm{CM}(60° + \omega t) = -\bar{u}_\mathrm{CM}(60° - \omega t)$ and $\bar{u}_\mathrm{CM}(\omega t = 60°) = 0$ (any signal comprising only triplen harmonics with $\sin(k \cdot 3 f_\mathrm{ac})$ at multiples $k \in \mathbb{N}$ of $3 f_\mathrm{ac}$ results to zero at $\omega t = 60°$) Hence, the valid CM voltage waveforms can be defined upon a single 30° interval and the number of paths is reduced to $n = n_\mathrm{u}^{(n_\mathrm{t}-1)/12} = 25$ for the considered example.

The CM voltage waveforms (calculated in MATLAB) obtained with (i) and (ii) are highlighted in **Fig. 3b** with thin gray lines, and the resulting $n = 25$ valid waveforms according to (i)-(iii) are further highlighted with the line color indicating the resulting energy buffering requirement ΔE_dc relative to $\Delta E_{\mathrm{dc},0}$ (modulation without CM injection and $\bar{u}_\mathrm{CM} = 0$). The best $\bar{u}_\mathrm{CM,opt}$ and worst $\bar{u}_\mathrm{CM,FT}$ CM voltage waveforms with respect to the resulting ΔE_dc are highlighted with thicker lines in **Fig. 3b** and discussed in more detail in the following.

C. Optimal CM Voltage Waveform Results

A high-resolution waveform sweep with $n_\mathrm{u} = 9$ and $n_\mathrm{t} = 97$ is conducted and the symmetry conditions (i)-(iii) reduce the number of investigated waveforms from $n \approx 4 \times 10^{92}$ to $n \approx 43 \times 10^6$ which is manageable with state-of-the art compute servers.

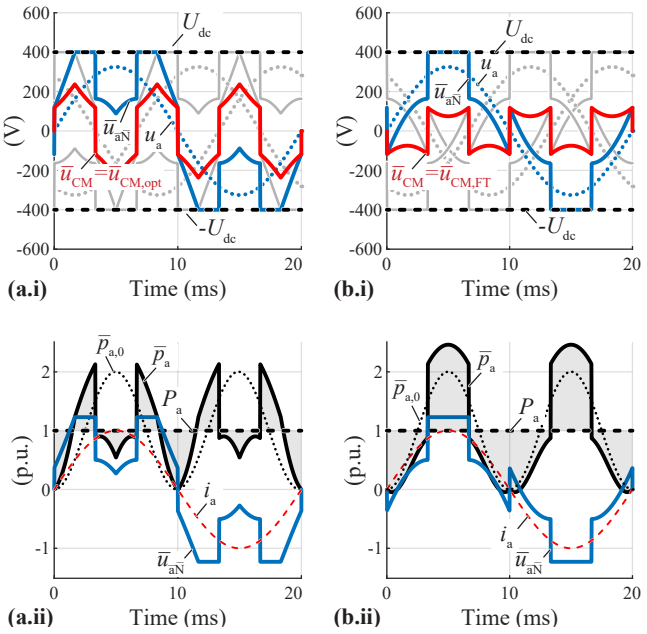

Fig. 4. Main PFC rectifier front-end waveforms (with focus on phase a) according to the system specifications in **Table I** and $C_\mathrm{dc} \to \infty$ for **(a)** the optimal (with $\bar{u}_\mathrm{CM} = \bar{u}_\mathrm{CM,opt}$, $\Delta E_\mathrm{dc} = 3.6\,\mathrm{J}$) and **(b)** the worst CM voltage waveform (with $\bar{u}_\mathrm{CM} = \bar{u}_\mathrm{CM,FT}$, $\Delta E_\mathrm{dc} = 9.0\,\mathrm{J}$): **(x.i)** sinusoidal grid voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$, LF PFC rectifier front-end input voltages $\bar{u}_\mathrm{a\bar{N}}, \bar{u}_\mathrm{b\bar{N}}, \bar{u}_\mathrm{c\bar{N}}$ with respect to the common starpoint N, and ideally constant dc-link voltage $U_\mathrm{dc} = \bar{U}_\mathrm{dc}$. **(x.ii)** phase a LF PFC rectifier front-end input voltage $\bar{u}_\mathrm{a\bar{N}}$, grid current i_a, and LF input power $\bar{p}_\mathrm{a}$ (for comparison the input power $\bar{p}_{\mathrm{a},0}$ for conventional operation from **Fig. 2a** is presented with a dotted line).

The resulting optimal LF CM voltage waveform $\bar{u}_\mathrm{CM,opt}$ is very similar to **Fig. 3b** and converges (with increasing resolution n_u and n_t) to the Discontinuous Pulse Width Modulation (DPWM) strategy (which should not be confused with *Digital* PWM) highlighted in **Fig. 4a**, where the switch-node $\bar{x}$ of the phase $x \in \{a, b, c\}$ with the instantaneous middle absolute grid voltage value $|u_\mathrm{x}(t)| = \mathrm{median}(|u_\mathrm{a}(t)|, |u_\mathrm{b}(t)|, |u_\mathrm{c}(t)|)$ is clamped depending on the instantaneous grid voltage polarity to the positive (if $u_\mathrm{x} > 0$) or negative (if $u_\mathrm{x} < 0$) dc-link rail, and $\bar{u}_\mathrm{CM,opt}$ is defined as

$$\bar{u}_\mathrm{CM,opt}(t) = \begin{cases} \bar{U}_\mathrm{dc} - u_\mathrm{x}(t), & u_\mathrm{x}(t) \geq 0 \\ -\bar{U}_\mathrm{dc} - u_\mathrm{x}(t), & u_\mathrm{x}(t) < 0, \end{cases} \tag{8}$$

which, e.g., for the first 120° interval of the grid period results to

$$\bar{u}_\mathrm{CM,opt}(t) = \begin{cases} \bar{U}_\mathrm{dc} - u_\mathrm{c}(t), & 0° < \omega_\mathrm{ac} t \leq 30° \\ \bar{U}_\mathrm{dc} - u_\mathrm{a}(t), & 30° < \omega_\mathrm{ac} t \leq 60° \\ -\bar{U}_\mathrm{dc} - u_\mathrm{b}(t), & 60° < \omega_\mathrm{ac} t \leq 90° \\ -\bar{U}_\mathrm{dc} - u_\mathrm{c}(t), & 90° < \omega_\mathrm{ac} t \leq 120°. \end{cases} \tag{9}$$

Such a modulation strategy is known in literature within the context of non-modular/monolithic three-phase PFC ac-dc converters [21] (featuring a single dc output voltage)

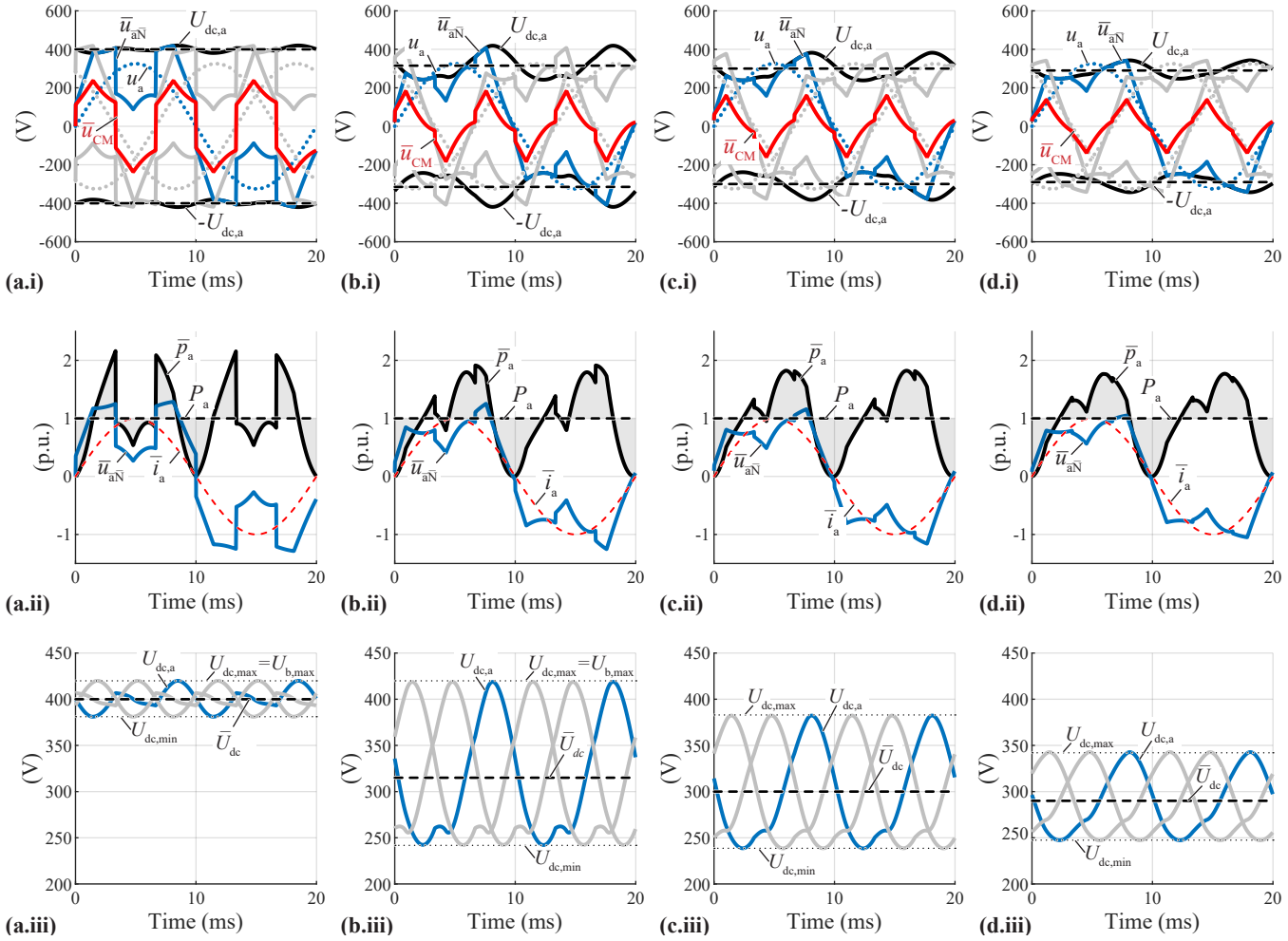

Fig. 5. Main PFC rectifier front-end waveforms (with focus on phase a) according to the system specifications in **Table I** for optimal CM voltage modulation and **(a)** $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$, $C_{\mathrm{dc}} = 231\,\mu\mathrm{F}$ ($\Delta E_{\mathrm{dc}} = 3.6\,\mathrm{J}$, $\Delta U_{\mathrm{dc}} = 38.9\,\mathrm{V}$), **(b)** $\bar{U}_{\mathrm{dc}} = 315\,\mathrm{V}$, $C_{\mathrm{dc}} = 88\,\mu\mathrm{F}$ ($\Delta E_{\mathrm{dc}} = 4.8\,\mathrm{J}$, $\Delta U_{\mathrm{dc}} = 176.7\,\mathrm{V}$), **(c)** $\bar{U}_{\mathrm{dc}} = 300\,\mathrm{V}$, $C_{\mathrm{dc}} = 116\,\mu\mathrm{F}$ ($\Delta E_{\mathrm{dc}} = 4.9\,\mathrm{J}$, $\Delta U_{\mathrm{dc}} = 143.9\,\mathrm{V}$), and **(d)** $\bar{U}_{\mathrm{dc}} = 290\,\mathrm{V}$, $C_{\mathrm{dc}} = 179\,\mu\mathrm{F}$ ($\Delta E_{\mathrm{dc}} = 4.9\,\mathrm{J}$, $\Delta U_{\mathrm{dc}} = 95.4\,\mathrm{V}$): **(x.i)** sinusoidal grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$, LF PFC rectifier front-end input voltages $\bar{u}_{\mathrm{a\bar{N}}}, \bar{u}_{\mathrm{b\bar{N}}}, \bar{u}_{\mathrm{c\bar{N}}}$ with respect to the common starpoint $\bar{N}$, and module a dc-link voltage $U_{\mathrm{dc,a}}$ (the average value $\bar{U}_{\mathrm{dc}}$ is represented by a dashed line). **(x.ii)** phase a LF PFC rectifier front-end input voltage $\bar{u}_{\mathrm{a\bar{N}}}$, grid current i_{a}, and LF input power $\bar{p}_{\mathrm{a}}$. **(x.iii)** module dc-link voltages $U_{\mathrm{dc,a}}, U_{\mathrm{dc,b}}, U_{\mathrm{dc,c}}$, and the resulting minimum $U_{\mathrm{dc,min}}$, average $\bar{U}_{\mathrm{dc}}$ and maximum $U_{\mathrm{dc,max}}$ values of the dc-link voltages (note that in (a) and (b) $U_{\mathrm{dc,max}}$ equals the maximum blocking voltage of the power semiconductors $U_{\mathrm{b,max}}$).

and cascaded modular H-bridge converters [20], and the CM voltage $\bar{u}_{\mathrm{CM,opt}}$ increases the LF module input power $\bar{p}_{\mathrm{a}}$ in the vicinity of $\omega t = 30°$ and decreases $\bar{p}_{\mathrm{a}}$ around $\omega t = 90°$ compared to $\bar{p}_{\mathrm{a},0}$ representing the LF input power for conventional operation as comparison.

For this CM voltage waveform $\bar{u}_{\mathrm{CM,opt}}$ the energy buffering requirement of the PFC rectifier front-ends (visualized by the light-gray areas in **Fig. 4a**) results to $\Delta E_{\mathrm{dc}} = 3.6\,\mathrm{J}$, i.e., a reduction of 43 % is achieved compared to the conventional modulation with $\bar{u}_{\mathrm{CM}} = 0$ presented in **Fig. 2a**. Additionally, the semiconductor switching losses are advantageously reduced due to the 1/3 lower number of switching actions (enabled by the DPWM operation where always one out of three PFC rectifier front-ends is in a clamped state) compared to $\bar{u}_{\mathrm{CM}} = 0$ (where all PFC rectifier front-ends are continuously switching). Note that the time discretization n_{t} limits the derivative $\mathrm{d}\bar{u}_{\mathrm{CM}}/\mathrm{d}t$ at the CM voltage zero crossing at $k \cdot 60°$ ($k \in \mathbb{N}$, see **Fig. 3b**). However, for $n_{\mathrm{t}} = 97$ the resulting ΔE_{dc} differs by only <1 % from the ideal waveforms depicted in **Fig. 4a**.

For completeness, also the worst (with respect to minimizing ΔE_{dc}) CM voltage waveform $\bar{u}_{\mathrm{CM,FT}}$ given by the Flat Top (FT) DPWM [21]–[23] strategy is highlighted in **Fig. 4b**. There, the switch-node $\bar{x}$ of the phase x with the instantaneous maximum absolute grid voltage value is clamped depending on the instantaneous grid voltage polarity to the positive (if $u_{\mathrm{x}} > 0$) or negative (if $u_{\mathrm{x}} < 0$) dc-link rail. Such a modulation is optimal with respect to switching losses, as the PFC rectifier front-end with the highest instantaneous current values ceases switching and is hence of interest in non-modular/monolithic PFC ac-dc converters without LF energy storage requirement. However, here, the energy buffering requirement of the PFC rectifier front-end increases by 41 % compared to conventional modulation to $\Delta E_{\mathrm{dc}} = 9.0\,\mathrm{J}$. The reason for this increase in ΔE_{dc} becomes obvious from **Fig. 4a.ii** as, e.g., for phase a, the waveform $\bar{u}_{\mathrm{CM,FT}}$ further increases the module input power $\bar{p}_{\mathrm{a}}$ in the vicinity of $\omega t = 90°$ where the maximum pulsation of the grid power $p_{\mathrm{g,a}}$ occurs.

D. Minimum DC-Link Voltage / Capacitance Operation

For finite dc-link capacitance values C_{dc} the dc-link voltages fluctuate due to the pulsating LF module input power $\bar{p}_{\mathrm{x}}$. Given that (6) is fulfilled for all modules throughout the fundamental grid period (i.e., grid current controllability is maintained), the dc-link voltage fluctuation does not impact the generation of the LF CM voltage for, e.g., conventional modulation and third-harmonic voltage injection. This, however, does not apply for the DPWM strategies depicted in **Fig. 4:** If one phase x clamps its switch node $\bar{x}$ to the corresponding positive dc-link rail, the CM voltage reference for the two remaining PFC rectifier front-ends switching at HF is defined as $\bar{u}_{\mathrm{CM}}(t) = U_{\mathrm{dc,x}}(t) - u_{\mathrm{x}}(t)$, i.e., is affected by the LF dc-link voltage fluctuation of phase x. Hence, according to (2) the LF fluctuation of the dc-link voltage $U_{\mathrm{dc,x}}(t)$ impacts the module input power $\bar{p}_{\mathrm{x}}(t)$, and vice versa, such that no simple analytic expression exists to describe the input voltage, current and power waveforms of the PFC rectifier front-end for finite values of C_{dc}. Therefore, the numerical calculation of the steady-state input power waveform and the corresponding fluctuation of the dc-link voltages is performed iteratively in MATLAB until the waveforms converge.

Fig. 5a presents the calculated main PFC rectifier front-end waveforms for an average dc-link voltage $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ and $C_{\mathrm{dc}} = 231\,\mu\mathrm{F}$ in each phase. There, the peak-to-peak dc-link voltage fluctuation results to $\Delta U_{\mathrm{dc}} = 38.9\,\mathrm{V}$ and slightly impacts the generated CM voltage waveform $\bar{u}_{\mathrm{CM}}$. However, the LF module input power $\bar{p}_{\mathrm{a}}$ is largely identical to **Fig. 4a** with $C_{\mathrm{dc}} \to \infty$ such that also the resulting $\Delta E_{\mathrm{dc}} = 3.6\,\mathrm{J}$ remains unaffected by the finite dc-link capacitor value.

The relevant question for the practical realization of the optimal CM modulation of **Sec. II-C** is hence what minimum amount of dc-link capacitance $C_{\mathrm{dc,min}}$ is required in each phase module to assure the safe PFC rectifier front-end operation. For this, two relevant conditions exist: First, the current controllability according to (6) needs to be maintained. Second, the maximum blocking voltage of the power semiconductors must be respected, corresponding in each phase x to the constraint

$$U_{\mathrm{dc,x}}(t) \leq U_{\mathrm{b,max}}, \tag{10}$$

with typically $U_{\mathrm{b,max}} = 420\,\mathrm{V}$ for 600 V power semiconductors to assure a blocking voltage margin of 30 % which is considered in the following.

Fig. 6 investigates the minimally required dc-link capacitor value $C_{\mathrm{dc,min}}$ of the optimal CM voltage injection modulation for nominal power operation according to **Table I** as a function of the average dc-link voltage levels $\bar{U}_{\mathrm{dc}}$. The steady-state input power waveform and the corresponding fluctuation of the dc-link voltages are again calculated numerically in MATLAB and for a given value of $\bar{U}_{\mathrm{dc}}$, $C_{\mathrm{dc,min}}$ is obtained by decreasing C_{dc} iteratively up to the point where either (6) or (10) is no longer fulfilled.

The previously discussed operating condition in **Fig. 5a** is highlighted in **Fig. 6** and the selected capacitance value corresponds to $C_{\mathrm{dc,min}} = 231\,\mu\mathrm{F}$ for $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$, which is substantially below $C_{\mathrm{dc,min,0}} = 400\,\mu\mathrm{F}$ required to

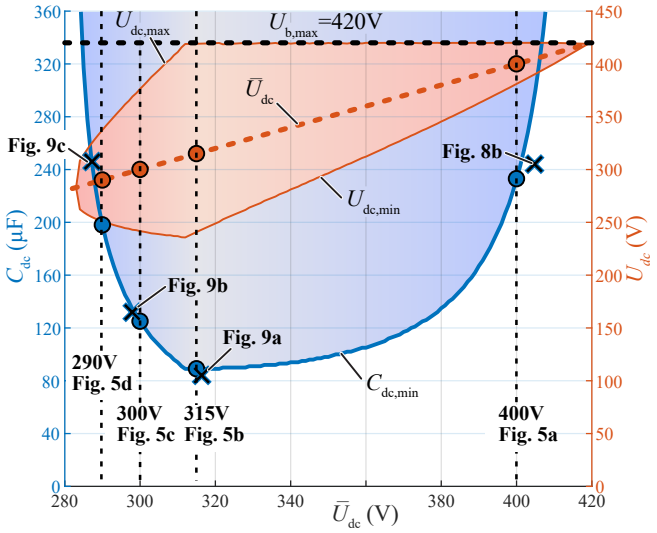

Fig. 6. Impact of the average dc-link voltage level $\bar{U}_{\mathrm{dc}}$ on the minimally required dc-link capacitor value $C_{\mathrm{dc,min}}$ for the optimum CM voltage injection modulation of **Sec. II-C**. The resulting minimum $U_{\mathrm{dc,min}}$, average $\bar{U}_{\mathrm{dc}}$ and maximum $U_{\mathrm{dc,max}}$ values of the dc-link voltage $U_{\mathrm{dc,x}}(t)$ for nominal power operation according to **Table I** are highlighted on the second y-axis. Note that $C_{\mathrm{dc,min}}$ is defined by the maximum blocking voltage of the power semiconductors $U_{\mathrm{b,max}}$ for $\bar{U}_{\mathrm{dc}} \geq 315\,\mathrm{V}$ with $U_{\mathrm{dc,max}} = U_{\mathrm{b,max}}$. The values of $\bar{U}_{\mathrm{dc}}$ and $C_{\mathrm{dc,min}}$ considered in the simulations (**Fig. 5**) and in the experimental verification (**Fig. 9**, **Fig. 10**) are highlighted with a circle and a cross, respectively.

comply with (10) for the conventional operation illustrated in **Fig. 2a** [14,24]. The resulting minimum values $U_{\mathrm{dc,min}}$ and maximum values $U_{\mathrm{dc,max}}$ within a fundamental period of the dc-link voltage $U_{\mathrm{dc,x}}(t)$ are also highlighted in **Fig. 6** on the second y-axis. There it becomes obvious that for $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ the minimum dc-link capacitor value $C_{\mathrm{dc,min}}$ is constrained by the maximum dc-link voltage value $U_{\mathrm{dc,max}}$ and (10).

Hence, lowering the average dc-link voltage to $\bar{U}_{\mathrm{dc}} = 315\,\mathrm{V}$ (at this point $C_{\mathrm{dc,min}}$ is equally constrained from (6) and (10)) allows operation with a substantially lower $C_{\mathrm{dc,min}} = 88\,\mu\mathrm{F}$ (i.e., a 62 % reduction compared to $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$). Note that now the grid voltage amplitude is larger than the average dc-link voltage $\hat{U}_{\mathrm{ac}} > \bar{U}_{\mathrm{dc}}$ (i.e., conventional operation with $\bar{u}_{\mathrm{CM}} = 0$ is not possible) and the corresponding main PFC rectifier front-end waveforms are presented in **Fig. 5b**. Here, the dc-link capacitor utilization is high (i.e., a small C_{dc} is sufficient to maintain PFC rectifier operation) and a voltage fluctuation of $\Delta U_{\mathrm{dc}} = 176.7\,\mathrm{V}$ results. This heavily impacts the input power waveforms and increases the energy buffering requirement to $\Delta E_{\mathrm{dc}} = 4.8\,\mathrm{J}$. Note that such a high ΔU_{dc} imposes substantial current stresses on the dc-link capacitors C_{dc} and a wide input-voltage range for the subsequent isolated dc-dc converter stages which needs to be considered in the system design.

Then, for a further decrease of the average dc-link voltage $\bar{U}_{\mathrm{dc}}$, the minimum dc-link capacitor value $C_{\mathrm{dc,min}}$ is constrained by (6) and increases again. E.g., for $\bar{U}_{\mathrm{dc}} = 300\,\mathrm{V}$ (**Fig. 5c**) and $\bar{U}_{\mathrm{dc}} = 290\,\mathrm{V}$ (**Fig. 5d**), a minimum dc-link capacitor value of $C_{\mathrm{dc,min}} = 116\,\mu\mathrm{F}$ and $C_{\mathrm{dc,min}} = 179\,\mu\mathrm{F}$, respectively, is required and compared to $\bar{U}_{\mathrm{dc}} = 315\,\mathrm{V}$ the dc-link voltage fluctuation reduces again.

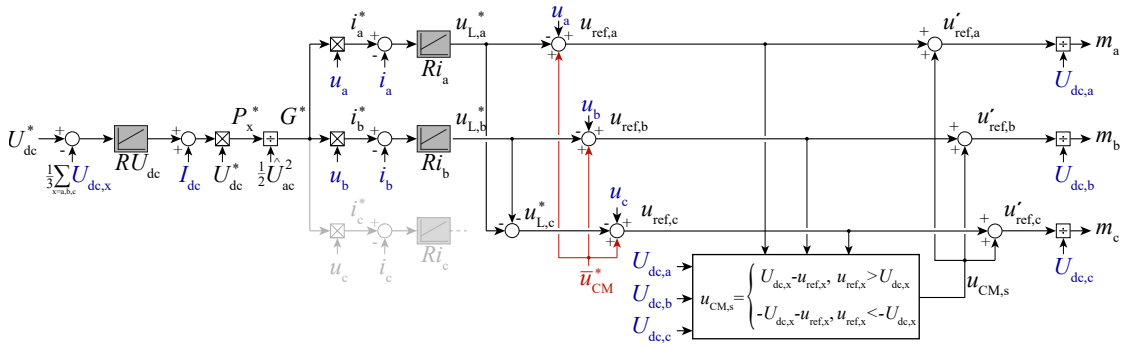

Fig. 7. Considered PFC rectifier control structure comprising the saturable CM voltage modulator from [20,25] setting $u_{\mathrm{CM,s}}$ such that in each module x the LF switch node voltage $\bar{u}_{\mathrm{x\bar{N}}}(t)$ remains below the limit imposed by the dc-link voltage $U_{\mathrm{dc,x}}(t)$, i.e., $\bar{u}_{\mathrm{x\bar{N}}}(t) \in [-U_{\mathrm{dc,x}}(t), U_{\mathrm{dc,x}}(t)]$.

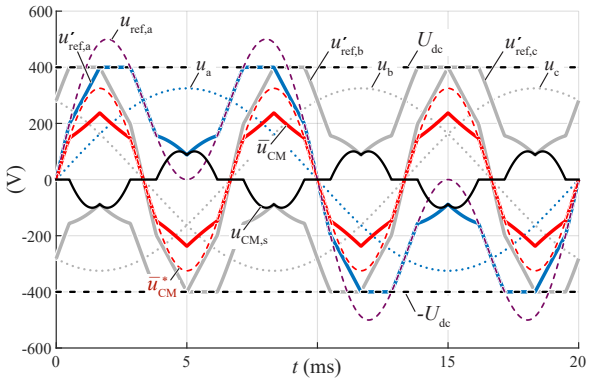

Fig. 8. Simplified voltage waveforms of the PFC rectifier control structure in **Fig. 7**: A large open-loop third-harmonic voltage reference $\bar{u}_{\mathrm{CM}}^*$ is added to the grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$ which results in reference voltages $u_{\mathrm{ref,a}}, u_{\mathrm{ref,b}}, u_{\mathrm{ref,c}}$ (only $u_{\mathrm{ref,a}}$ is shown) exceeding the (ideally constant) dc-link voltage U_{dc}. To maintain grid current controllability according to (6) the saturable CM voltage modulator [20] adds a correction term $u_{\mathrm{CM,s}}$, resulting in the final reference voltages $u'_{\mathrm{ref,a}}, u'_{\mathrm{ref,b}}, u'_{\mathrm{ref,c}}$ with the CM component $\bar{u}_{\mathrm{CM}}$ which is very similar to the optimal CM voltage waveform in **Fig. 4a** but shows limited $\mathrm{d}\bar{u}_{\mathrm{CM}}/\mathrm{d}t$ values at the CM voltage zero crossing at $k \cdot 60^\circ$ ($k \in \mathbb{N}$).

In closing it can be stated that the optimal CM modulation of **Sec. II-C** enables operation with lower dc-link capacitor values C_{dc} and/or lower average dc-link voltage $\bar{U}_{\mathrm{dc}}$ compared to conventional operation and the goal is hence to verify these findings in practice.

III. PFC Rectifier Control with Optimal CM Injection Modulation

The identified optimum modulation requires a special control structure for the three PFC rectifier front-ends [20]–[23,25] as for a given point in time one out of three phases completely ceases switching and clamps the switch node potential to either the positive or negative dc-link rail and the remaining two phases realize sinusoidal three-phase grid currents $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$ resulting in a collaborative control where the burden of the grid current control is shared among the PFC rectifier front-ends.

The considered cascaded PFC rectifier control structure is depicted in **Fig. 7**. The dc-link voltage regulator RU_{dc} (implemented as a Proportional-Integral (PI) controller) sets a grid conductivity reference value $G^* = \hat{I}_{\mathrm{ac}}^*/\hat{U}_{\mathrm{ac}}$ (i.e., the grid current amplitude reference $\hat{I}_{\mathrm{ac}}^*$ normalized by the grid voltage amplitude $\hat{U}_{\mathrm{ac}}$, with the unit Ω^{-1}) based on the instantaneous dc-link voltage error and the dc module output current feed-forward term I_{dc}. Note that here the instantaneous mean dc-link voltage $\frac{1}{3}\sum_{x\in\{a,b,c\}} U_{\mathrm{dc,x}}$ is considered to later obtain symmetric three-phase current references. In case the dc-link voltage balancing among the three-modules cannot be guaranteed by the subsequent isolated dc-dc converter stages, the control strategy of [2,26] would need to be implemented.

A sinusoidal grid current reference value i_{x}^* with $x \in \{a, b, c\}$ is then obtained by multiplying G^* with the respective grid voltage u_{x}. The grid current reference values are then tracked by the phase current controllers Ri_{x} (again implemented as PI controllers) where only two out of three grid currents are regulated (here the currents of phase a and b) and the third control signal is derived with a symmetry condition as only two degrees of freedom exist for the grid currents in an open-starpoint configuration of three PFC rectifier front-ends.

Next, the measured grid voltages are added as feed-forward terms to the phase current controller outputs. The optimal CM voltage injection is realized by means of the saturable CM voltage modulator from [20] with the main controller voltage waveforms highlighted in **Fig. 8**: A large open-loop CM voltage reference $\bar{u}_{\mathrm{CM}}^* = M_{\mathrm{3rd}} \cdot \hat{U}_{\mathrm{ac}} \sin(3\omega_{\mathrm{ac}} t)$ (with e.g., $M_{\mathrm{3rd}} = 1.0$) is added as a feed-forward term to the controller outputs. It is important to clarify that for $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ the resulting voltage reference $u_{\mathrm{ref,x}}$ with $M_{\mathrm{3rd}} = 1.0$ violates the current controllability constraint (6). Therefore, in a second step the saturable CM voltage modulator sets a correction term $u_{\mathrm{CM,s}}$ such that in each module x the final reference voltage $u'_{\mathrm{ref,x}}(t)$ remains below the limit imposed by the dc-link voltage $U_{\mathrm{dc,x}}(t)$ (corresponding to $u_{\mathrm{x\bar{N}}} \in [-U_{\mathrm{dc,x}}(t), U_{\mathrm{dc,x}}(t)]$). Finally, the adjusted reference voltages $u'_{\mathrm{ref,x}}$ are translated into modulation indices $m_{\mathrm{x}} \in [-1, 1]$ by division with the respective instantaneous dc-link voltage which allows to generate the power semiconductor control signals in each PFC rectifier front-end by means of PWM for the HF bridge-leg and based on the sign of m_{x} for the LF bridge-leg (see **Fig. 1a**).

Note that by increasing M_{3rd}, the $\mathrm{d}\bar{u}_{\mathrm{CM}}/\mathrm{d}t$ at the CM voltage zero crossing (occurring at $k \cdot 60^\circ$ ($k \in \mathbb{N}$) becomes increasingly steep and approaches the ideal waveforms of

Fig. 4a where a CM voltage step occurs when the clamping reference transitions from one phase to another. However, as found in **Sec. II-C** the finite $\mathrm{d}\bar{u}_{\mathrm{CM}}/\mathrm{d}t$ (resulting there as a consequence of the time discretization) only marginally impacts the energy buffering requirement ΔE_{dc}. Further, a CM voltage reference step might negatively impact the current controllers, such that $M_{\mathrm{3rd}} = 1.0$ is considered in the experimental verification of the concept.

IV. Experimental Verification

For the experimental verification of the proposed concept an existing 6 kW prototype system according to **Table I** is employed and details on the hardware can be found in Ref. [17]. The converter comprises three single-phase PFC rectifier front-ends and three individual resistive loads are used to emulate the subsequent isolated dc-dc converter stages and for the operating point in **Fig. 9a** the dc-link voltage (and hence module dc output current) fluctuation remains below $\pm 10\,\%$.

Experimental nominal power PFC rectifier front-end waveforms for conventional modulation with $\bar{u}_{\mathrm{CM}} = 0$ are depicted in **Fig. 9a** where a sinusoidal grid current i_{a} can be observed. **Table II** lists the measured performance with $\Delta E_{\mathrm{dc}} = 6.5\,\mathrm{J}$ (serving in the following as the base value for the relative energy buffering reduction) buffered by the dc-link capacitor in phase a. Note that here, the maximum value of the dc-link voltage $U_{\mathrm{dc,max}}$ exceeds the target value from (10) of $U_{\mathrm{b,max}} = 420\,\mathrm{V}$ which prevents the use of 600 V power semiconductors (as discussed in **Sec. II-D** a dc-link capacitor minimum value of $C_{\mathrm{dc,min,0}} = 400\,\mu\mathrm{F}$ is required to allow sufficient voltage blocking margin for $\bar{u}_{\mathrm{CM}} = 0$). This, however, is not problematic for the prototype system (also allowing operation in delta-configuration with $\bar{U}_{\mathrm{dc}} = 700\,\mathrm{V}$) employing 1.2 kV SiC power semiconductors.

Fig. 9b depicts the main converter waveforms for the optimal CM voltage modulation from **Sec. II-C**: There, the PFC rectifier front-end voltages are non-sinusoidal and only two out of three modules perform operation with PWM at any given point in time and $\Delta E_{\mathrm{dc}} = 3.8\,\mathrm{J}$ is reduced – as predicted – by more than 40 % compared to **Fig. 9a**. The large CM voltage injection slightly increases the grid current distortion, however, the grid current i_{a} remains sinusoidal and a small Total Harmonic Distortion (THD) of 3.0 % results.

Next, the goal is to verify the operation limits of the optimal CM voltage modulation with respect to minimum average dc-link voltage $\bar{U}_{\mathrm{dc}}$ and/or dc-link capacitance C_{dc} according to **Sec. II-D**. The nominal dc-link capacitance of the prototype system is $C_{\mathrm{dc}} = 240\,\mu\mathrm{F} = 6 \times 40\,\mu\mathrm{F}$ realized with film capacitors and can be decreased in steps of $40\,\mu\mathrm{F}$ to approximate the operating conditions highlighted in **Fig. 6**. The dc-link capacitance C_{dc} measured with an LCR-meter slightly deviates from the nominal capacitance value due to component tolerances and is stated in **Table II** for each considered operating point.

Fig. 10a presents operation with an average dc-link voltage reduced to $\bar{U}_{\mathrm{dc}} = 317\,\mathrm{V}$ which enables minimum dc-link capacitance operation with $C_{\mathrm{dc}} = 80\,\mu\mathrm{F}$ while complying with (6) and (10). The grid current i_{a} shows notable distortion but remains largely sinusoidal despite the massive dc-link voltage fluctuation ΔU_{dc} and the grid current THD results to 5.9 %. It is important to highlight that $\Delta E_{\mathrm{dc}} = 5.0\,\mathrm{J}$ is elevated compared to **Fig. 9b**. Hence, this operating condition represents the maximum dc-link capacitor utilization, i.e., a small C_{dc} (with a large voltage fluctuation ΔU_{dc}) is sufficient to maintain PFC rectifier operation, and not the minimum energy buffering requirement. Despite this large dc-link voltage fluctuation ΔU_{dc}, the measured buffered energy ΔE_{dc} (with resistive loads) closely matches the calculated value (where isolated dc-dc converter stages with constant input power are considered) with a small deviation $<5\,\%$.

When further lowering the average dc-link voltage $\bar{U}_{\mathrm{dc}}$ the minimally required dc-link capacitor value C_{dc} increases again and **Fig. 10b** presents converter waveforms for $\bar{U}_{\mathrm{dc}} = 298\,\mathrm{V}$ and $C_{\mathrm{dc}} = 120\,\mu\mathrm{F}$, with $\Delta E_{\mathrm{dc}} = 5.1\,\mathrm{J}$. There, the dc-link voltage fluctuation ΔU_{dc} is reduced compared to **Fig. 10a** such that also the grid current quality is notably improved with a THD of 4.1 %.

Last, **Fig. 10c** presents experimental waveforms close to the lower bound of feasible average dc-link voltage with $\bar{U}_{\mathrm{dc}} = 284\,\mathrm{V}$ where the dc-link capacitor values are increased again to $C_{\mathrm{dc}} = 240\,\mu\mathrm{F}$. There, the maximum dc-link voltage advantageously remains low with $U_{\mathrm{dc,max}} < 320\,\mathrm{V}$ and $\Delta E_{\mathrm{dc}} = 4.9\,\mathrm{J}$.

In closing it can be stated that the optimal CM modulation of **Sec. II** and the associated energy buffering savings and extreme operating conditions with minimum dc-link voltage and/or capacitance are successfully verified by the experimental results provided in this section.

V. Conclusion

The phase-modular isolated three-phase Power Factor Correction (PFC) ac-dc converter structure with individual isolated dc-dc converter stages presented in **Fig. 1a** advantageously facilitates the use of standard single-phase equipment and the low 400 V dc-link voltage level allows to use high performance 600 V semiconductors. The main drawback of this topology, however, is the fact that the time-varying single-phase input power only sums to a constant three-phase output power at the isolated dc output voltage, such that large dc-link capacitor values are required. Therefore, recent literature proposes to reduce the dc-link energy buffering requirement ΔE_{dc} by means of a third-harmonic Common-Mode (CM) voltage injection modulation.

This paper identifies the optimal CM voltage waveform with respect to minimizing ΔE_{dc} which results in a collaborative modulation where for a given point in time only two out of three phases operate with Pulse Width Modulation (PWM) while the third phase ceases switching. Further, optimal CM voltage modulation with reduced dc-link voltage levels and/or dc-link capacitance values is investigated. Experimental results with a 6 kW prototype system yield a reduction in ΔE_{dc} by up to 42 % or, alternatively, operation with an average dc-link voltage below 285 V, which closely match the theoretical considerations.

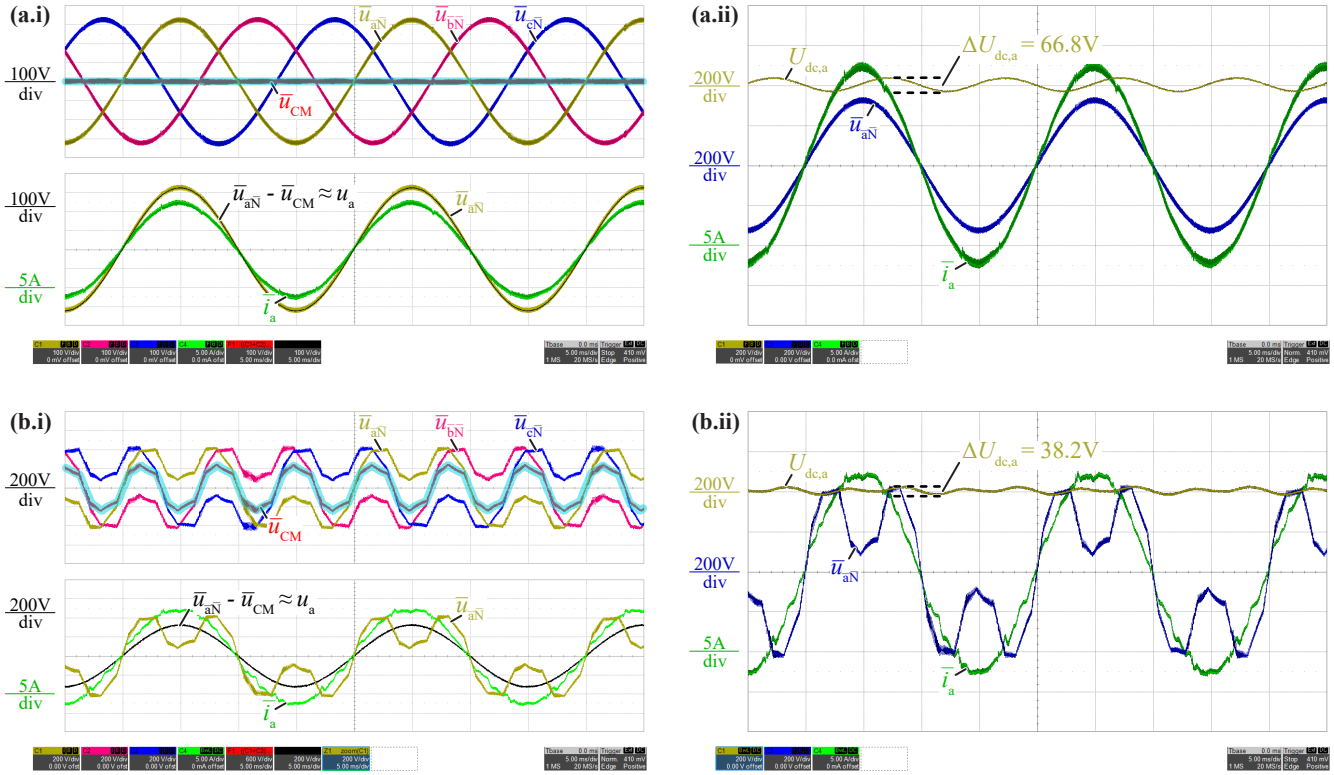

Fig. 9. Experimental nominal power PFC rectifier front-end waveforms obtained with a 6 kW prototype system according to the system specifications in **Table I** for **(a)** conventional modulation (with $\bar{u}_{\mathrm{CM}} = 0$, $\Delta E_{\mathrm{dc}} = 6.5\,\mathrm{J}$) and **(b)** optimal CM voltage injection (with $\bar{u}_{\mathrm{CM,opt}}$, $\Delta E_{\mathrm{dc}} = 3.8\,\mathrm{J}$): **(x.i)** LF PFC rectifier front-end input voltages $\bar{u}_{a\bar{N}}, \bar{u}_{b\bar{N}}, \bar{u}_{c\bar{N}}$, LF CM voltage $\bar{u}_{\mathrm{CM}} = \frac{1}{3}(\bar{u}_{a\bar{N}} + \bar{u}_{b\bar{N}} + \bar{u}_{c\bar{N}})$ (highlighted with a semi-transparent cyan line), and grid current i_{a} of phase a. **(x.ii)** phase a LF PFC rectifier front-end input voltage $\bar{u}_{a\bar{N}}$, grid current i_{a}, and dc-link voltage $U_{\mathrm{dc,a}}$.

TABLE II: MEASUREMENT RESULTS.

Mod.	C_{dc} nom. (meas.)	U_{dc} meas.	$U_{\mathrm{dc,max}}$ meas.	$U_{\mathrm{dc,min}}$ meas.	ΔE_{dc} meas. (meas. rel.)	ΔE_{dc} calc.	THD_{40} meas.
Fig. 9a	240 µF (244 µF)	400 V	433 V	367 V	6.5 J (100 %)	6.4 J	1.4 %
Fig. 9b	240 µF (244 µF)	405 V	425 V	385 V	3.8 J (58.4 %)	3.6 J	3.0 %
Fig. 10a	80 µF (84 µF)	317 V	390 V	235 V	5.0 J (77.0 %)	4.8 J	5.9 %
Fig. 10b	120 µF (124 µF)	298 V	358 V	238 V	5.1 J (79.4 %)	4.9 J	4.1 %
Fig. 10c	240 µF (244 µF)	284 V	319 V	250 V	4.9 J (76.0 %)	4.9 J	3.9 %

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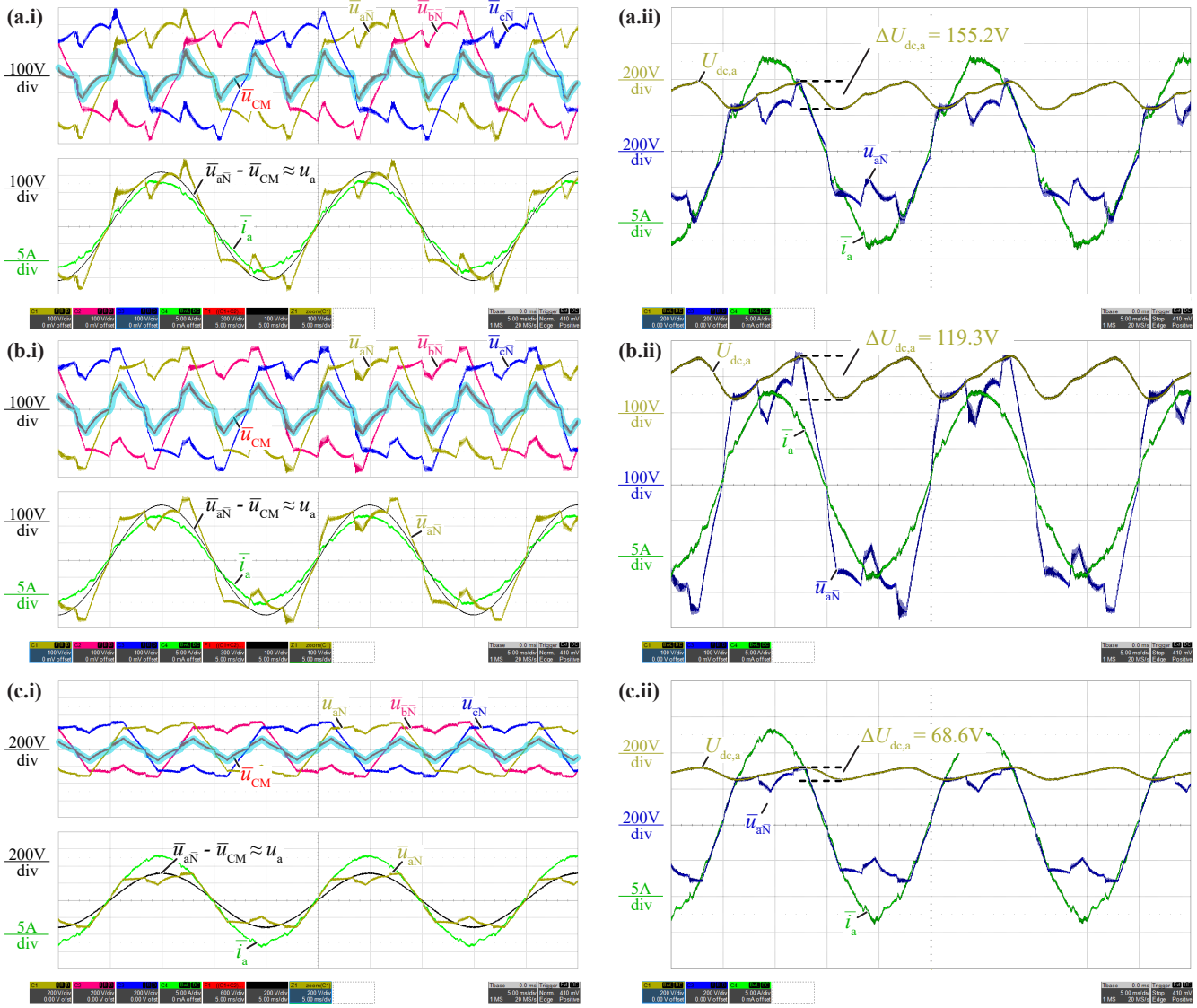

Fig. 10. Experimental nominal power PFC rectifier front-end waveforms for optimal CM voltage injection obtained with a 6 kW prototype system according to the system specifications in **Table I** and with minimum average dc-link voltage $\bar{U}_{\mathrm{dc}}$ and/or dc-link capacitor C_{dc} values (see **Fig. 6**), i.e., **(a)** $\bar{U}_{\mathrm{dc}} = 317\,\mathrm{V}$, $C_{\mathrm{dc}} = 80\,\mu\mathrm{F}$, and $\Delta E_{\mathrm{dc}} = 5.0\,\mathrm{J}$, **(b)** $\bar{U}_{\mathrm{dc}} = 298\,\mathrm{V}$, $C_{\mathrm{dc}} = 120\,\mu\mathrm{F}$, and $\Delta E_{\mathrm{dc}} = 5.1\,\mathrm{J}$, **(c)** $\bar{U}_{\mathrm{dc}} = 284\,\mathrm{V}$, $C_{\mathrm{dc}} = 240\,\mu\mathrm{F}$, and $\Delta E_{\mathrm{dc}} = 4.9\,\mathrm{J}$. **(x.i)** LF PFC rectifier front-end input voltages $\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}, \bar{u}_{\bar{\mathrm{b}}\bar{\mathrm{N}}}, \bar{u}_{\bar{\mathrm{c}}\bar{\mathrm{N}}}$, LF CM voltage $\bar{u}_{\mathrm{CM}} = \frac{1}{3}(\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}} + \bar{u}_{\bar{\mathrm{b}}\bar{\mathrm{N}}} + \bar{u}_{\bar{\mathrm{c}}\bar{\mathrm{N}}})$ (highlighted with a semi-transparent cyan line), and grid current i_{a} of phase a. **(x.ii)** phase a LF PFC rectifier front-end input voltage $\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}$, grid current i_{a}, and dc-link voltage $U_{\mathrm{dc,a}}$.

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APPENDIX A
IMPACT OF THE DC-LINK VOLTAGE ON THE OPTIMAL CM VOLTAGE TRAJECTORY

The analysis in **Sec. II** is limited to $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ and this Appendix further provides the optimal CM voltage trajectories obtained with the method from **Sec. II-B** for different dc-link voltage levels $\bar{U}_{\mathrm{dc}} = \{300\,\mathrm{V}, 400\,\mathrm{V}, 500\,\mathrm{V}, 600\,\mathrm{V}\}$.

Fig. 11a considers $\bar{U}_{\mathrm{dc}} = 300\,\mathrm{V}$ with $\bar{U}_{\mathrm{dc}} < \hat{U}_{\mathrm{ac}}$ such that the eligible LF CM voltage range according (7) does not allow for conventional modulation with $\bar{u}_{\mathrm{CM}} = 0$ as $\bar{u}_{\mathrm{CM,max}}$ and $\bar{u}_{\mathrm{CM,min}}$ change signs during one fundamental period. Here, the optimal CM voltage trajectory $\bar{u}_{\mathrm{CM,opt}}$ results in $\Delta E_{\mathrm{dc}} = 4.6\,\mathrm{J}$ and corresponds to a DPWM strategy, where the switch-node $\bar{x}$ of the phase x with the instantaneous middle absolute grid voltage value is clamped to the positive (if $u_{\mathrm{x}} > 0$) or negative (if $u_{\mathrm{x}} < 0$) dc-link rail [20,21]. Hence, the same modulation strategy is optimal for both $\bar{U}_{\mathrm{dc}} = 300\,\mathrm{V}$ and $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ (shown in **Fig. 11b** for completeness) where the larger range of eligible CM voltages (7) with $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ enables an improved energy buffering requirement of $\Delta E_{\mathrm{dc}} = 3.6\,\mathrm{J}$ compared to $\bar{U}_{\mathrm{dc}} = 300\,\mathrm{V}$ with $\Delta E_{\mathrm{dc}} = 4.6\,\mathrm{J}$.

For a further increase in the dc-link voltage (**Fig. 11c,d**), the optimal CM voltage injection strategy changes, as the continuous clamping of the middle phase would overcompensate the instantaneous power pulsation, and $\Delta E_{\mathrm{dc}} = 3.1\,\mathrm{J}$ and $\Delta E_{\mathrm{dc}} = 3.0\,\mathrm{J}$ can be achieved for $\bar{U}_{\mathrm{dc}} = 500\,\mathrm{V}$ and $\bar{U}_{\mathrm{dc}} = 600\,\mathrm{V}$, respectively, which is below the theoretically achievable limit for pure third-harmonic voltage injection modulation [14]. However, it is important to highlight that for $\bar{U}_{\mathrm{dc}} = 500\,\mathrm{V}$ and $\bar{U}_{\mathrm{dc}} = 600\,\mathrm{V}$ power semiconductors with a rated voltage $> 600\,\mathrm{V}$ are required, thereby mitigating one of the main advantages of the converter concept such that these dc-link voltage levels are less of a practical interest.

APPENDIX B
OPERATION IN UNBALANCED MAINS

The analysis in **Sec. II** is performed assuming an ideally symmetric three-phase grid. In case of a grid voltage imbalance the range of feasible LF CM voltages (7) (to satisfy the boost-type ac-dc converter voltage limit according to (6)) is altered and **Fig. 12** presents the resulting maximum $\bar{u}_{\mathrm{CM,max}}$ and minimum CM voltage $\bar{u}_{\mathrm{CM,min}}$ for a 20 % reduced voltage amplitude $\hat{U}_{\mathrm{ac}}$ in phase a. Despite the grid voltage imbalance, the clamping strategy from II-C can be employed, where the resulting LF CM voltage waveform $\bar{u}_{\mathrm{CM}}$ is no longer 120° symmetric.

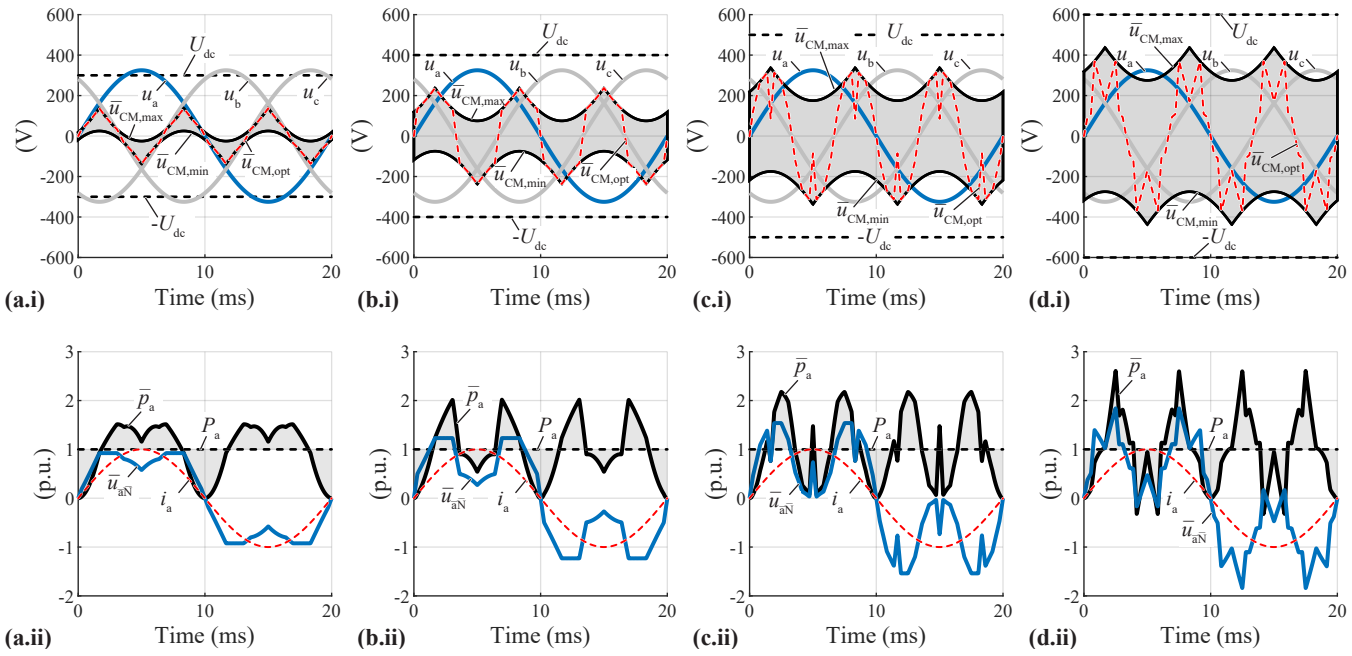

Fig. 11. Optimal LF CM voltage waveform (evaluated with $n_{\mathrm{u}} = 9$ and $n_{\mathrm{t}} = 73$) for the system specifications in **Table I**, with $C_{\mathrm{dc}} \to \infty$, and **(a)** $\bar{U}_{\mathrm{dc}} = 300\,\mathrm{V}$ ($\Delta E_{\mathrm{dc}} = 4.6\,\mathrm{J}$), **(b)** $\bar{U}_{\mathrm{dc}} = 400\,\mathrm{V}$ ($\Delta E_{\mathrm{dc}} = 3.6\,\mathrm{J}$), **(c)** $\bar{U}_{\mathrm{dc}} = 500\,\mathrm{V}$ ($\Delta E_{\mathrm{dc}} = 3.1\,\mathrm{J}$), **(d)** $\bar{U}_{\mathrm{dc}} = 600\,\mathrm{V}$ ($\Delta E_{\mathrm{dc}} = 3.0\,\mathrm{J}$): **(x.i)** grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$, ideally constant dc-link voltage $U_{\mathrm{dc}} = \bar{U}_{\mathrm{dc}}$, eligible LF CM voltage range (highlighted by a light gray area) limited by $\bar{u}_{\mathrm{CM,max}}$ and $\bar{u}_{\mathrm{CM,min}}$ according to (7), and optimal CM voltage waveform $\bar{u}_{\mathrm{CM,opt}}$. **(x.ii)** phase a LF PFC rectifier front-end input voltage $\bar{u}_{\mathrm{a\bar{N}}}$, grid current i_{a}, and LF input power $\bar{p}_{\mathrm{a}}$.

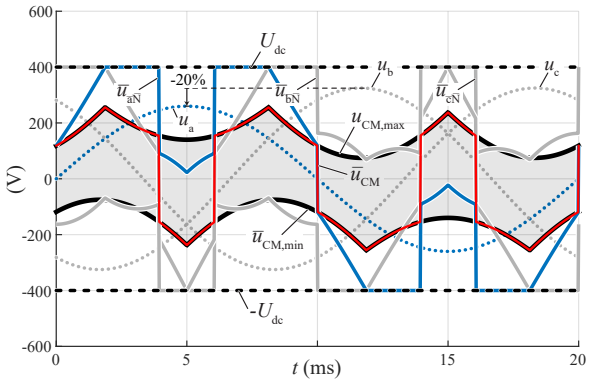

Fig. 12. Optimal LF CM voltage waveform from **Fig. 4a** for an unbalanced grid where the phase a voltage amplitude $\hat{U}_{\mathrm{ac}}$ is decreased by 20 %: grid voltages $u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$, ideally constant dc-link voltage $U_{\mathrm{dc}} = \bar{U}_{\mathrm{dc}}$, LF PFC rectifier front-end input voltages $\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}, \bar{u}_{\bar{\mathrm{b}}\bar{\mathrm{N}}}, \bar{u}_{\bar{\mathrm{c}}\bar{\mathrm{N}}}$, eligible LF CM voltage range (highlighted by a light gray area) limited by $\bar{u}_{\mathrm{CM,max}}$ and $\bar{u}_{\mathrm{CM,min}}$ according to (7), and optimal CM voltage waveform $\bar{u}_{\mathrm{CM}}$.

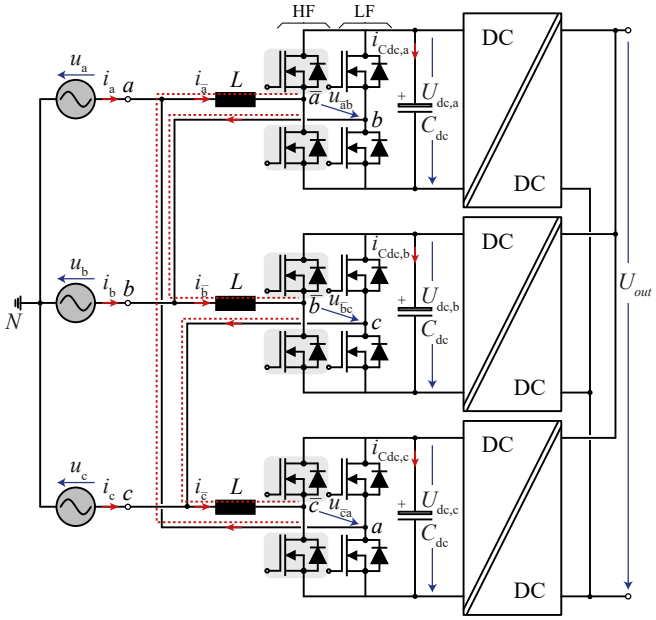

Fig. 13. Phase-modular three-phase isolated PFC ac-dc converter system with a delta (Δ) arrangement of the PFC rectifier front-ends [17] (with a typical average dc-link voltage level of $\bar{U}_{\mathrm{dc}} = 700\,\mathrm{V}$ for a grid with $230\,\mathrm{V_{rms}}$ line-to-neutral voltage): The LF CM current circulating inside the Δ-connection (the current path is highlighted with a red dashed line) does not impact the grid currents and allows to alter the LF input power flows of the modules.

APPENDIX C
OPTIMAL CM CURRENT INJECTION MODULATION OF DELTA-CONNECTED PHASE-MODULAR ISOLATED THREE-PHASE PFC AC-DC CONVERTERS

It is important to highlight that the discussed optimal CM modulation strategy can also be employed to a delta (Δ) arrangement of the PFC rectifier front-ends [17] where an LF CM *current* $\bar{i}_{\mathrm{CM}}$ circulates between the modules (the CM current path is highlighted in **Fig. 13**) and thereby allows to redistribute the grid input power pulsation. Here, the three module input currents $i_{\bar{\mathrm{a}}}, i_{\bar{\mathrm{b}}}, i_{\bar{\mathrm{c}}}$ are individually controlled and details on the required control structure can be found in [17]. Further, the dc-link voltages do not directly impose an upper bound for the LF CM current reference (as it is the case for the LF CM voltage reference with (7) for the star-connection of the modules in **Fig. 1a**). However, high values of the LF CM current amplitude are accompanied by additional conduction losses in the ac-dc front-end power semiconductors and boost inductors L (which are then also required to feature a higher saturation compared to conventional modulation with $\bar{i}_{\mathrm{CM}} = 0$), such that the optimal LF CM current waveform $\bar{i}_{\mathrm{CM,opt}}$ cannot be identified a priori for a given grid voltage amplitude and dc-link voltage level (as it is the case for the star-connection of the modules in **Fig. 1a**), but needs to be assessed separately for each specific converter design.

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